# Czech Technical University in Prague

## Faculty of Electrical Engineering

Electronics & communications
Department of microelectronics

# Physical Simulations of the Behavior of Integrated Current Sensors

MASTER'S THESIS

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ČVUT ČESKÉ VYSOKÉ UČENÍ TECHNICKÉ V PRAZE

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2) Focus on electro-mechanical-thermal simulations of the current sensor behavior and create its model.
3) Discuss possible modifications to the topology of the sensor and surrounding system components from the point of view of minimizing negative effects.
4) Compare the parameters and behavior of the designed model with a real structure.

Seznam doporučené literatury:

1) Ansys learning hub:
https://courses.ansys.com/index.php/courses/intro-to-ansys-hfss/lessons/intro-to-aedt-user-interface-lesson-1/
2) Freescale Semiconductor (2008), Thermal Analysis of Semiconductor Systems [White paper],
https://www.nxp.com/docs/en/white-paper/BasicThermalWP.pdf

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Datum převzetí zadání Podpis studenta


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# Declaration

I declare that I prepared the assigned master's thesis independently with the contribution of the thesis supervisors, both at school and at the company Allegro MicroSystems, and I have conscientiously listed all the materials used (literature, catalog sheets,…) in the attached list below.

In Prague on ……………………….                                                ……………………………….

Matěj Hašek

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My thanks go to Ing. Vladimír Janíček, Ph.D. for guiding my thesis. A big thank you goes to Ing. Radek Krystián for guiding my work in the Allegro MicroSystems company and for the advice, discussions and help during struggling. And finally, all my thanks go to all my loved ones who have always been here for me as my immense support.

Matěj Hašek

**Abstrakt**

Tato práce se věnuje problematice teplotních vlivů na proudové integrované senzory a celé systémy. Zaměřena je zejména na zkoumání teplotních gradientů. V práci je vytvořený model celého systému který je následně zkoumán elektro-teplotně-mechanickými simulacemi. Model je vytvořen pro systém s šesti vrstvou deskou plošného spoje a s dvou vrstvou deskou plošného spoje. V práci jsou rozebrány dva postupy jak celý systém odsimulovat. Hlavním výstupem je zkoumání teplotního rozložení a teplotního gradientu v oblastech čipu. Následně je zkoumán rozdíl vlivu kvality DPS na teplotní chování systému. Výsledky jsou potvrzeny laboratorním měřením. Dále jsou provedé mechanické simulace v závislosti na teplotě pro DPS s připojeným integrovaným obvodem. Nakonec jsou navrženy a odsimulovány 4 alternativní návrhy pro zlepšní teplotních parametrů během měření stejnosměrného či střídavého proudu vylepšením pomocí chladiče, změnami v pouzdře či ve vodivých částech.



**Klíčová slova** – proudový senzor, integrovaný obvod, simulace desky plošného spoje, teplotní gradient, elektro-teplotně-mechanické simulace



**Abstract**

This publication focuses on the problem of temperature effects on integrated current sensors and entire systems. It is mainly focused on the investigation of the temperature gradients. In the thesis, a model of the entire system is created, which is subsequently investigated by electro-thermal-mechanical simulations. The model is created for the six-layer and two-layer printed circuit boards. Two procedures for simulating the entire system are analyzed in the thesis. The main output is the examination of the temperature distribution and temperature gradient in the areas of the chip. Subsequently, the difference in the influence of PCB quality on the thermal behavior of the system is investigated. The results are confirmed by the laboratory measurements. Next, mechanical simulations are made for the PCB and connected IC. Finally, 4 alternative designs are designed and simulated to improve the temperature parameters during direct or alternating current measurement by improving with a cooler, changes in the package, or conductive parts. The pros and cons of the upgrades are then discussed.



**Key words** – current sensor, integrated circuit, printed circuit board simulations, thermal gradient, electro-thermal-mechanical simulations

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# Tables of the used abbreviations and symbols

| Shortcut | Explanation |
|---|---|
| PCB | Printed Circuit Board |
| AC | Alternating Current |
| DC | Direct current |
| IC | Integrated Circuit |
| GMR | Giant Magneto Resistive |
| SOIC | Small Outline Integrated Circuit |
| PTH | Plated Through Hole |
| FEM | Finite Element Method |
| FVM | Finite Volume Method |
| EM | Electro-Magnetic |
| AEDT | Ansys Electronics Desktop |
| TIM | Thermal Interface Material |
| PC | Personal Computer |
| IP+ | Positive pin of the primary current loop |
| IP- | Negative pin of the primary current loop |
| Vcc | Supply voltage pin |
| GND | Ground pin |
| Vout | Output voltage pin |
| Vfault | Fault voltage pin |
| GUI | Graphical User Interference |

| Symbol | Explanation | Unit |
|---|---|---|
| $P$ | Power | $(\mathrm{W})$ |
| $I$ | Current | $(\mathrm{A})$ |
| $V$ | Voltage | $(\mathrm{V})$ |
| $R$ | Electrical resistance | $(\Omega)$ |
| $\rho$ | Electrical resistivity of the substance | $(\Omega\cdot\mathrm{m})$ |
| $L$ | Length | $(\mathrm{m})$ |
| $A$ | Area | $(\mathrm{m}^2)$ |
| $G$ | Electrical conductance | $(\mathrm{S})$ |
| $\sigma$ | Electrical conductivity of the substance | $(\mathrm{S/m})$ |
| $J$ | Current density | $(\mathrm{A/m}^2)$ |
| $E$ | Electric field | $(\mathrm{V/m})$ |
| $T$ | Temperature | $(°\mathrm{C}\text{ or }\mathrm{K})$ |
| $Q$ | Heat | $(\mathrm{W})$ |
| $q$ | Heat flux | $(\mathrm{W/m}^2)$ |
| $k$ | Thermal conductivity of the substance | $(°\mathrm{C}\cdot\mathrm{W/m})$ |
| $h$ | Heat transfer coefficient | $(°\mathrm{C}\cdot\mathrm{W/m}^2)$ |
| $E_{\mathrm{emis}}$ | Radiation | $(\mathrm{W/m}^2)$ |
| $\sigma_{\mathrm{const}}$ | Stefan-Boltzmann constant | $(\mathrm{K}^4\cdot\mathrm{W/m}^2)$ |
| $G_{\mathrm{irrad}}$ | Irradiation | $(\mathrm{W/m}^2)$ |
| $\epsilon$ | Emissivity | $(-)$ |
| $\alpha$ | Absorptivity | $(-)$ |
| $F$ | Point of view factor | $(-)$ |
| $\Delta T$ | Temperature gradient | $(°\mathrm{C}\text{ or }\mathrm{K})$ |
| $V_{\mathrm{H}}$ | Hall voltage | $(\mathrm{V})$ |
| $I_{bias}$ | Biasing current | $(\mathrm{A})$ |
| $I_{\mathrm{C}}$ | Forward current | $(\mathrm{A})$ |
| $I_{\mathrm{S}}$ | Reverse bias saturation current | $(\mathrm{A})$ |

| | | |
|---|---|---|
| $V_{\mathrm{BE}}$ | Forward voltage | $(\mathrm{V})$ |
| $V_{\mathrm{T}}$ | Thermal voltage | $(\mathrm{V})$ |
| $n$ | Ideality factor | $(-)$ |
| $k_{\mathrm{const}}$ | Boltzmann constant | $(\mathrm{J/K})$ |
| $q_{\mathrm{charge}}$ | Elementary charge | $(\mathrm{C})$ |
| $I_{\mathrm{load}}$ | Load current | $(\mathrm{A})$ |
| $P_{\mathrm{MAX}}$ | Maximal ohmic loss on the visualization | $(\mathrm{W/m^3})$ |
| $P_{\mathrm{solid}}$ | Total computed losses | $(\mathrm{W})$ |
| $J_{\mathrm{MAX}}$ | Maximal current density on the visualization | $(\mathrm{A/m^2})$ |

# 1. Introduction and motivation

In the modern world, a world full of advanced technologies, everything is interwoven together by electronics. From toys to high-tech satellites, we meet devices powered by electronics at every step of our everyday lives and nowadays we cannot imagine life without them. But while the systems that connect us and share our position or light can vary in many ways, nearly every electronic device shares the same fundamental building block – the small and very complex integrated circuit.

An Integrated Circuit (IC), commonly known as a chip, is a device made of a semiconductor material called silicon. Integrated circuits are compact electronic devices made up of interconnected components such as resistors, transistors, capacitors, etc. Built on a single piece of semiconductor material, such as silicon, the integrated circuit can contain hundreds to billions of components – all working together as one single part.

The uses and purposes of integrated circuits are vast. From children's toys to computers, cars, or even spaceships. Chip can function within each device as a microprocessor, amplifier, or memory. As more and more electronic devices are made, more chips are needed. Especially with new devices with many special smart functions. Integrated circuits can also be used with the function as current sensor.

As the electric vehicle market grows, more current sensors are needed. But the electric car market is not the only one. Integrated current sensors are also important in solar panel applications, washing machines, or the whole car industry. But as with all electronic devices also integrated circuits of every type must face issues with rising temperature [ 1 ], [ 2 ], [ 3 ].

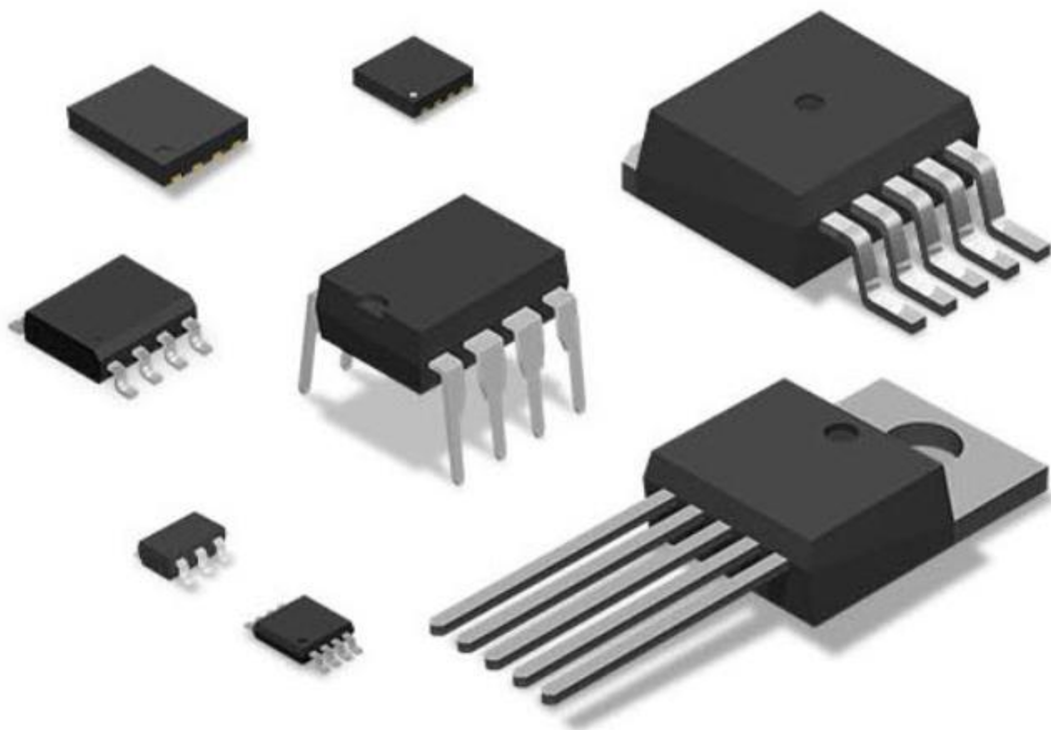

*Figure 1: Example of integrated circuits* [ 4 ]

# 2. Integrated Circuits and heat

Integrated circuits and whole electronics share common ailments. One of them and a very important one is heat. Heat can be a problem for IC and other electrical components. Ambient temperature can significantly influence the behavior of the parts, their accuracy, or even ordinary functionality. But ambient temperature is not the only problem.

Due to flowing current parts are generating extra heat. So, the parts themselves are unwanted heat generators. This is a thing that we cannot get rid of easily until a pure superconductor is invented. So, we must calculate with it because otherwise heat can cause damage to the part, or it can destroy the whole circuit in the worst case.

Each electrical component has a defined operating temperature range, in which functionality is ensured. But when the conditions are not met, the functionality may not be right. Many things can change with rising temperatures. Not speaking only about electronic stuff, material changes are also possible (like shortening or lengthening, etc.). In short, too much heat can cause total disaster.

That is why it is important to determine heat generation and its dissipation. Electro-thermal simulations during the device design phase can show weaknesses of the whole system and can prevent future issues. Speaking about chips, the crucial parameter is also the thermal gradient across the chip die or even the thermal gradient across the whole system. Let's talk about heat in general [ 5 ].

## 2.1. Heat in electronic systems

Heat in electronic systems is given (besides ambient heat) by Joule's heating. Joule heating (also known as Ohmic or resistive heating) is a process by which the passage of an electric current through a conductor produces heat. Although Joule's heating has many practical applications (light bulb, electric fuse, etc.), it can cause trouble. Joule's heating can be easily calculated as

$$P = I \cdot V \quad [\mathrm{W}] \tag{1}$$

where $I$ $[\mathrm{A}]$ is current flowing through the element and $V$ $[\mathrm{V}]$ is voltage across the element. This means the higher the current the higher Joule's heat. Voltage can be calculated as

$$V = I \cdot R \quad [\mathrm{V}] \tag{2}$$

So, Joule's heat also depends on resistance of the element.

Ohmic resistance of the element is given by:

$$R = \rho \cdot \frac{L}{A} \quad [\Omega] \tag{3}$$

where $\rho$ is the electrical resistivity, $L$ $[\mathrm{m}]$ is length the of the element and $A$ $[\mathrm{m}^2]$ is the cross-sectional area of the conductor. As you can see, Joule's heat also depends on the material physical properties and its geometry.

Electrical resistivity, which is one of the physical characteristics of the material, can vary with temperature. Each material has its thermal modifier (change of resistivity with temperature). So, it is important to include this modifier in consideration. [ 6 ]

So, power $P$ can be expressed with use of Ohm's law as equations ( 4 ) and ( 5 ):

$$P = I^2 \cdot R \tag{4}$$

$$P = \frac{U^2}{R} = U^2 \cdot G \tag{5}$$

where $G$ [S] is the conductance of the material. The conductance is equal to the inverse of resistance. It can be expressed as:

$$G = \sigma \frac{A}{L} \tag{6}$$

where $\sigma$ is the electrical conductivity of the substance, $A$ is the cross-section area and $l$ is the length of the medium [ 7 ]. An also $\sigma = \frac{1}{\rho}$.

From the equations ( 1 ), ( 3 ), and ( 6 ) is quite straightforward that the heat in mass is dependent on many aspects. The crucial aspects are the geometry of the mass ($A$ and $L$), physical specifications ($\rho$ or $\sigma$), and connected filed ($V$ and $I$).

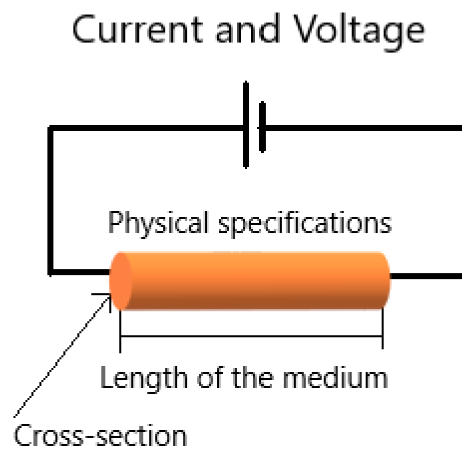


*Figure 2: Joule's heat*

Another possibility to calculate the Joule heating is to calculate it at a particular location in space. Therefore, Joule's heat can be calculated in differential form, and it is given by:

$$\frac{\mathrm{d}P}{\mathrm{d}V} = \mathbf{J} \cdot \mathbf{E} \tag{7}$$

where $\mathbf{J}$ is the current density, and $\mathbf{E}$ is the electric field. As a material in the system has its conductivity $\sigma$, and then $\mathbf{J} = \sigma\mathbf{E}$, equation ( 7 ) can be expressed as:

$$\frac{\mathrm{d}P}{\mathrm{d}V} = \mathbf{J} \cdot \mathbf{J}\frac{1}{\sigma} = J^2\frac{1}{\sigma} = J^2\rho \tag{8}$$

which directly corresponds to the "$I^2R$" macroscopic form [ 16 ].

# 3. Heat transfer

As I said, flowing current produces Joule's heat. So, the heat is generated in the metals and semiconductors in the chip. Due to the generated heat, these parts are warming up. So, the whole chip is getting warmer. And not chip only, but also other components of the system. This is caused by heat transfer. Heat transfer is a common mechanism familiar to everybody. People use Joule's heating in the kettle to make a cup of coffee. This process requires the transfer of heat from an electrical resistance element to the water [ 6 ], [ 8 ].

Due to thermodynamics, heat transfer is possible in three ways: conduction, convection, and radiation. In complex systems, all those three processes take part. Each of them works differently. Let's take a closer look at them [ 9 ].

## 3.1. Conduction

The first of the heat transfer modes is conduction. Conduction is the transmission of heat through a substance without apparent motion of the substance. It can be seen as the transfer of energy from the more energetic to the less energetic particles of a substance due to the interactions between the particles. So, higher temperatures are associated with higher energy.

Conductive transfer of energy is different among gas, liquid, and solid materials. In all these cases, heat transfer is caused by molecular interactions. In gas and liquid is the heat transfer caused by collisions. In a solid, conduction may be attributed to atomic activity in the form of lattice vibrations. In an electrical nonconductor, the energy transfer is exclusively via the lattice waves, in a conductor, it is a combination of lattice waves and the translational motion of the electrons.

On a microscopic level, the physical mechanisms of conduction are very complex. But at the macroscopic level, we can use phenomenological laws. The phenomenological law governing thermal conduction was proposed by J. B. Fourier – *Fourier's law of heat conduction*. I will describe this law on a simple problem of heat flow in one dimension across a plane wall.

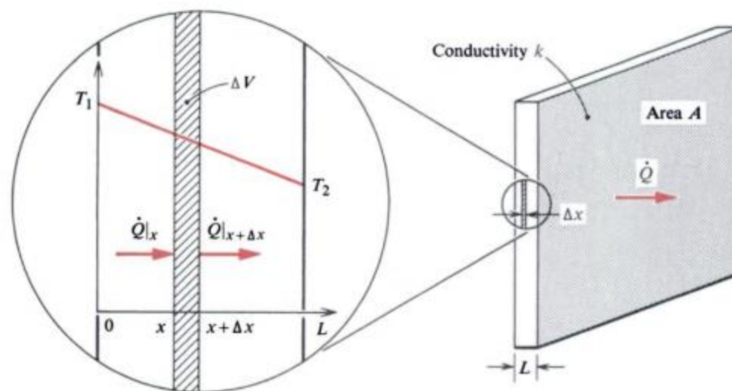


*Figure 3: Steady one-dimensional conduction across a plane wall* [ 11 ]

Figure 3 shows a plane wall of surface $A$ and thickness $L$. Its face is at $x = 0$ maintained at temperature $T_1$ and the face at $x = L$ maintained at $T_2$. The heat flow through the wall is $\dot{Q}$. Direction of the flow is in the decreasing temperature – if $T_1 > T_2$, $\dot{Q}$ is in the positive direction.

According to Fourier's law, the local heat flux is proportional to the negative of the local temperature gradient:

$$\frac{\dot{Q}}{A} = q \tag{9}$$

And

$$q \propto -\frac{\mathrm{d}T}{\mathrm{d}x} \tag{10}$$

where $q$ is the heat flux per unit area perpendicular to the flow direction $[\mathrm{W/m^2}]$, $T$ is the local temperature $[\mathrm{K\ or\ °C}]$, and $x$ is the coordinate in the flow direction $[\mathrm{m}]$. When the fraction is negative, the minus sign in equation ( 10 ) gives a positive $q$ in the positive $x$ direction because heat is transferred in the direction of decreasing temperature. This equation is supplemented by term $k$ which is proportional to *thermal conductivity of substance*. Units of equation are $\left[\frac{\mathrm{W}}{\mathrm{m}}\mathrm{K}\right]$ or $\left[\frac{\mathrm{W}}{\mathrm{m}}\mathrm{°C}\right]$:

$$q = -k\frac{\mathrm{d}T}{\mathrm{d}x} \tag{11}$$

Under the steady-state conditions shown in Figure 3, where the temperature distribution is linear, the temperature gradient may be expressed as

$$\frac{\mathrm{d}T}{\mathrm{d}x} = \frac{T_2 - T_1}{L} \tag{12}$$

And the equation for the heat flux is then:

$$q = -k\frac{T_2 - T_1}{L} = k\frac{\Delta T}{L} \tag{13}$$

From equation ( 9 ) heat flow is then

$$\dot{Q} = qA = -kA\frac{\mathrm{d}T}{\mathrm{d}x} \tag{14}$$

If we rearrange the equation and integrate it across the plane wall, we get:

$$\frac{\dot{Q}}{A}\int_0^L \mathrm{d}x = -\int_{T_1}^{T_2} k\ \mathrm{d}T \tag{15}$$

If we ignore small variations of $k$ with temperature, we get:

$$\dot{Q} = \frac{kA}{L}(T_1 - T_2) = \frac{T_1 - T_2}{\frac{L}{kA}} \tag{16}$$

This equation is a thermal analogy of Ohm's law. $\Delta T$ can be viewed as potential for heat flow (analogy to voltage) and $L/kA$ can be viewed as a thermal resistance analogous to electrical resistance (opposite to the thermal conductivity).

The thermal conductivity $\mathrm{k}$ of a substance depends on its microscopic structure. It is the ability to conduct heat. Thermal conductivity is different in different materials and tends to vary with temperature. Most materials with good electrical conductivity are good thermal conductors. For example, the thermal conductivity of copper is much higher than the thermal conductivity of epoxy or dielectric layers of PCB. This consideration can approximate a little how the distribution of heat could look like [ 10 ], [ 11 ], [ 12 ], [ 13 ].

## 3.2. Convection

The second of the heat transfer modes is convection. Convective heat transfer is the term used to describe the transfer of heat from a surface to a moving fluid when they are at different temperatures. Convection is comprised of two mechanisms. The first one is diffusion – random molecular motion. Energy is also transferred by the bulk motion of the fluid. So, the total heat transfer of convection is due to the superposition of energy transport by the random motion of the molecules and by the bulk motion of the fluid. The energy transport due to the bulk motion we call advection. Convection is usually classified according to the nature of the flow. Therefore, we speak about forced convection and natural convection.

The forced convection is the case when the flow is caused by external means, for example, by fan, pump, or atmospheric winds. A typical application can be a fan providing air cooling of hot electrical components on a PCB. On the other hand, flow in natural (free) convection is induced by buoyancy forces. These forces are due to density differences caused by temperature variations in the fluid. Fluid that contacts a component (solid, etc.) heated to higher temperature experiences an increase in temperature and so a reduction in density. This fluid becomes lighter and buoyancy forces induce vertical motion. An example of natural convection can be a heat transfer from the heat sink to the surroundings without external forces.

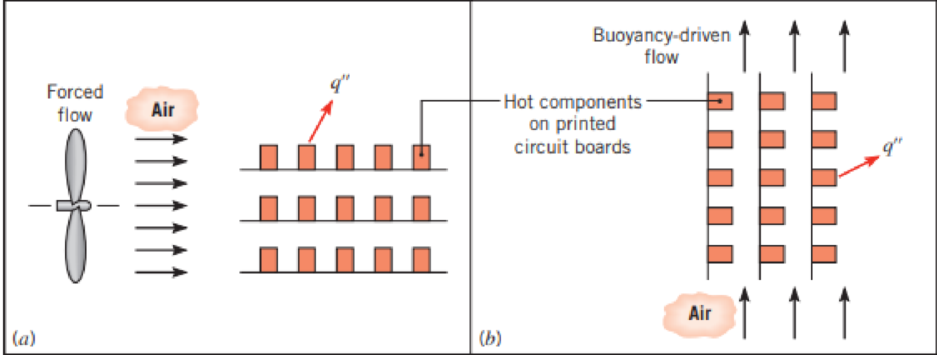


*Figure 4: Convection heat transfer processes: a) Forced convection. b) Natural convection* [ 13 ]

Heat transferred, for example from the wall to the fluid by convection is proportional to the temperature difference. So, the heat flux is then:

$$q_C = h_C(T_S - T_\infty) \quad (17)$$

where $q_C$ is the heat flux from the surface into the fluid $[\mathrm{W/m^2}]$, heat flux is proportional to the difference between the surface and surrounding fluid temperature ($T_S$ and $T_\infty$). Last part

of the equation is the *convective heat transfer coefficient* $h_\mathrm{C}\left[\frac{\mathrm{W}}{\mathrm{m}^2}\ \mathrm{K}\right]$. This equation is also often called Newton's law of cooling. But it is more like definition than true law.

Heat transfer can be than expressed as

$$\dot{Q}_\mathrm{C} = \bar{h}_\mathrm{C} A (T_\mathrm{S} - T_\infty) \tag{18}$$

Due to variation of $h_\mathrm{C}$ between laminar and turbulent flow, $\bar{h}_\mathrm{C}$ is used instead. $\bar{h}_\mathrm{C}$ is an average heat transfer coefficient for an isothermal surface of area $A$.

Relation between $h_\mathrm{C}$ and $\bar{h}_\mathrm{C}$ is defined as

$$\bar{h}_\mathrm{C} = \frac{1}{A}\int_0^A h_\mathrm{C}\,\mathrm{d}A \tag{19}$$

However, this is valid only for isothermal surfaces. In case that surface is not isothermal, defining an average heat transfer coefficient is more difficult. In general, high heat transfer coefficients $\bar{h}_\mathrm{C}$ are associated with high thermal conductivities, high flow velocities, and small surfaces [ 10 ], [ 11 ], [ 12 ], [ 13 ].

## 3.3. Radiation

The last of the modes is radiation. Thermal electromagnetic radiation is energy emitted by all matters which are at nonzero temperature. I will focus on solid surfaces, but radiation can be emitted either by liquids or gases. A particle of electromagnetic energy is a photon. Heat transfer can be viewed either in terms of electromagnetic waves or in terms of phonons. Instead of conduction and convection radiation heat transfer does not a need material medium through which energy travels. So, heat transfer is possible through a region in which a perfect vacuum exists.

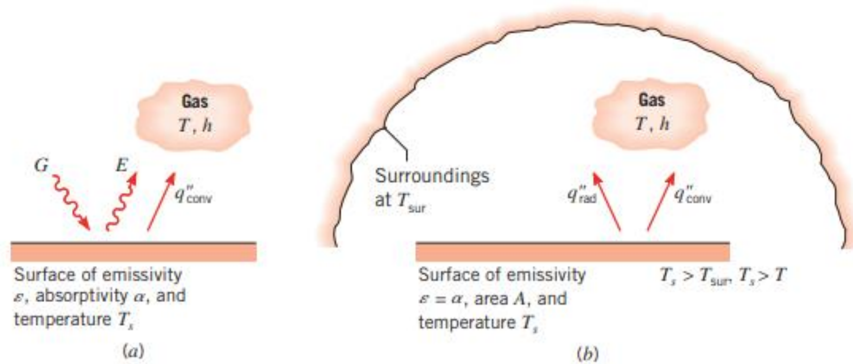


*Figure 5: Radiation exchange: a) at a surface, b) between surface and large surroundings* [ 13 ]

The radiation emitted by the surface originates from the thermal energy of the matter, and the rate at which energy is released per unit area is termed the surface emissive power $E_\mathrm{emis}\left[\frac{\mathrm{W}}{\mathrm{m}^2}\right]$. Emissive power is limited with Stefan-Boltzmann law:

$$E_\mathrm{b} = \sigma_\mathrm{const} T_\mathrm{S}^4 \tag{20}$$

where $T_s$ [K] is the absolute temperature of the surface and $\sigma_{\text{const}} = 5.67 \times 10^{-8} \left[\frac{\text{W}}{\text{m}^2}\text{K}^4\right]$ is the *Stefan-Boltzmann constant*. Such a surface is called a blackbody or ideal radiator. The blackbody is defined as a surface that absorbs all incidental radiation and reflects none. From the other perspective, the flux of radiant energy incidents on a surface it's its irradiation $G_{\text{irrad}} \left[\frac{\text{W}}{\text{m}^2}\right]$. Speaking about the blackbody, the radiation must be equal to irradiation.

But this is only idealization, the heat flux of real surfaces is less than the heat flux of a blackbody at the same temperature. So, the previous equation needs to be adjusted:

$$E = \epsilon \sigma_{\text{const}} T_s^4 \quad (21)$$

where $\epsilon$ is a radiative property of the surface called the *emissivity*. The emissivity values are in the range $0 \leq \epsilon \leq 1$ and so it is dimensionless. This property measures how efficiently the surface emits energy relative to a blackbody.

Surface can absorb a portion, or all, of the irradiation $G$. Absorbed irradiation increases the thermal energy of matter. The rate of absorbed energy per unit surface area may be evaluated thanks to the surface radiative property termed as an *absorptivity* $\alpha$:

$$G_{\text{abs}} = \alpha G \quad (22)$$

where $G_{\text{abs}}$ is absorbed irradiation. Absorptivity is defined in the range of $0 \leq \alpha \leq 1$. If $\alpha < 1$, portions of the irradiation $G$ are reflected, if $\alpha = 1$, all the irradiation is absorbed. So, absorptivity and emissivity affect the thermal energy of matter.

Radiation is affected by one more factor and that is that electromagnetic radiation travels in straight lines. This means that the amount of radiation that an object receives from a radiative heat source depends on the orientation. This factor is called the *point of view factor* (eventually configuration or orientation factor) $F$ and it is a function of the geometry of the configuration to be analyzed. In a situation when a real body exchanges radiant energy with only blackbody, the exchange is given by:

$$\dot{Q} = \sigma A_1 F_{1-2} \epsilon_1 (T_1^4 - T_2^4), \qquad F_{1-2} \leq 1 \quad (23)$$

where $1-2$ defines how is surface 2 viewed by surface 1. In more detail, this factor is defined as a fraction of total radiant energy that leaves surface 1 and arrives on surface 2 [ 10 ], [ 11 ], [ 12 ], [ 13 ].

### 3.4. Thermal gradient

Speaking about heat, heat flow, heat flux, etc., thermal gradient is a very important parameter. Temperature gradient means the difference in the heat energy of two bodies and decides the direction of the heat flow between the bodies when the system is enclosed and isolated. It describes temperature changes around the location. So, thermal gradient is a function of three-dimensional space:

$$T = T(x, y, z) \quad (24)$$

$$\nabla T = \left(\frac{\partial T}{\partial x}, \frac{\partial T}{\partial y}, \frac{\partial T}{\partial z}\right) \tag{25}$$

where temperature $T$ is a continuous and differentiable function, $x, y, z$ are coordinates of the location where we are investigating thermal gradient and $\nabla T$ is the vector of the thermal gradient itself. As was written above, thermal gradient can be viewed as an analogy to voltage in electronic circuits.

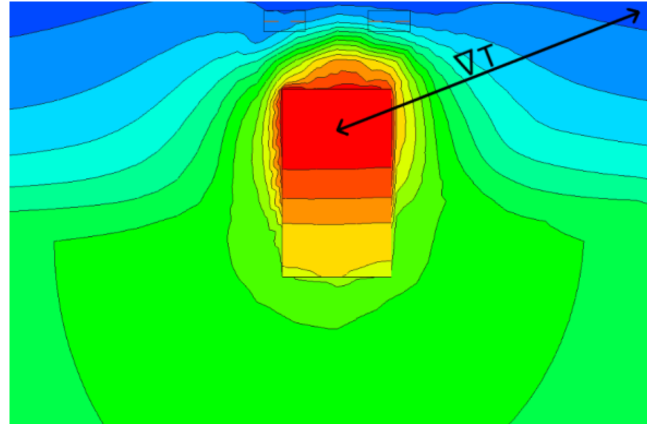


*Figure 6: Thermal gradient*

The temperature difference or gradient itself in systems is an important thing. During the design of electronics, it is important to take thermal gradients into consideration.

Each part can generate different heat. Does not matter if on die or PCB. This can be caused by many reasons (technology, materials,…). Also, surrounding conditions can influence the dissipation of the heat. This results in a temperature difference. So, the same components can have different characteristics because they are working in different temperatures. If the thermal gradient were high, differences would be also higher.

The high gradient in the system can cause trouble. For example, coupled transistors on the die need to work in the same conditions. Only then can be the right function guaranteed. So, thermal dissipation should be as uniform as possible or known in advance during the design phase. Then placement of the critical block can be optimized [ 5 ], [ 9 ], [ 14 ], [ 15 ].

# 4. Current sensors

A current sensor is a device that detects flowing current and converts it to output voltage which is easily measurable. The output voltage is proportional to the flowing current through the measured path. Current sensors play a critical role in modern power electronics systems and are necessary for purposes of protection and control. There is a wide variety of current sensors, and each one is suitable for specific applications (current range, ambient conditions, etc.). In industry and many other applications integrated current sensors are used [ 17 ], [ 18 ].

These types of chips aim to achieve the following characteristics:

- Compact size
- Compatibility with the manufacturing process
- High bandwidth
- High noise immunity
- High stability with varying module temperature
- High isolation

## 4.1. Shunt

The most cost-effective sensing elements are shunts. They have compact profiles suitable for DC or AC measurements. Even though shunts are suitable for AC applications, they are not suitable for applications of up to tens of MHz. Shunts must be inserted in the main current path and therefore decrease efficiency. Shunts CS applications are limited by the max common mode voltage of the operation amplifier. So, it is well suited for low voltage apps [ 18 ].

## 4.2. Current transformer

The current transformer is another possibility. Current transformers have been widely used for AC current sensing with a bandwidth of up to tens of MHz. It can also detect pulse currents of up to 5 kA with 20 ns rise time. Additional driving circuits are normally not necessary. Current transformers cannot measure DC current. Also, they are not cheap, but the technology is quite simple [ 18 ].

## 4.3. GMR current sensor

An interesting principle to measure current with integrated sensors is to use GMR sensors. Integrated GMR current sensors are based on the Giant Magneto Resistive effect. This means that electrical resistance changes with a magnetic field. GMR sensors are made of alternating thin layers of ferromagnetic and non-ferromagnetic materials. Each layer is only a few atomic layers thick. These sensors are usually etched into the Wheatstone bridge pattern to improve the sensitivity and to minimize temperature dependence. GMR current sensors are not so cheap, but they are able to measure current from DC values up to tens of GHz. But this technology is quite complicated. Advantages are low noise and high sensitivity [ 18 ].

## 4.4. Hall effect-based sensors

Another variant of current sensing is to use Hall effect technology which is part of the galvanomagnetic sensors relay on the Lorenz force. Because the current sensors used in this work are using the Hall effect, I will talk about them in more detail. Hall effect is a common measuring method. It is an isolated and non-intrusive device that can be applied to sense either DC or AC current up to hundreds of kHz. Also measured currents can be in the range of tens to hundreds of Amperes. Hall sensors can work over a wide temperature range and can provide repeatable measuring [ 18 ].

## 4.5. Hall effect

Hall effect relies on the Lorentz force which is acting on moving carriers. In contrast with GMR current sensors, where Lorentz force causes a change in the resistivity (magneto-resistive effect), here, the Hall effect generates a voltage drop orthogonal to the path of moving carriers.

The principle is to convert the magnetic field to Hall voltage. The external flowing current creates a magnetic field around the conductor in proportion to the current. in Figure 7 we can see a rectangular n-type semiconductor device with length $l$, width $w$ and thickness $t$. Current $I_{\mathrm{bias}}$ flows through the contacts $\mathrm{C}_1$ and $\mathrm{C}_2$. It is forced due to an external electric field $\mathbf{E}_{\mathrm{bias}}$. Due to Lorentz force, when an external magnetic field is applied to the Hall plate, Hall voltage $V_{\mathrm{H}}$ occurs between contacts $\mathrm{S}_1$ and $\mathrm{S}_2$. So, the magnetic field is converted on the Hall plate to the Hall voltage. Then this voltage can be measured relatively easily.

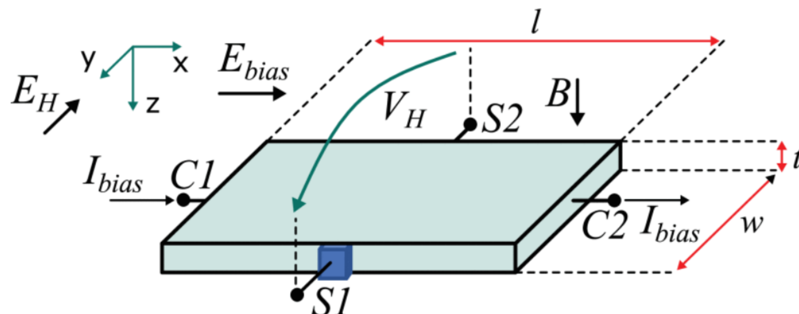


*Figure 7: Rectangular Hall plate explaining a generation of Hall voltage* [ 19 ]

Hall effect-based sensors have many advantages. Hall plate can be integrated into the chip. It is highly compatible with silicon technologies and can be easily integrated into CMOS technology or some alternative (better performance). The advantage is that measured current is not flowing directly through the die but through the lead frame placed close to the die and hall plates. This type of sensor has high accuracy. However, silicon-based Hall sensors (without the magnetic concentrators) have lower sensitivity with respect to the GMR. Resolution is usually limited by noise performance and depends on the type of sensor.

Hall effect-based sensors have serval limitations including quite low sensitivity, limited bandwidth, and temperature dispersion of the parameters. Yet their compact nature, low cost, good linearity and last but not least their ability to measure DC currents make them suitable for modern power applications [ 18 ], [ 19 ], [ 20 ].

## 4.6.Thermal issues of Hall effect-based sensors

As with everything, the Hall effect is affected by the temperature. From the previous paragraph is obvious that Hall plates are not heated directly because the measured current is not flowing through the plate. Integrated current sensors of this type usually use a lead frame to conduct measured current. Integrated circuits are small devices, which means that the conductors inside are not big either. Therefore, wires heat up quickly and to quite high temperatures. Especially when the flowing current is high.

As the measured currents can be up to hundreds of Amperes (depending on the package), power loss of the current loop of the lead frame can grow high. So, the lead frame is the main producer of the heat that spreads to the whole chip. But also, temperature affects the electrical resistance of the element, the mobility of major carriers, and the sensitivity of the sensor. This is usually compensated on a chip within the full operating range (usually -50 °C to 150 °C). A change of sensitivity with temperature is called temperature drift. This is also one of the problems why thermal management is important.

# 5. Integrated current sensor ACS37013

As I mentioned in the previous section, there is a wide variety of current sensors. However, in this work I will use a sensor of only one type, and this is a current sensor ACS37013 developed by the company Allegro MicroSystems [ 21 ]. Chip ACS37013 is a fully integrated Hall-effect-based current sensor. Its output is proportional to the input current flowing through the primary current loop. It is a bidirectional device with quite a wide range of measurable currents. ACS37013 uses two Hall plates to sense flowing current differentially. This solution provides subtraction of the external interfering common-mode magnetic fields.

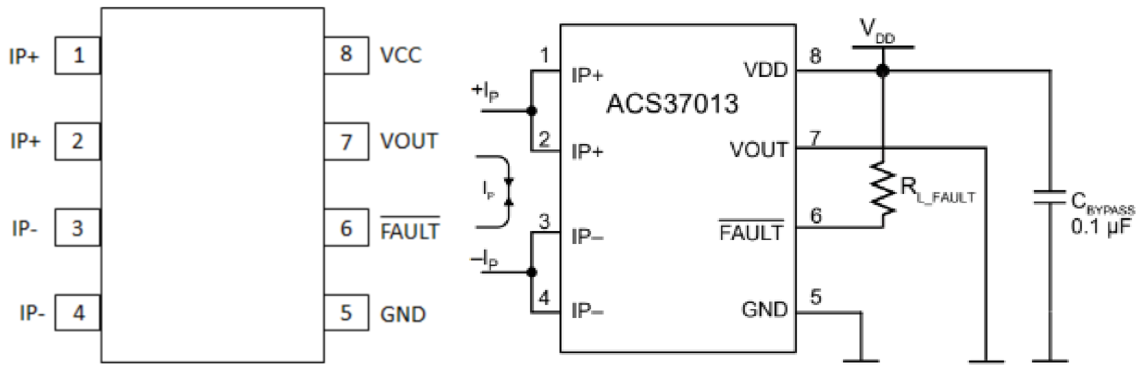


*Figure 8: Integrated current sensor ACS37013 with its typical application* [ 21 ]

This current sensor is integrated into the standard package SOIC-8. The lead frame is specifically designed for current sensing. Four terminals are for an input current being sensed (two pins IP+, two pins IP-). A part of the lead frame connected to those pins forms a sensing current loop. Two terminals are used for the power supply (VCC and GND). The rest of the terminals are output signals (VOUT and FAULT) [ 21 ].

## 5.1.Model of the ACS37013

The model of the integrated current sensor is one of the most important parts of the simulation. As I wrote in section 5, IC 37013 uses the SOIC-8 package which is quite common. This is an advantage because no custom footprints are needed. As this model does not aim to solve the electrical behavior of the circuits on the die, it is simplified as the black box made of silicon.

The lead frame of the chip is made of main 5 parts. The first is the current loop. It is more massive than other parts of the lead frame because it must take much higher current than other parts. The loop is shaped due to the sensing principle. Resistance of the loop is $0.9\ \mathrm{m\Omega}$ at room temperature. The other 4 parts of the lead frame connect the die with outside terminals (described in previous paragraphs).

The die is connected to the lead frame by the copper pillars. Those connecting pillars are soldered to the lead frame. All these parts are covered in epoxide [ 21 ].

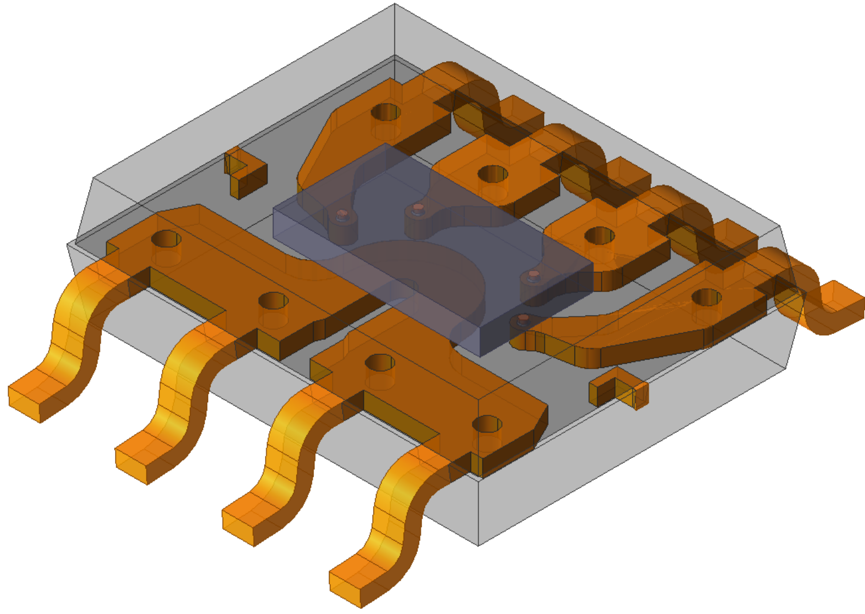

*Figure 9: Model of the integrated current sensor ACS37013*

# 6. Printed circuit board (PCB)

A printed circuit board is a device that is made of a non-conductive material and conductive lines are printed or etched. PCB can have conductive layers on one side, or two sides or it can be a multilayer structure. This means a sandwich structure made of many conducting layers each separated by insulating layers. Typical PCBs are made of glass-fiber composites. Traces (conductive paths) are usually made of copper, but a variety of materials may be used. PCBs are mostly flat and rigid but there are flexible substrates for special applications [ 22 ].

As I wrote in the sections above, modern semiconductor devices are shrinking to achieve better parameters such as higher power densities, lower parasitic inductances, etc. Therefore, power management plays a crucial role. The heat that is generated inside the semiconductors must be effectively dissipated. If not, high temperatures can cause a wide variety of issues. Here comes the importance of the design of the PCB.

To achieve an increase in power density and better heat dissipation it is necessary to design PCB properly. During heat transfer across the PCB and between the PCB and surrounding take place conduction, convection, and radiation. According to the PCB definition in the paragraph above, standard PCB is made of conductive and non-conductive materials. Thermal behavior is directly affected by the parameters of conductive material, mostly copper. Crucial is the number of the copper layers and their thickness. This mass then behaves as a heatsink for components. This means better heat dissipation. The total thickness of the PCB is important. This parameter is also influenced by the thickness of non-conductive materials, usually materialFR-4 [ 23 ], [ 24 ].

If the conducting layers of the PCB were not connected, heat dissipation and distribution would be difficult and inefficient. Thermal resistance between layers would be relatively high. So, important is the mechanism of connecting layers via plated through holes (PTHs), i.e., vias. Electro-thermal PTHs provide a thermal path to transfer heat from its source. Via layout is usually created in some pattern. These patterns can be uniform or non-uniform. A common pattern is a simple array of vias created through a multilayer structure of the PCB. If a via in pad is used, then filling and plating the via with copper and FR-4 epoxide is necessary. Another possibility is that vias are filled with conductive paste. Solder can provide better thermal conductivity. Vias placing is typically limited by via-to-via spacing, via diameter, or via plating thickness. Everything described in the paragraphs above can be seen in Figure 10 bellow [ 23 ], [ 24 ].

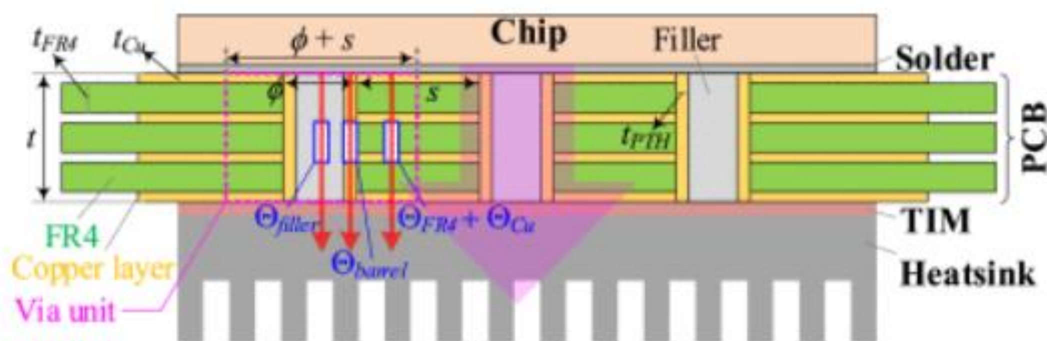


*Figure 10: Planar section of a four-layer PCB with heatsink* [ 23 ]

# 7. Simulations

The development of microelectronics brings new challenges. The effort is to create a long-term reliable and high-performance product. The reduction of the sizes hits the limitations of technology. This means higher demands on the junction temperatures, the density of power dissipation, etc. Also, technologies are forced to be operational in wide ranges of ambient temperatures. The operating temperature as well as the distribution of the temperature over the system is the issue. This issue cannot be totally avoided. This is why all simulations are necessary. Electro-thermo-mechanical simulations can prevent many issues e.g. overheating, degraded efficiency, or reduced lifetime. Simulations can predict device and/or circuit behavior before fabrication which reduces costs [ 25 ], [ 26 ], [ 27 ], [ 28 ], [ 29 ].

## 7.1. Electro-thermal simulations

Electro-thermal simulations can be split into three categories. The first category implements a thermal network in an electrical simulator, the second one implements an electrical behavior in a thermal solver and the last one is a two-way coupling between the electrical and thermal simulators. Two-way coupling is an effective way to get precise results because it is a combination of both categories mentioned before. A brief description of the 2-way coupling workflow of electro-thermal simulations can be seen in Figure 11 [ 26 ].

Electronic solvers are using the Finite Element Method (FEM). This means that the solver discretizes all objects of the model to the basic elements. This process is provided by meshing. These basic elements created by mesh are then simulated. The granularity of the mesh determines the accuracy and precision of the FEM simulator. Nonetheless, the denser the mesh is the longer time is needed to provide calculations. A denser mesh means more elements. Meshing can be done in 2D or 3D. 3D mesh elements are usually tetrahedra-shaped and 2D are usually triangle-shaped [ 30 ].

Thermal solvers usually use the Finite Volume Method (FVM). The principle is similar to FEM. The domain is discretized into a finite set of volumes. This process is also done by meshing. There are similar "issues" as with the FEM method. Mesh density determines accuracy, precision, and computational time. Computations are done numerically [ 31 ].

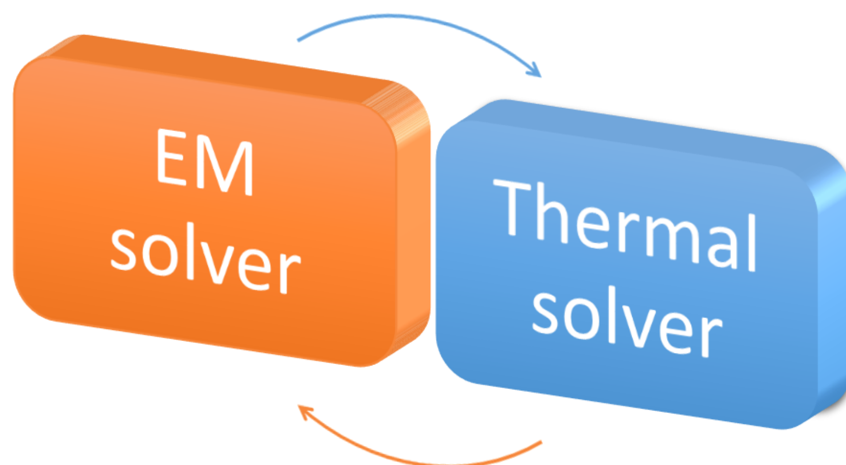


*Figure 11: Example flow chart of the 2-way coupling between electric solver and thermal solver*

## 7.2. Mechanical simulations

Following the previous paragraph, it is necessary to mention mechanical simulations as another type of simulations. These simulations are based on the mechanical properties of the materials. Speaking about electro-thermal-mechanical simulations, mechanical simulations relate to electro or thermal solvers in similar ways to electro-thermal simulations. This means that they are connected to electrical simulations or thermal simulations with coupling. The second solver has implemented information about electro or thermal behavior (depending on coupling).

Mechanical simulations are important because the behavior of the IC's materials can cause mechanical stress-related issues, such as reduced accuracy or even destruction. During switching or due to a long-time flowing current, the power dissipated by the device generates high junction temperatures. High temperatures cause thermal-induced stresses. Thermal stresses can cause differences in the behavior of the IC. In extreme cases, they can cause cracks in the metal lines, the delamination of the power metal from the substrate, or a crack of the dielectric between two metal lines which can cause short circuits [ 32 ], [ 33 ].

## 7.3. Ansys Electronics Desktop (AEDT)

One of the efficient tools to provide simulations described in previous paragraphs is a program from the Ansys company called Ansys Electronics Desktop (AEDT). AEDT is a multiphysics simulation software. This means that it enables users to design and simulate electromagnetic devices and perform thermal analysis and mechanical analysis. AEDT contains a variety of solvers focused on different problems. There are three electromagnetic solvers in AEDT: Maxwell, HFSS, and Q3D, which differ primarily in frequency range and in the aim of simulation. Thermal simulations are provided by Icepak solver. Mechanical simulations are provided by Mechanical solver [ 30 ], [ 31 ], [ 34 ], [ 35 ], [ 36 ].

## 7.4. Ansys SIwave

Ansys SIwave is another product from the Ansys company. SIwave is an EM field solver. SIwave is focused on simulations of PCBs and packages. Performed simulations are simulations of signal and power integrity (SI & PI analysis), electromagnetic compatibility, and DC analysis with thermal coupling. The last analysis does not differ much from the AEDT, because the DC simulation is coupled with an Icepak solver. The advantage of SIwave is the possibility of exportation of results directly to AEDT [ 37 ].

## 7.5. CST Studio Suite

Product CST Sudio Suit is an alternative to Ansys's products. Electromagnetic field solvers focus on applications across the EM spectrum. CST Studio Suite focuses on every aspect of electric simulations. Solvers can be coupled together to perform multiphysics simulations [ 38 ].

# 8. Die temperature measurement

Temperature sensing is an important aspect of the validation of the device. Simulations should be confirmed by precise laboratory measurements. Temperature control is necessary even during standard usage of the device. Temperature measuring can be done in many ways. A straightforward type of measuring temperature on the chip's die is by P-N junction.

## 8.1. Temperature measurement on P-N junction

P-N junction temperature sensors are semiconductor electronic devices that can be integrated into ICs. These sensors are able to measure a relatively large range of temperatures (approx. 55 °C to 150 °C). High performance, affordability, and ease of use make them popular in many solutions. The disadvantages are lower accuracy and slower response time. However, these sensors have a linear and easily measurable voltage output.

The semiconductor temperature sensors operate by measuring the voltage drop on the biased P-N junction, which is temperature-dependent. The energy gap between the valence and conduction changes with temperature. This phenomenon is affecting electrical conductivity. When the diode or the P-N junction is forward-biased, the voltage drop across the junction is directly proportional to the temperature. This allows the device to function as a temperature sensor. This type of sensor does not require the connection of complex circuits and can be implemented with diodes or transistors, which are more common on the chip. The model of the sensing circuit is in the Figure 12 [ 39 ], [ 40 ].

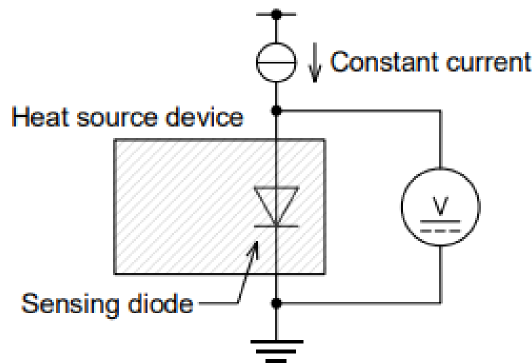


*Figure 12: Model of circuit for measuring voltage drop on the forward-biased diode* [ 40 ]

## 8.2. Theory about P-N junction temperature sensing and 2-current method

As was written in paragraphs above, this type of device uses P-N junction temperature-dependance to measure temperature. The basic equation for the diode or P-N junction is ( 26 ). This equation explains relations between the forward current, voltage drop and temperature.

$$I_{\mathrm{C}} = I_{\mathrm{S}}\left(e^{\frac{V_{\mathrm{BE}}}{(nV_T)}} - 1\right) \qquad (26)$$

Where $I_{\mathrm{C}}$ is the forward current, $I_{\mathrm{S}}$ is the reverse bias saturation current, $V_{\mathrm{BE}}$ is the forward voltage, $V_{\mathrm{T}}$ is the thermal voltage, $n$ is the ideality factor and $k_{\mathrm{const}}$ is Boltzmann's constant. $-1$ can be ignored if $V_{\mathrm{BE}} \gg \mathrm{V_T}$. Then the approximate model of $V_{\mathrm{BE}}$ is

$$V_{\mathrm{BE}} \approx n \cdot \frac{k_{\mathrm{const}} T}{q_{\mathrm{charge}}} \ln\left(\frac{I_{\mathrm{C}}}{I_{\mathrm{S}}}\right) \qquad (27)$$

Where $q_{\mathrm{charge}}$ is an elementary charge. Eq. ( 27 ) can be rewritten to temperature calculation as

$$T = q_{\mathrm{charge}} \cdot \frac{V_{\mathrm{BE}}}{nk_{\mathrm{const}} \cdot \ln\left(\frac{I_{\mathrm{C}}}{I_{\mathrm{S}}}\right)} \tag{28}$$

$k_{\mathrm{const}}, n$ and $I_{\mathrm{S}}$ are constants. The easiest way to measure temperature is to force current, measure voltage drop and calculate temperature. But this procedure's accuracy is dependent on constants $n$ and $I_{\mathrm{S}}$. These constants are process dependent and can vary a lot.

Therefore, two currents method is used. This method uses 2 different bias currents and diode voltage can be rewritten in delta form as

$$\Delta V_{\mathrm{BE}} = V_{\mathrm{BE1}} - V_{\mathrm{BE2}} = \frac{nk_{\mathrm{const}}T}{q_{\mathrm{charge}}} \ln\left(\frac{I_{\mathrm{C1}}}{I_{\mathrm{C2}}}\right) \tag{29}$$

Rewriting this equation to temperature calculation

$$T = \frac{V_{BE1} - V_{BE2}}{\frac{nk_{\mathrm{const}}}{q} \ln\left(\frac{I_{\mathrm{C1}}}{I_{\mathrm{C2}}}\right)} \tag{30}$$

With this equation there is no more temperature dependence on the $I_S$. Measured voltage can be also affected by the series resistances $R_{\mathrm{S}}$. This impedance is quite small. It is possible to get rid of this dependence by using the three currents method. It is necessary to measure the voltage with a small error to obtain accurate results [ 41 ], [ 42 ].

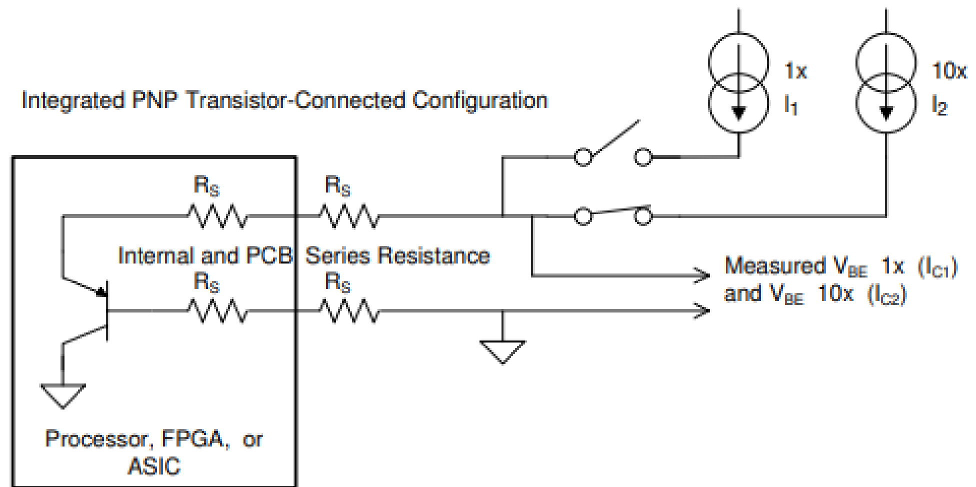


*Figure 13: Two currents method* [ 42 ]

# 9. Thermal distribution upgrades

Upgrades in thermal dissipation are needed because miniaturization and integration increase the heat flux tremendously. This brought challenges in thermal management. Especially with high-performance devices. However, heat distribution is important for all devices [ 44 ].

The first upgrade, and historically most used, is a basic heat sink. Heat sinks are usually made of aluminum because of its material properties. But as the power dissipation increased, needed heat sink sizes (volumes) increased either. On the other hand, a heat sink in combination with the Thermal Interface Material (TIM) is quite straightforward and cheap way to cool any device (Figure 14). A basic heat sink can be upgraded with liquid cooling or a fan which changes the natural convection to forced convection.

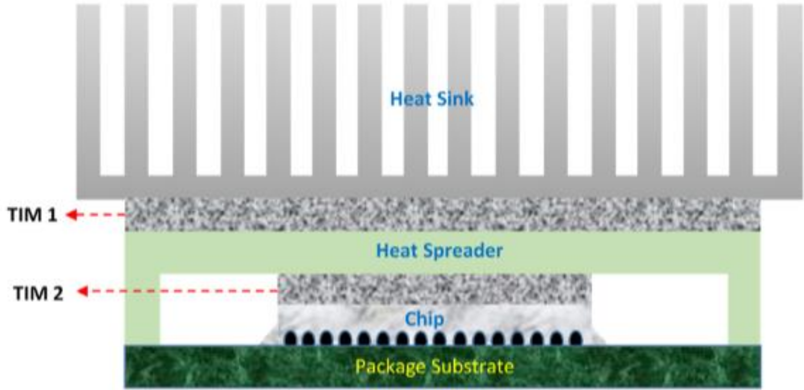


*Figure 14: A Typical structure of the TIMs used in microelectronic packaging* [ 45 ]

Heat sinks can be created as a structure inside of the chip. This process eliminates the need for the TIMs. This solution requires leak-tight fluid interconnects from the system fluid loop to the silicon chip. The microchannels that allow better heat flow can be fabricated using micromachining, molding, or embossing in a variety of materials (silicon, glass, metals, carbon, or polymers). Used material plays an important role in determining final thermal resistance. Visible in Figure 15.

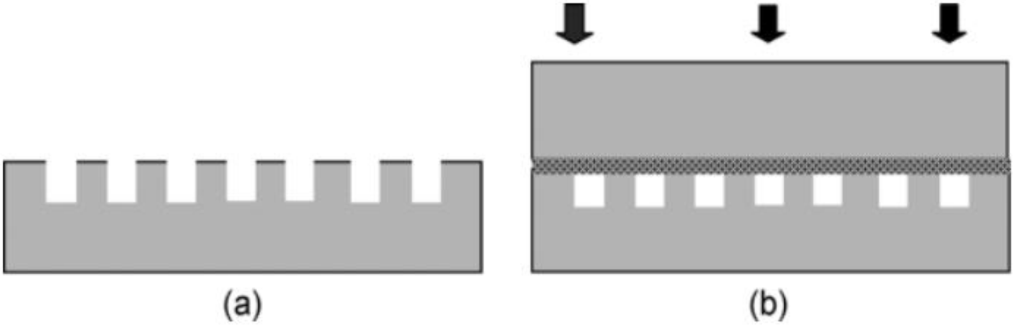


*Figure 15: Illustration of the formation of the microchannels by the glue bonding of a glass cover plate* [ 46 ]

Not only devices using cooling microchannels, but also other chips can benefit from the well-chosen package. The better the device is tight to the PCB the better the heat flow and cooling. That is why flip chips are a good choice. In combination with the possibility mentioned above, flip chips can provide an efficient interconnection of the microchannels on the die and the through holes on the PCB. Such a solution provides effective heat dissipation, although implementation of this system is not the simplest [ 43 ], [ 45 ], [ 46 ].

# 10. First assumptions

The idea of the whole project is something like this. Use the model of a package and a PCB and in the relevant tool proceed with a necessary simulation to explore the thermal gradient on the silicon die of the chip. Explore also heat dissipation on the other parts. Then do the laboratory measuring of the same real system and compare the results. When the results of the measuring differ from the simulation, upgrade the simulation in a way where the results will be as close to each other as possible. If everything works great, there is a possibility to try to create some thermo-mechanical simulations to observe the behavior of the package.

The assumptions for the simulation and for the setup are:

- DC load current $I_{\mathrm{LOAD}} = 50\ \mathrm{A}$
- Cables connected (1 m long, cross-section 70 $mm^2$, material - copper)
- Full PCB modeling, no layout simplifications
- Via metallization 25 um
- Exact lead frame modeling
- Natural convection + radiation
- Steady-state simulation
- Ambient temperature 25 °C
- Two-way coupling

As I wrote in the passage about simulations, when electro-thermal simulations are solved, it is necessary to calculate losses in all parts of the system. These losses are then transferred to the thermal solver which calculates heat losses in copper or some other conductors or semiconductors. I decided to use a solution that combines many of Ansys's tools. In the first line, the model of the PCB is solved in the Ansys SIwave tool. The solution is then inserted in the Ansys Icepak, which is a thermal solver. The next important part is the chip itself. According to section 7.3, this software contains 3 different electrical solvers. As I am interested in the DC solution, the Maxwell tool is a good option. Then all parts should be connected to one system. After this, it is possible to determine the total losses of all parts and use them as input for thermal solutions. Thereafter thermal calculations can be obtained.

The second possibility of simulation with the Ansys tools which I tried is to use different inputs of the PCB model. This means not to use Ansys SIwave but only Ansys AEDT. A STEP model of the PCB can be directly imported into the Maxwell tool. An advantage and a disadvantage of this solution is that the STEP model is very detailed. A large amount of detail could cause simulation problems even though it should bring more precise results.

The next step is to simulate another PCB and compare the results with the first one. Each should show different results. Then it is necessary to confirm the simulations with the real measurements.

The device on the PCB is then analyzed in the mechanical solver to observe the mechanical deformation due to the rising temperature in the package.

After the confirmation of the models and mechanical simulations, I created a proposal for the package upgrades to achieve better thermal results.

# 11. The first steps in the Ansys

## 11.1. Model of the PCB TED-0004110 in the SIwave

The model of the printed circuit board is imported in the format of .edb and it is shown in Figure 16. This PCB is made of 6 layers, and it is used as a testing board. Chip is placed in the middle. On one side (let's say it is the bottom side from the top view) are placed current loop pads. This is the place where the supply wires are connected. The copper of the loop is placed in all layers, which are connected by vias. On the other side (let's say the top side from the top view) there are placed communication pins such as the Vcc pin, which connects supply voltage to the chip, Vout pin, and Vfault pin. Also, there is a GND potential. The model contains information about placed capacitors, resistors, and some pin headers.

After importing the model, I had to update some settings. The materials were set correctly but the thickness of copper in the top and bottom layers was not right. Due to the manufacturing process is the thickness higher than the layers in the middle. Therefore, I increased it from 0.07 mm to 0.095 mm. After this PCB model was ready for simulation.

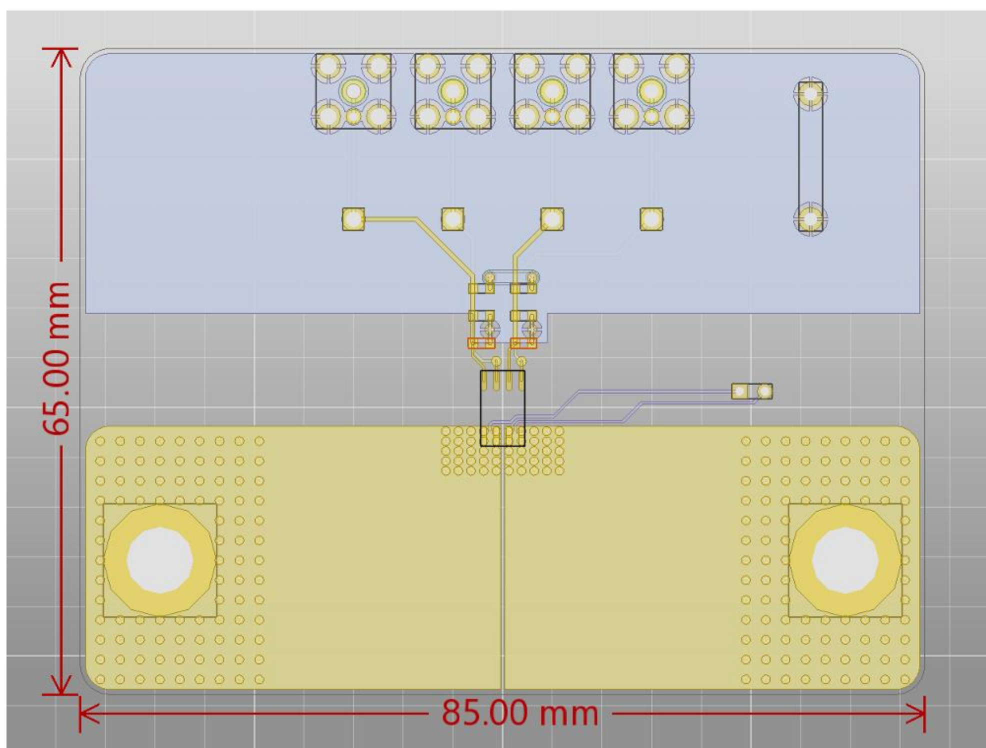


*Figure 16: Model of the PCB TED-0004110*

The first simulations in the SIwave tool were set like this: between connecting pads was set voltage of 1 V. The current was set by a current source. This setup allows the user to set the value and the direction of the current between the two points. The package of chips that I use in this work uses the SOIC-8 case. Therefore, it is obvious that the lead frame IP loop has 4 pins, 2 input pins, and 2 output pins. That's why I chose to set 2 current sources, each 25 A. In this simulation is no exact model of the package. But the .edb file contains information about the chip, at least its position on the PCB. So, SIwave creates a black box in the same place.

The advantage of the Ansys SIwave is that it can create a 2-way coupling between the SIwave solver and Icepak solver. This means that losses are computed in SIwave due to set DC current. These losses are then put to the Icepak solver which calculates heating and temperature distribution caused by the losses. As the setting of the simulation is 2-way coupling, results from Icepak are put back to the SIwave solver. Initial conditions are now different from the first solution. The solver does another calculation and the whole process repeats itself as many times as set (mostly 2 or 3 times). An important setting here is that Icepak should solve natural convection.

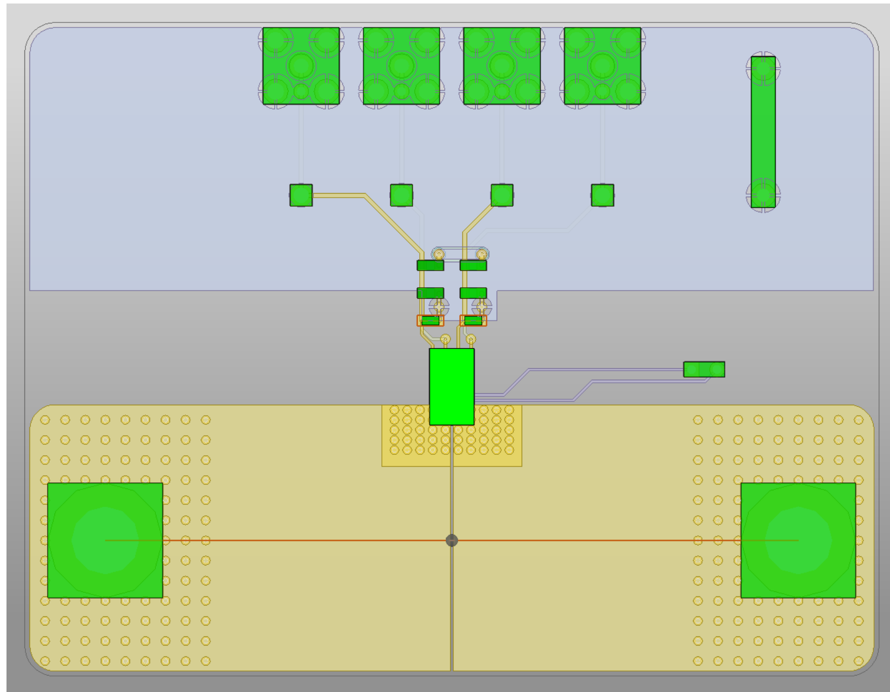

*Figure 17: Model of the TED-0004110 PCB prepared for the DC simulation*

## 11.2. Results from the SIwave simulations

The 2-way coupling brings both EM solver and thermal results. A useful thing about this type of simulation in the SIwave is that no special setting of mesh is needed. Meshing uses an adaptive solution. This means that mesh is automatically denser in important spots and coarser in less important places to save computing memory and reduce computing time. Visible in the picture Figure 18 below.

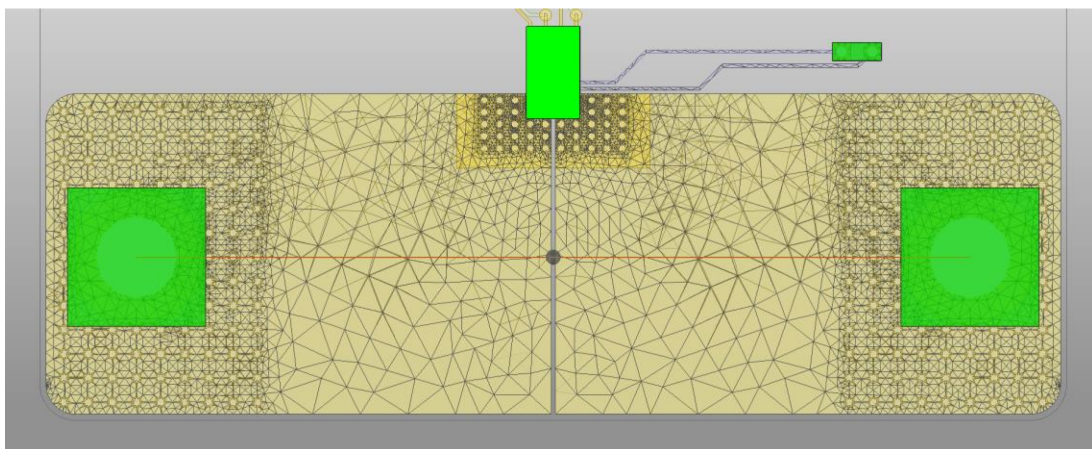

*Figure 18: Graph of the mesh of the IP loop from SIwave*

The main thing that is calculated by *DC IR Drop* simulation is the losses. Losses are not the only thing that is calculated and visualized. SIwave computes also current density $J$, power density $P$ and visualizes via current $I_{\mathrm{v}}$ value and direction. These values are visualized in the form of surface graphs at the points of interest. Graphical visualization gives a much better idea of what is happening than just numbers and it can be seen in Figure 19 and Figure 20. However, total losses in the PCB equal $P_{\mathrm{solid}} = 0.83\ \mathrm{W}$.

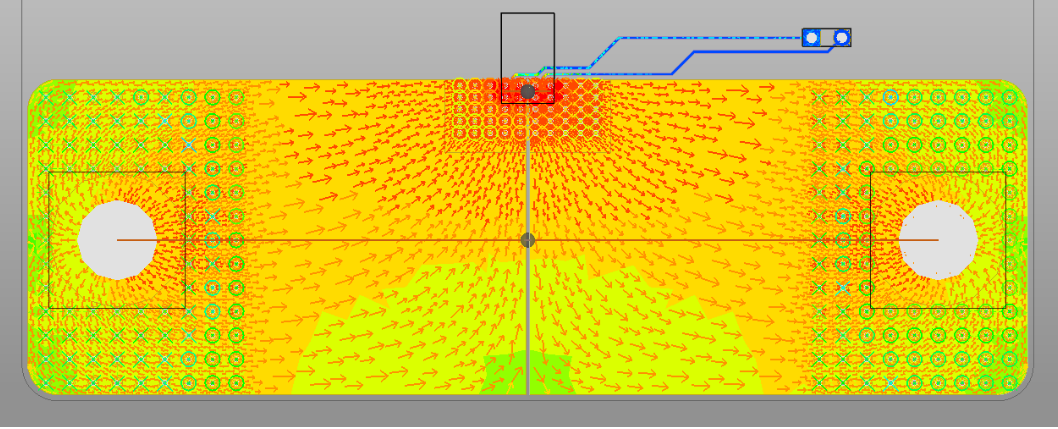

*Figure 19: First iteration of the coupling. Arrows represents current density J, X and O represents via currents Iv and background colors represents power P, Psolid = 0.74* W

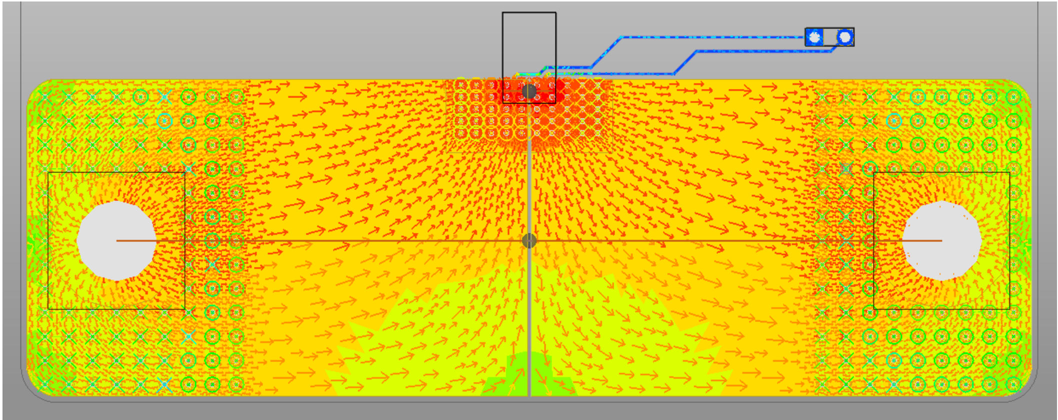

*Figure 20: Second iteration of the coupling. Arrows represents current density J, X and O represents via currents Iv and background colors represents power P, Psolid = 0.83* W

SIwave includes feedback data from the Icepak so it is able to plot temperature distribution in quite a good way. However, the quality of thermal graphs from SIwave is far away from the ones created in the Icepak. So, this is only an informative visualization to observe if the distribution looks as expected. The results of the temperature visualization are visible in Figure 21. The legend is visible inside the plot.

A little conclusion of the usage of the SIwave tool. I got useful results that gave me a better understanding of what was going on at the PCB. Also, as I wrote, SIwave provides the possibility of exporting a model of simulated parts directly to the Ansys AEDT, especially to the Icepak tool. This is an important part because AEDT abounds in greater versatility. This means the possibility of creating and simulating not only the PCB but also the whole system.

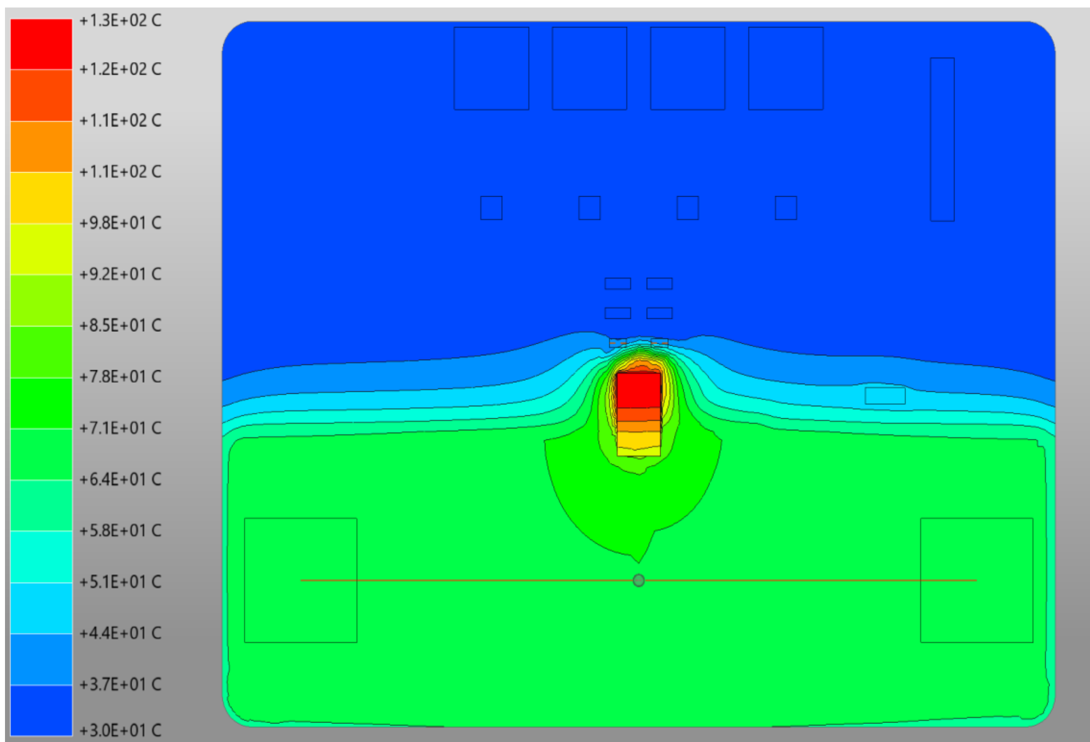


*Figure 21: Graph of the temperature distribution from the SIwave*

# 12. Ansys Maxwell tool simulations of PCB TED- 0004110

As was described in sections 7.3 and 10, the Maxwell tool is suitable for solving DC circuit problems. Except for the PCB, which is solved in the SIwave and then exported into a HFSS format, all the other components will be solved in the Maxwell. Two necessary components are the wires and the model of the real package described in section 5.1.

## 12.1. Model of the supply wires

Even though it may seem that supply wires do not have to be important for the simulation, the opposite is true. According to section 10, those power lines are both 1 meter long with a cross-section of 70 mm$^2$. This means that the mass of the copper should work as the heatsink for the PCB. The model of the wires reflects real power lines used in the real measure setup. Wires are isolated and terminated with a ring terminal. The model is visualized in Figure 22, Figure 23, and Figure 24. Nonetheless, the properties of the copper are supplemented by the dependence of the electrical conductivity on the temperature. This is important for the 2-way coupling in future thermal simulations.

*Figure 22: Model of the supply wires*

*Figure 23: Model of the supply wires, detailed top view*

*Figure 24: Model of the supply wires, detailed side view*

The load current is set to 50 A DC. Wires, the PCB, and the chip are connected in series. The current path is set via excitations of the faces. This can be seen in Figure 25. This visualization shows the setting of the input current, the second excitation is set on the face that will be connected to the PCB. The direction is opposite because the current here flows out of the wire. The second wire is set similarly to the previous description, but the directions are opposite.

To achieve better mesh and consequently more precise results, the maximal length of the mesh cells is set to 3.5 mm, which results in sufficiently dense mesh.

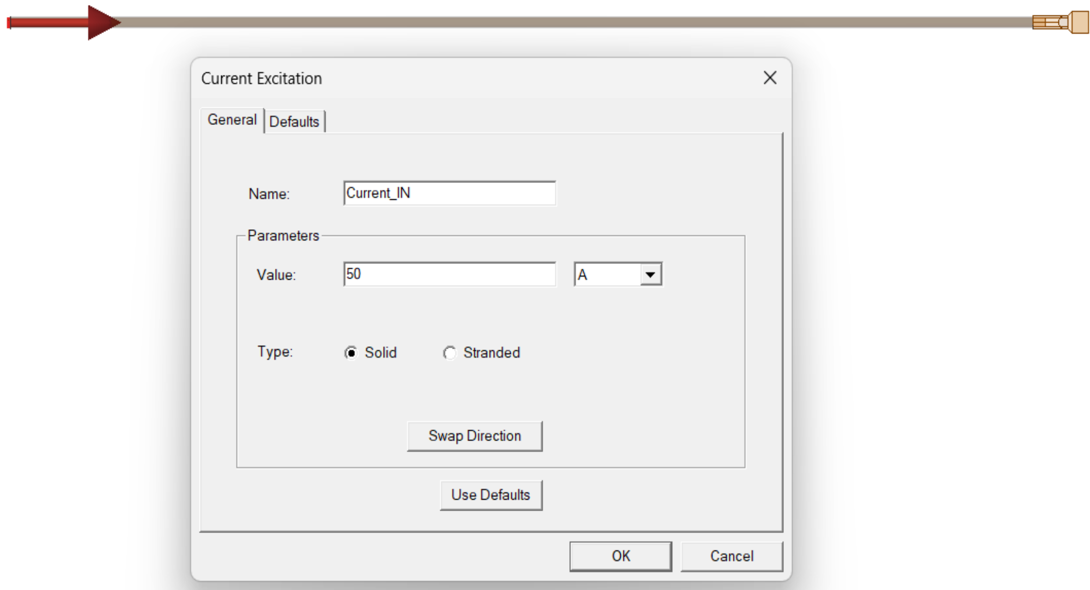


*Figure 25: Setting of the current path*

### 12.1.1. Wires simulation results – Current density $\boldsymbol{J}$

It is meaningless to show a graph of the whole size of the model of the wires. Current density is here uniform, changes are visible only on the ring terminals which are shown in Figure 26 and Figure 27. The maximal simulated current density $J_{\mathrm{MAX}}$ is $3 \times 10^6\ \mathrm{A/m^2}$.

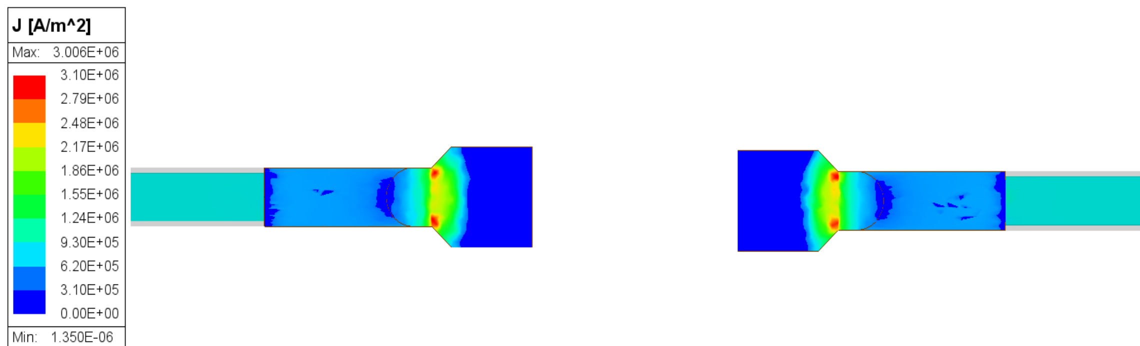


*Figure 26: Current density in the wires, top view*

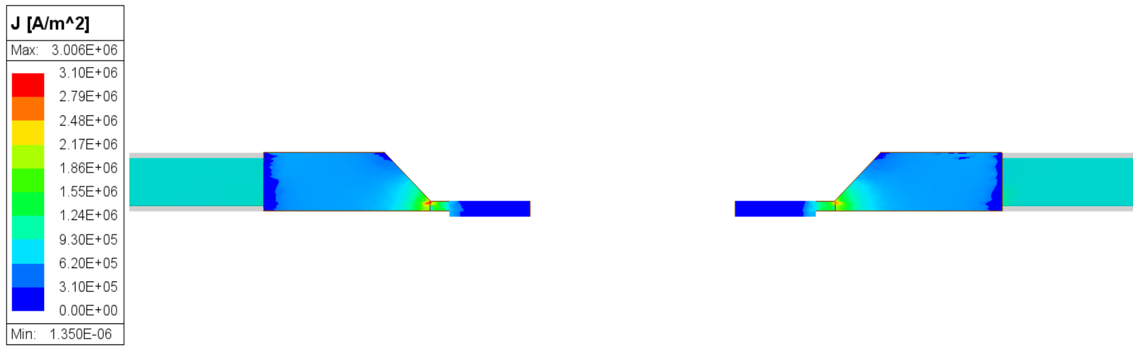


*Figure 27: Current density in the wires, side view*

### 12.1.2. Wires simulation results – Ohmic losses

The situation about results here is the same as in the previous section. Ohmic loss is only noticeable on the ring terminals. This is visible in Figure 28 and Figure 29. The maximal ohmic loss $P_{\mathrm{MAX}}$ on the visualization is $1.82 \times 10^5\ \mathrm{W/m^3}$. Total calculated losses of the solid $P_{\mathrm{solid}} = 1.33\ \mathrm{W}$.

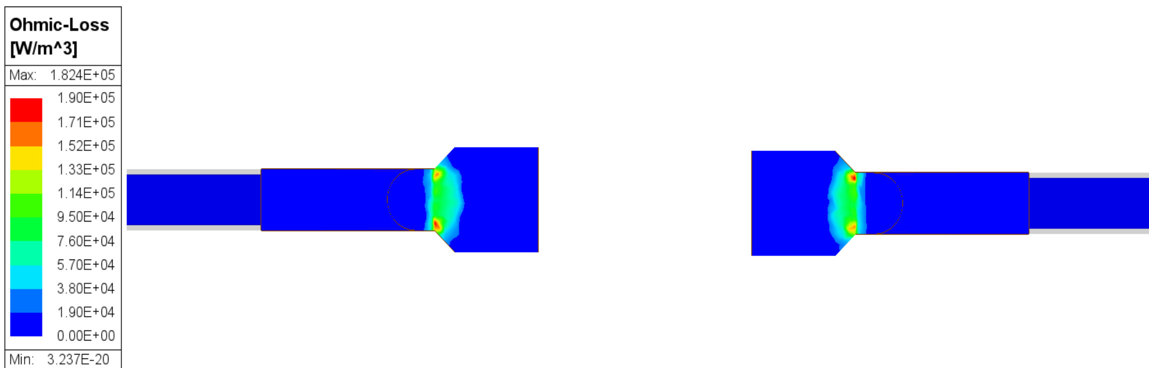


*Figure 28: Ohmic loss in the wires, top view*

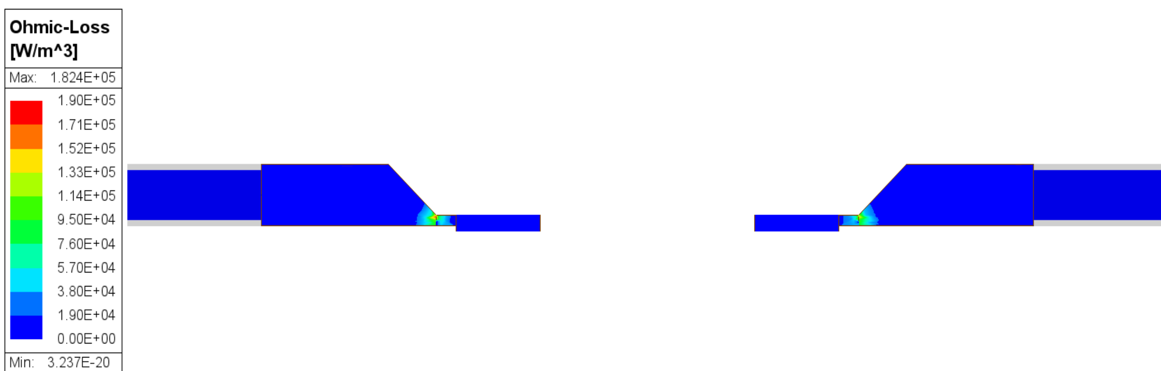


*Figure 29: Ohmic loss in the wires, top view*

## 12.2. Model of the ACS37013

The model of the chip was described in section 5.1 and is visible in Figure 9. The point of interest here is the primary current loop. This is where the heat is generated and from where the chip and the whole system are heated up. The biasing current is set to 50 A and the resistance of the lead frame is around $0.9\ \mathrm{m\Omega}$. According to that information expected power should be around 2.25 W at room temperature.

### 12.2.1. ACS37013 simulation results – Current density $\boldsymbol{J}$

Visualization of the current density here is important information. As can be seen in Figure 30, the $J$ is not uniform. As expected, density is higher on the terminals. But as the current flows the path of the least resistance, the highest density can be seen in the middle of the loop. Exactly only on one side of the loop. This is the place where the highest losses are then expected and where should be the highest temperature. The maximal simulated current density $J_{\mathrm{MAX}}$ is $1.11\ \times\ 10^{9}\ \mathrm{A/\ m^{2}}$.

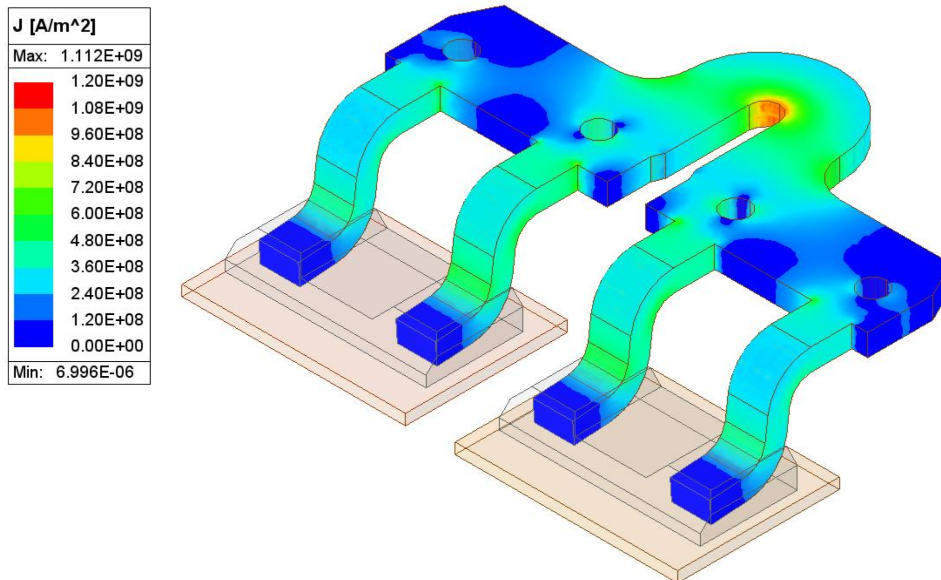


*Figure 30: Current density of the current loop*

### 12.2.2. ACS37013 simulation results – Ohmic loss

The ohmic loss reflects the results of the current density. As described in the previous paragraph, the density is highest in the middle of the loop. The highest ohmic loss occurs in the same place. Except in the middle of the loop, higher losses occur in the corners. This also reflects higher current density in those places. All these results are visible in Figure 31. Maximal ohmic loss $P_{\mathrm{MAX}}$ on the visualization is $2.24 \times 10^{10}\ \mathrm{W/m^{3}}$. Total calculated losses of the solid $P_{\mathrm{solid}}$ equal 2.12 W.

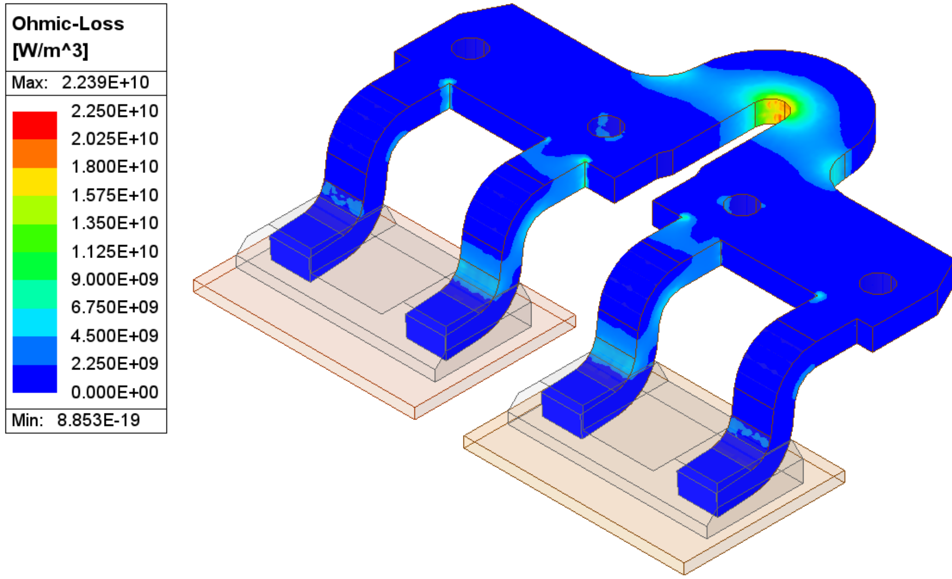


*Figure 31: Ohmic loss in the current loop*

# 13. Ansys Icepak simulations of PCB TED-0004110

Ansys Icepak, the thermal solver, was briefly described in section 7.3. The principle of the thermal solvers was described in section 7.1. In the GUI of the Icepak is the whole system connected together. All the losses described in previous sections are imported inside the Icepak and thermal calculations are made. Some materials are supplemented with a thermal modifier described in 2.1. Those materials are temperature-dependent. More precisely, the bulk conductivity of those materials is temperature-dependent.

## 13.1. Simulation setup

As described, the setup is made of the PCB model, package model, and model of the wires. The surroundings of the model are filled with air. It is the same as by real measurement. Boundaries are set as openings. This is an approximation that the boundary is not a wall, but air can flow through it. The temperature of the boundaries is set as an ambient temperature, which means 25 °C. Radiation is set to the same temperature. The simulation also uses 2-way coupling.

*Figure 32: Model of the whole system in the Icepak tool*

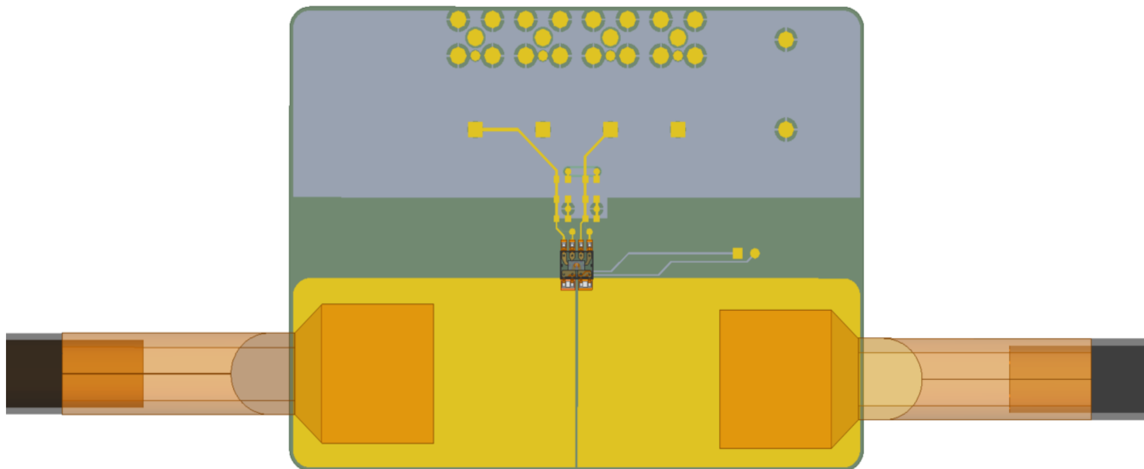

*Figure 33: Detailed model of the whole system in the Icepak tool*

## 13.2. Meshing

Because the parts of the models differ significantly in size, it is not possible to mesh everything together all at once. Serval parts need to be meshed separately. This allows to set mesh denser by more important parts and coarser by the others. The main heat generator is the current loop in the package. Heat will spread from here to the surroundings, which are the PCB and the air. According to section 3.2, heat dissipated in the air will cause movement of the fluid upwards. This is why it is important to correctly mesh surroundings where the movement is assumed.

The strategy of the meshing is to set the densest mesh in the close vicinity of the heat source and make it coarser with increasing distance. These settings should ensure the correct calculation of the heat transfer to the surroundings of the source. The mesh cell's size should be at least as big as the smallest part of the meshed block. Meshing sections are visible in Figure 34 and Figure 35. The densest mesh is in the closest vicinity of the package and around the PCB.

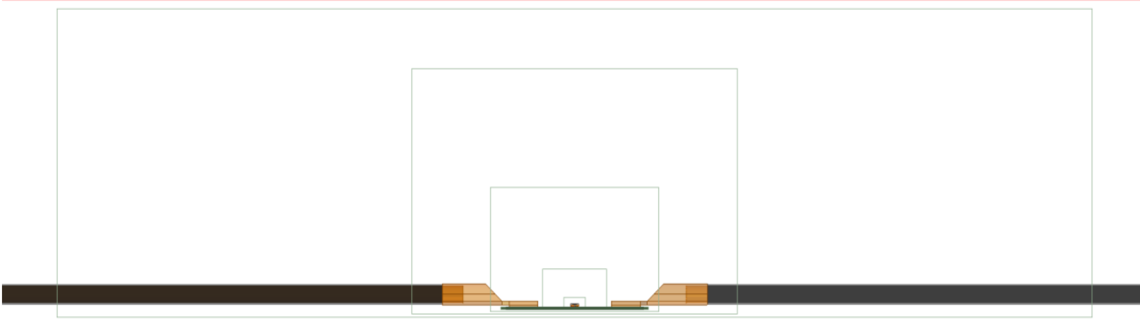

*Figure 34: Cutout of the meshing sections, side view*

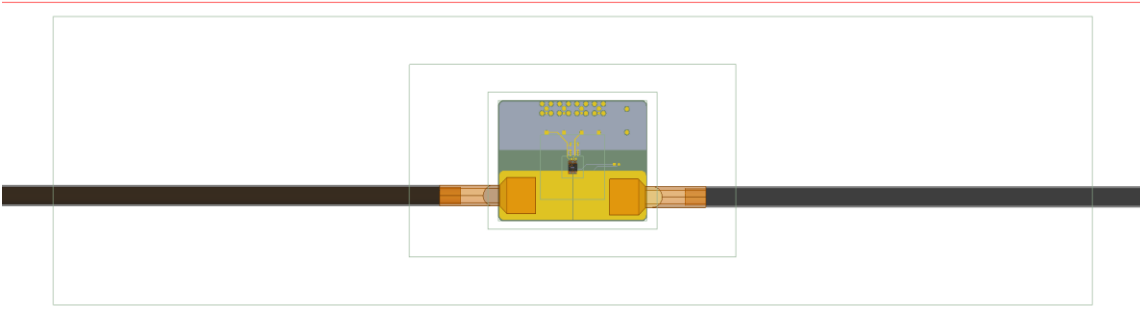

*Figure 35: Cutout of the meshing sections, top view*

In Figure 36 is visible mesh in the cut plane. It is visible that the mesh farther from the center has approx. 2.5 times more cells. This setting of mesh should ensure the best solution. The total number of meshed cells is over 18 million. This is actually a really huge number, and the solution cannot be computed on an average-quality PC. Therefore, the simulation is computed on the server.

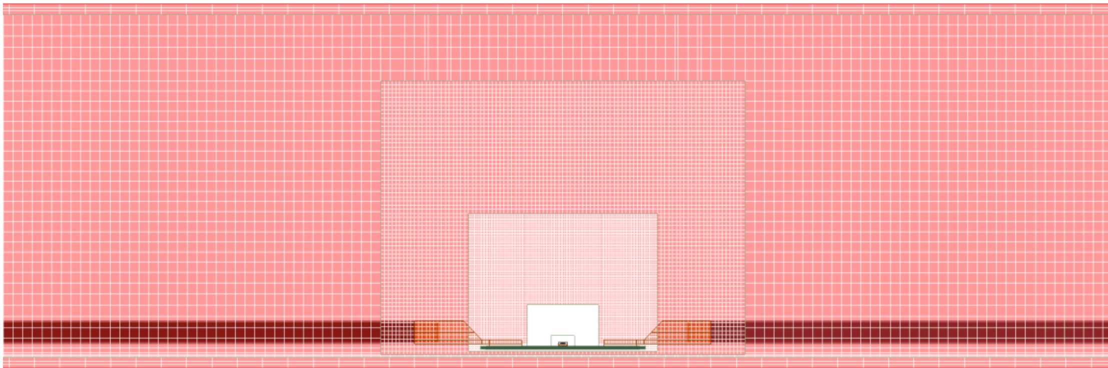

*Figure 36: Mesh visualization in cut plane in X axis, white color in the middle shows the densest mesh*

## 13.3. Results

The simulation ended after 3 successful passes. This means 3 calculations of the 2-way coupling. Each temperature calculation takes a maximum of 70 iterations. This setting ensures that each pass will converge successfully. Three passes are enough for temperature stabilization. Also, due to the really good quality of meshing less than 70 iterations per coupling were needed.

Crucial results are shown in the next subsections. The main point of interest is the chip's die. Temperature distribution over the system and total temperature gradient over the die is the main goal. Also, other temperature dissipations are important.

### 13.3.1. Temperature gradient over the die

The next Figure 37 zooms in the location of the die in the chip ACS37013. Therefore, the next figures, where the results are shown should be more understandable.

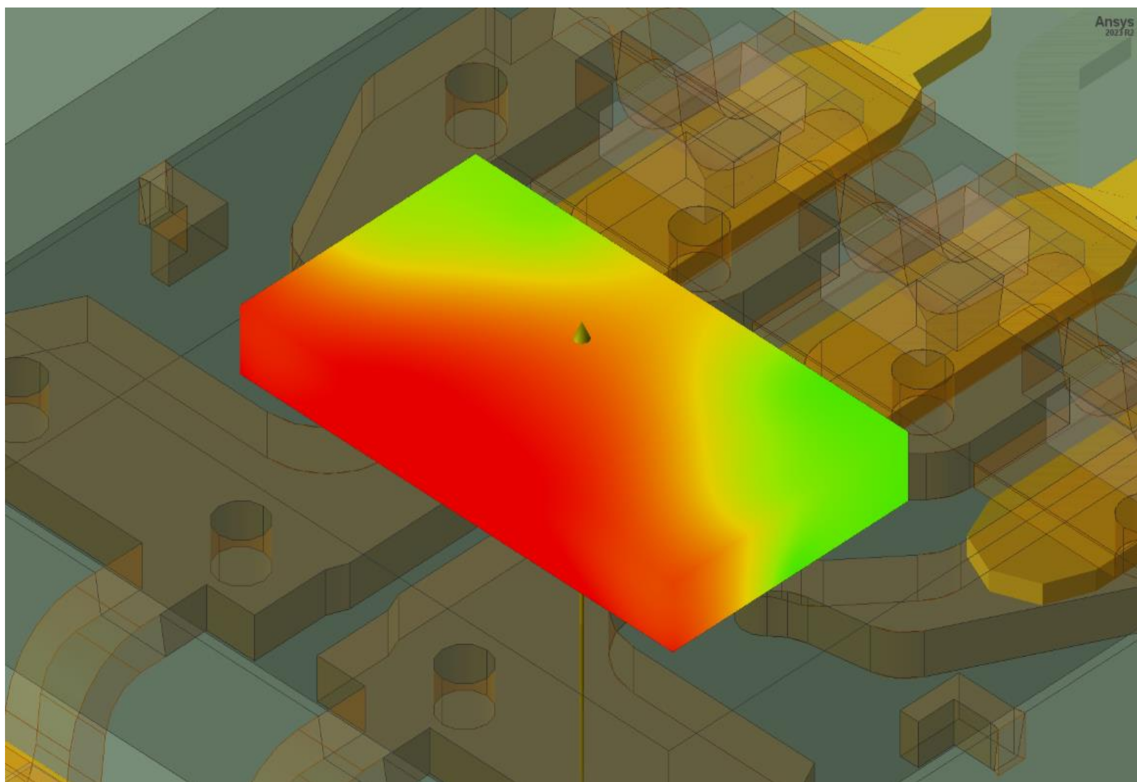


*Figure 37: A detailed view of the die in the chip and an illustrative temperature map of the temperature gradient*

The figures below show the temperature distribution on the chips die. The temperature gradient is easily visible. As can be seen, the highest temperature copies the shape of the primary current loop. The highest calculated temperature on the surface is $\boldsymbol{T_{\mathrm{MAX}} = 78.2\ °\mathrm{C}}$. The lowest temperature on the surface equals $\boldsymbol{T_{\mathrm{MIN}} = 74.1\ °\mathrm{C}}$. The lowest temperature is visible in the bottom view of the die in Figure 39. The four coldest points are places where the copper pillars connect pins on the die with the lead frame.

Due to this observation, the total temperature gradient over the die equals $\boldsymbol{\Delta T_{\mathrm{visualization}} = 4.1\ °\mathrm{C}}$.

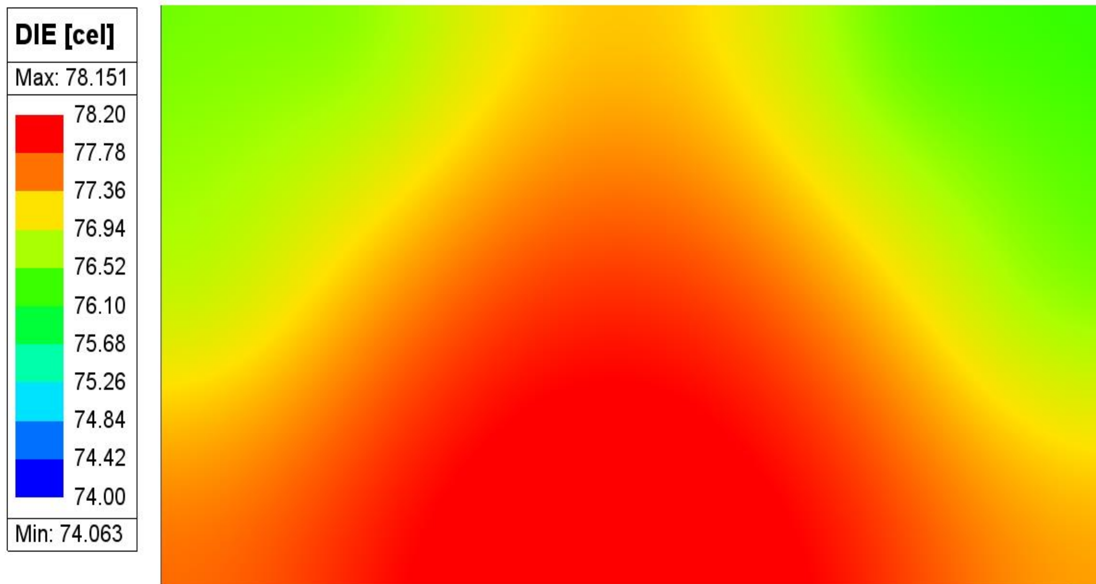


*Figure 38: Temperature distribution over the die, top view*

The point monitors (**see Figure 61**) are placed during the simulation on the same spots, where the measuring diodes lay on the real chip and are measured (**see Chapter 16**). Therefore, it is possible to determine the thermal gradient between those places. These results are visible in Table 1. The lowest temperature is on the thermometer number 5 and the highest is on the number 0. The total temperature gradient between the spots where measuring diodes lay equals $\boldsymbol{\Delta T_{\mathrm{monitors}} = 1.8\,^{\circ}\mathrm{C}}$.

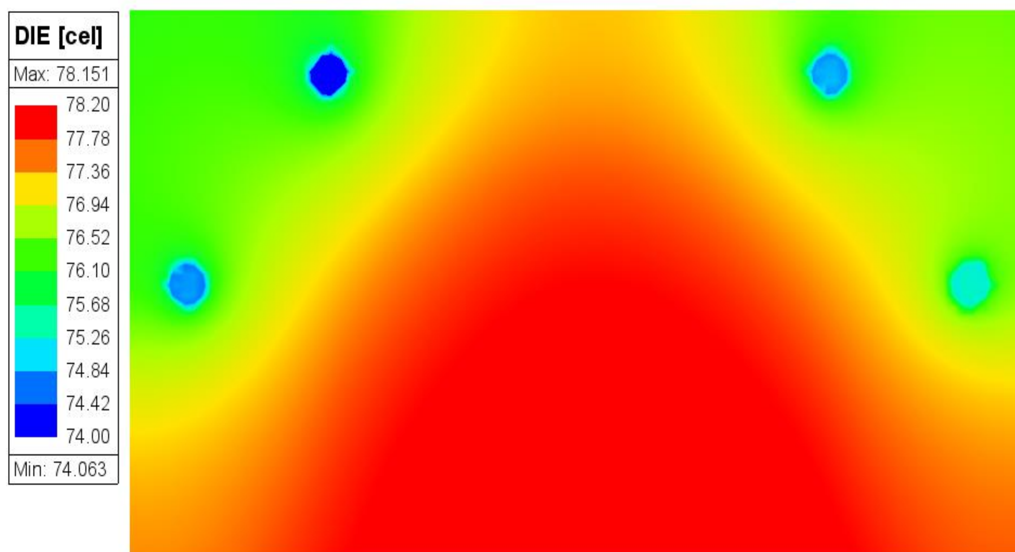


*Figure 39: Temperature distribution over the die, bottom view*

Table 1: Temperature on the measuring diode, TED-0004110

| Name | Temperature [°C] |
|---|---|
| Diode_0 | 78.0 |
| Diode_2 | 77.7 |
| Diode_6 | 77.4 |
| Diode_1 | 77.2 |
| Diode_4 | 76.7 |
| Diode_3 | 76.6 |
| Diode_5 | 76.2 |

### 13.3.2. Temperature distribution in the package

Temperature distribution in the package reflects dissipation in the surroundings. The highest temperature in the package is, not surprisingly, on the current loop. The maximal visualized temperature on the loop equals $T_{\text{loop}-\text{MAX}} = 90.3$ °C and this can be seen in Figure 40.

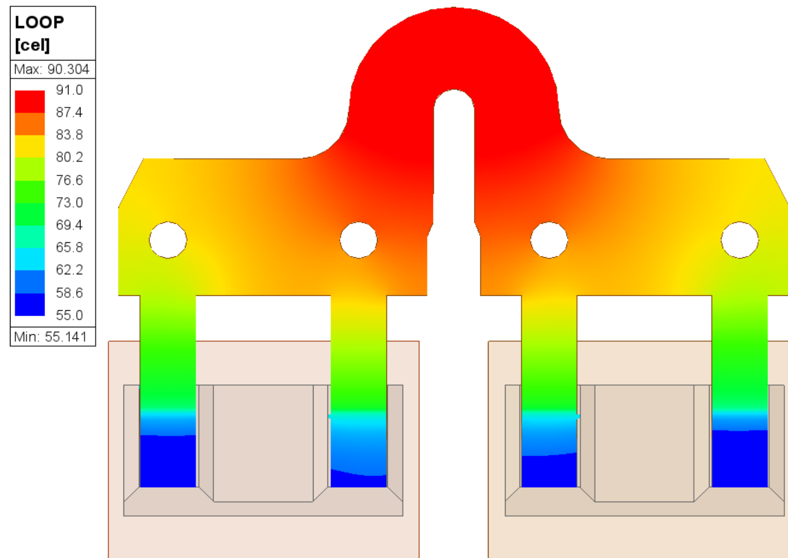


Figure 40: Temperature distribution on the primary current loop

In the previous Figure 40 is visible, that the heat flows to the PCB which here behaves as a heatsink. Therefore, the temperature on the loop differs significantly. Due to the lower thermal conductivity of the epoxide, the gradient over the package is quite high. It equals $\Delta T_{\text{package}} = 24.2$ °C and visualization can be seen on Figure 41 left. Also, a detailed view, where the upper half of the package is hidden can be seen in Figure 41 right.

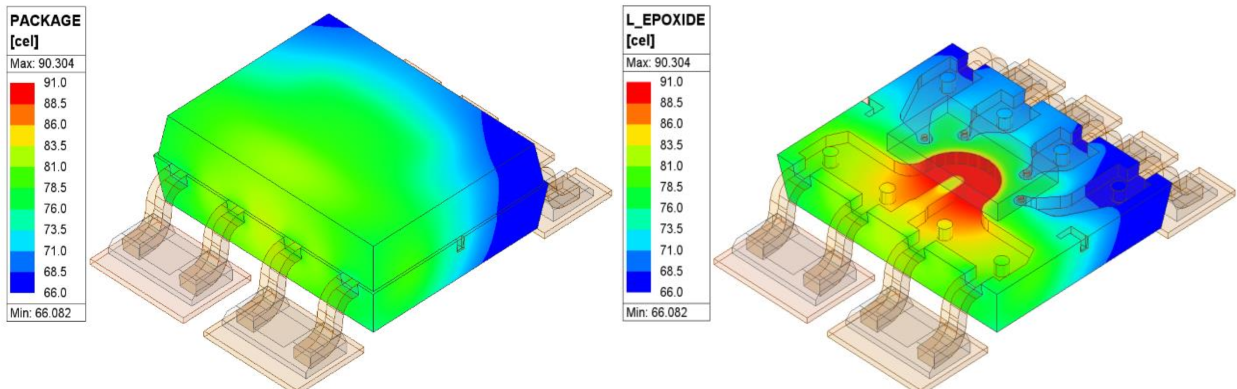


Figure 41: Temperature distribution over the package (left), detailed temperature distribution inside the package (right)

### 13.3.3. Temperature distribution over the PCB

According to the visualization of the thermal conductivity of the PCB which can be seen in the Appendix section, temperature distribution over the PCB has a similar shape. This is visible in Figure 42. $T_{\mathrm{PCB-MAX}} = 65.9\ °\mathrm{C}$. An interesting detail is a visualization of the temperature distribution on the routes above the package. Nonetheless, it is visible that PCB here works as a good heatsink, and the temperature from the package is well dissipated.

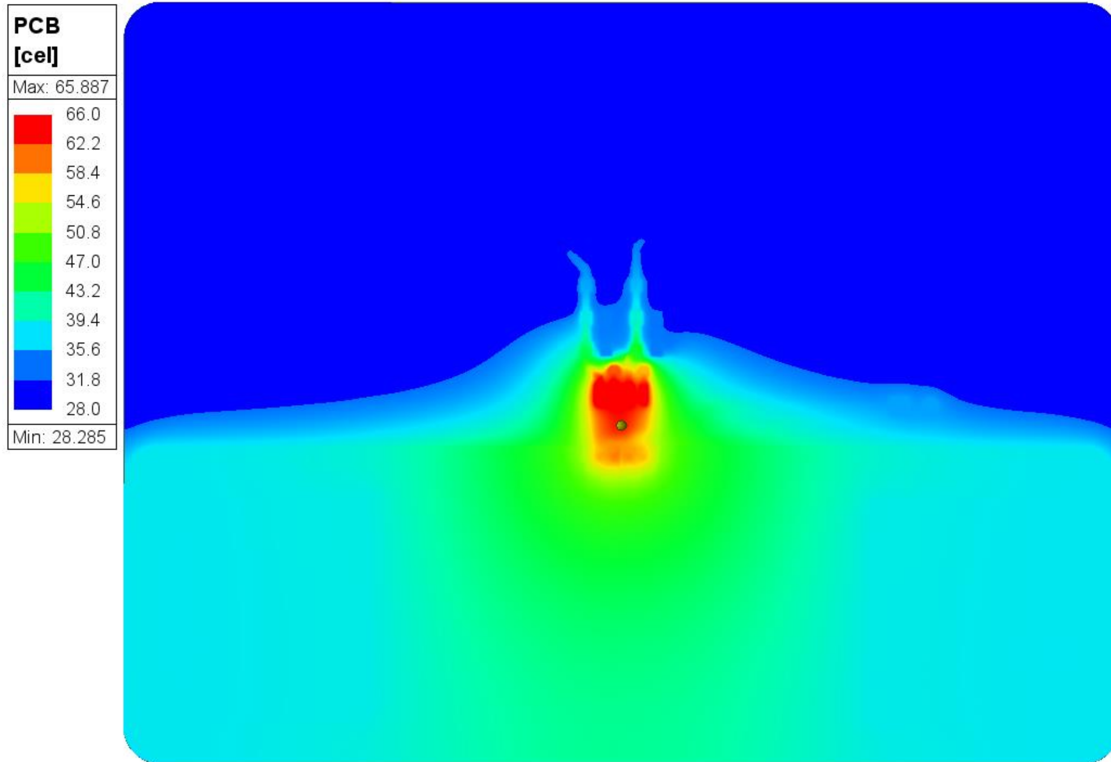


*Figure 42: Temperature distribution over the PCB TED-0004110*

# 14. Alternative solution with the STEP model of PCB TED- 0004110

Importing a step model of the PCB directly to the AEDT is the next possibility of simulation. The step model of the PCB is much more detailed than the model exported from the SIwave e.g. information about vias in each layer and so on. The assumption is that the step model of the PCB could give more precise results. The drawback is that the simulation will be much more demanding.

The idea is to simulate PCB as the other components. First, PCB will be simulated in the Maxwell tool to obtain EM losses which will be then imported into the Icepak solver. The rest is similar to the previous simulations. The system is connected together in the Icepak tool and thermal calculations will be made.

## 14.1. Maxwell solutions

The setting of the simulation here is the same as described in section 12. The model of the PCB needs to be upgraded with two thin current terminals. These terminals are the same size as the terminals of the wires because the wires will be connected to the same place in 14.2. The rest of the PCB model is equal to the description in section 11.1. Biasing current is set to 50 A and ambient temperature is set to 25 °C. PCB is visible in Figure 43.

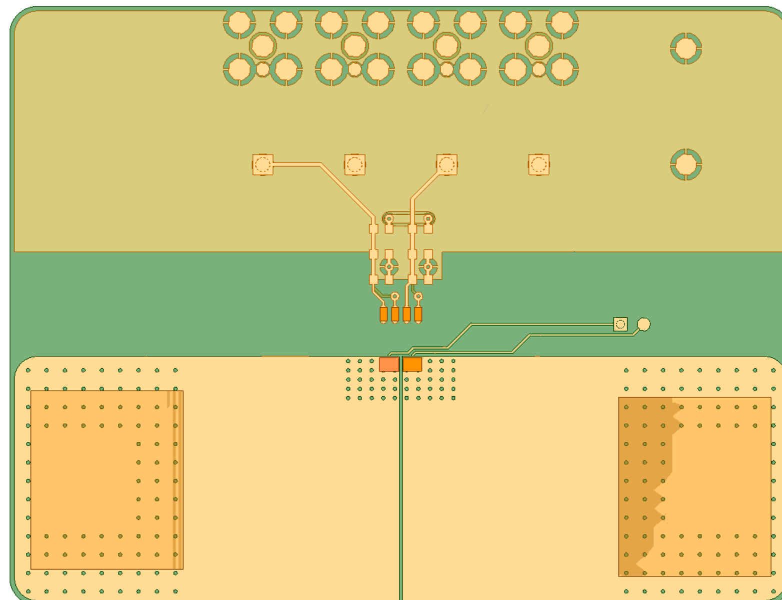

*Figure 43: Step model of the PCB TED-0004110, top view*

### 14.1.1. Results

Results of the simulations of EM losses in the package and wires are the same as described in sections 12.1 and 12.2 because their simulation conditions are the same. An important result is the EM loss in the PCB model. Figure 44 shows a visualization of the current density $J$ in the PCB model. According to previous results from SIwave simulations, it is not surprising that the highest current density is around the pads where the chip is connected. The maximal current density from the visualization is $J_{\mathrm{MAX}} = 2.44 \times 10^{8}\ \mathrm{A/m^2}$. Losses are not visualized here, because the

plot does not show anything interesting. Total solid losses in the PCB equal $P_{\text{solid}} = 0.49$ W. This result significantly differs from the previous solutions in 11.2.

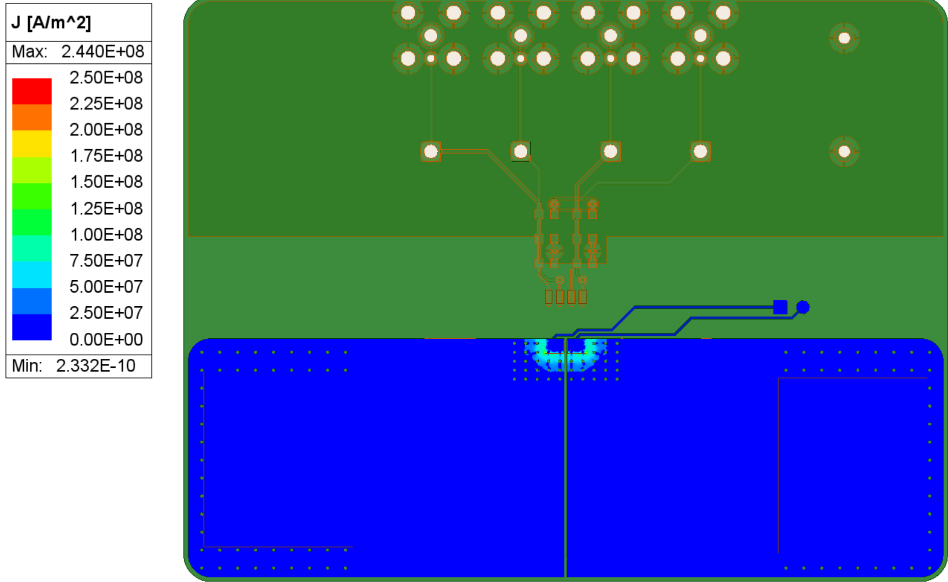


*Figure 44: Current density in the PCB, top view*

## 14.2. Icepak solutions

Because this model is more detailed than the model in section 13, precise meshing here is even more important. The models of the wires and package are the same. So, meshing here does not differ from the previous solution. 3D meshing of the PCB results in too many cells or the mesh is too coarse. Both variants result in the failure of the solution. Therefore, 2D meshing is used again. The connected model of the system is visible in Figure 45.

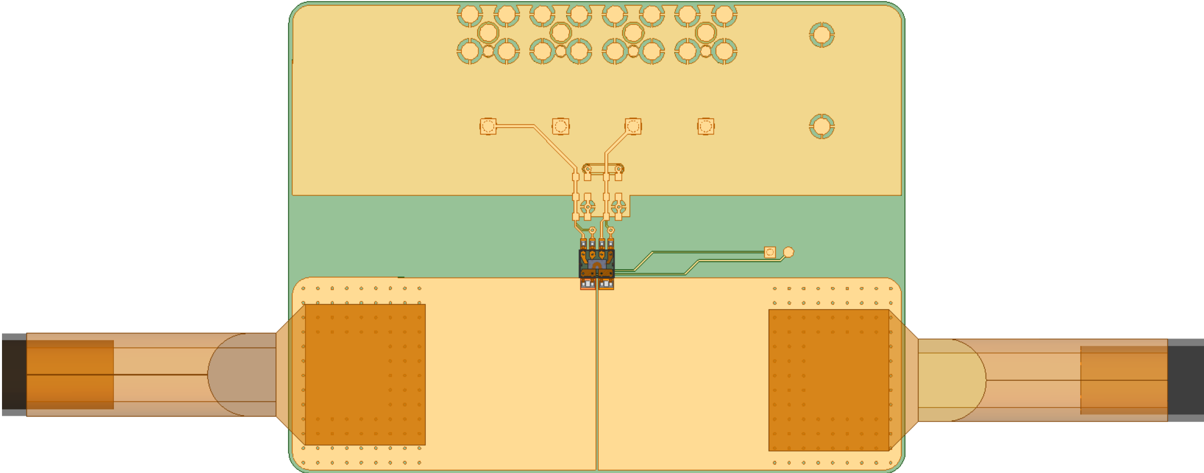

*Figure 45: Model of the system with step model of the PCB TED-0004110, detailed top view*

Because of too much detail in this model, everything takes too much time. Even basic validation of the system, which takes only serval seconds in the previous solutions, it takes serval minutes with this variant.

## 14.3. Results of the STEP model

After many attempts, I decided to leave this solution. The main reason is that this attempt did not lead to useful results. This solution was not even computable. Many times, the solution led to divergence. This problem was probably caused due to the quality of the mesh which was not good enough. The upgrade in meshing led to too high a number of meshing cells or did not lead to convergence.

Losses in the PCB were significantly different from the model calculated in the SIwave (section 11.2). I would expect similar results because both models are more or less the same. The next argument is that all calculations took a long time. Also, operations with this model were not so user-friendly.

So, after all this alternative is much worse compared to the one used in sections before. It is worse in the time consumption, in the memory consumption, and also in the final results, because I cannot obtain any. Therefore, the next simulations will be done in the way described in the previous solution.

# 15. Simulations of two-layer PCB TED-0003528

A different PCB from sections 11.1 and 13 is used in this section. This printed circuit board is meaningly different from the previous one. Its dimensions are different – smaller. TED-0003528 has only two conductive layers. These layers are thinner than copper layers by previously used PCB TED-0004110. All these parameters should make TED-0003528 worse than the PCB used before.

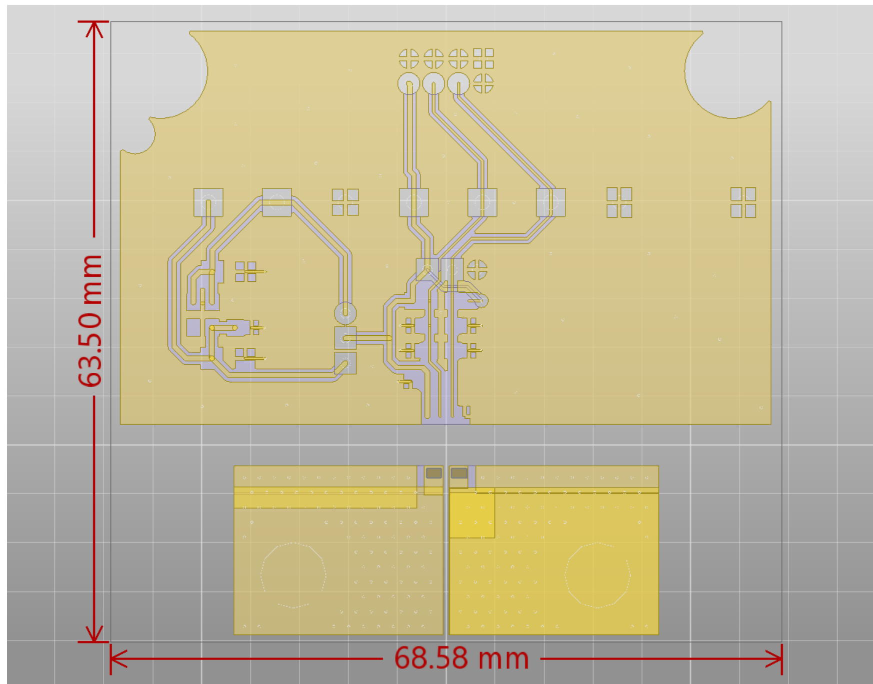


*Figure 46: Model of the PCB TED-0003528*

PCB can be seen in Figure 46 above. The setting of the simulation is pretty much the same as in section 11.1. The total current across the PCB and the chip is 50 A. Between connecting pads is set the potential of 1 V. PCB set to the simulation is visible in Figure 47 below.

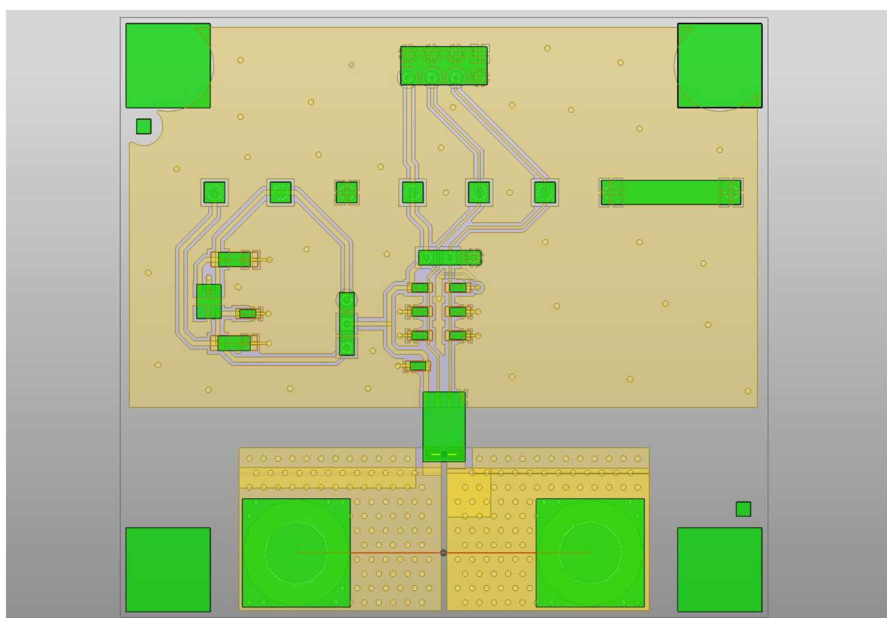

*Figure 47: Model of the TED-0003528 PCB prepared for the DC simulation*

## 15.1. SIwave results

As was described in 11.2, an adaptive mesh solution is used, so no other settings are necessary. Mesh is visible in Figure 48 below. It is dense enough to provide precise calculations.

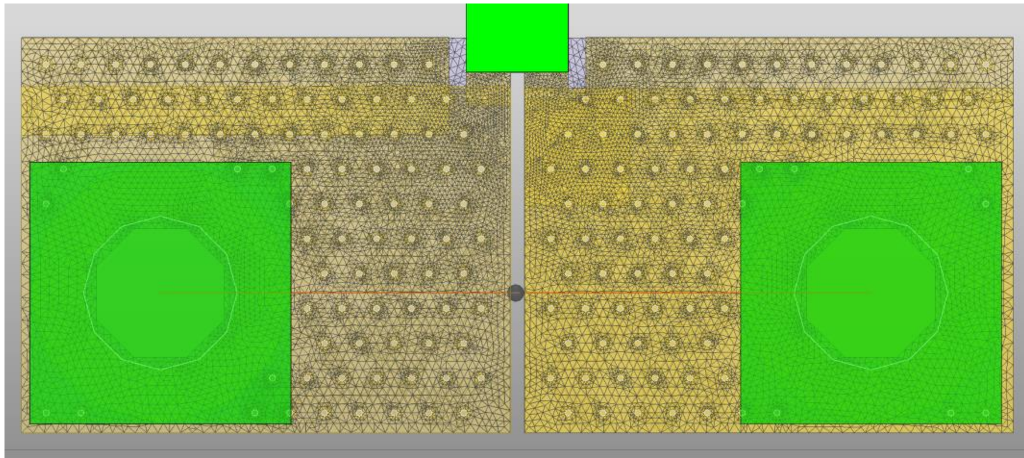

*Figure 48: Meshing of the current loop with adaptive mesh*

The results of the *DC IR* simulation are visible in the figures below. Figure 49 shows results of the same physical quantities as in the 11.2, e.g. current density, via current or power. It is obvious that maximal power loss is near the chip connection. The total power loss in the PCB equals $P_{\mathrm{solid}} = 1.55\ \mathrm{W}$. This value is approx. two times higher than the previously simulated PCB TED-0004110. Due to this ascertainment and following section 16.2.2 I decided to simulate and measure this system on the lower load current $I_{\mathrm{LOAD}} = 25\ \mathrm{A}$.

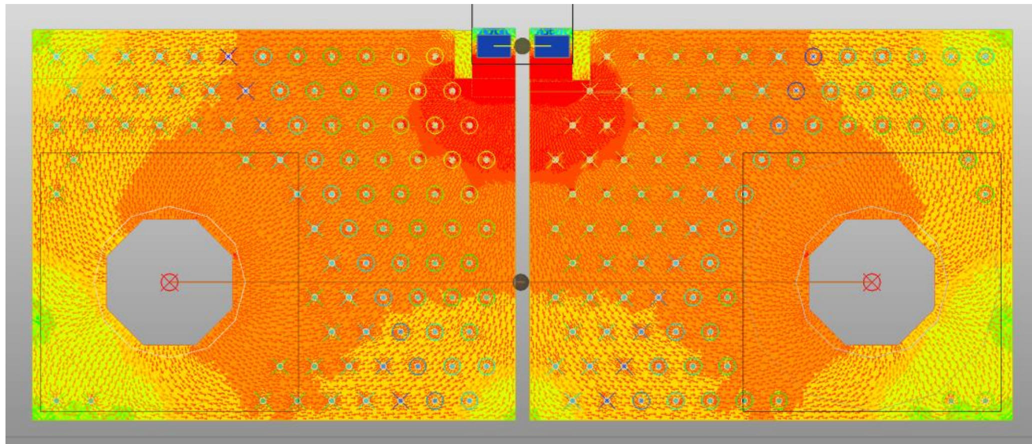

*Figure 49: Last iteration of the coupling. Arrows represents current density J, X and O represents via currents Iv and background colors represents power P, load current 50* A

Next graphs Figure 50 and Figure 51 show results computed for the lower input current. Losses in the PCB are significantly lower than for 50 A. Total computed losses in the PCB equal $P_{\mathrm{solid}} = 0.35\ \mathrm{W}$. Temperature distribution across the PCB visible in Figure 51 looks different from the distribution obtained in Figure 21. Dissipation has here much more chaotic shape and it is not ideal. This is caused by the larger area of the solid copper on the right side from the top view. The area on the left contains more components and routes which decreases thermal conductivity in this direction.

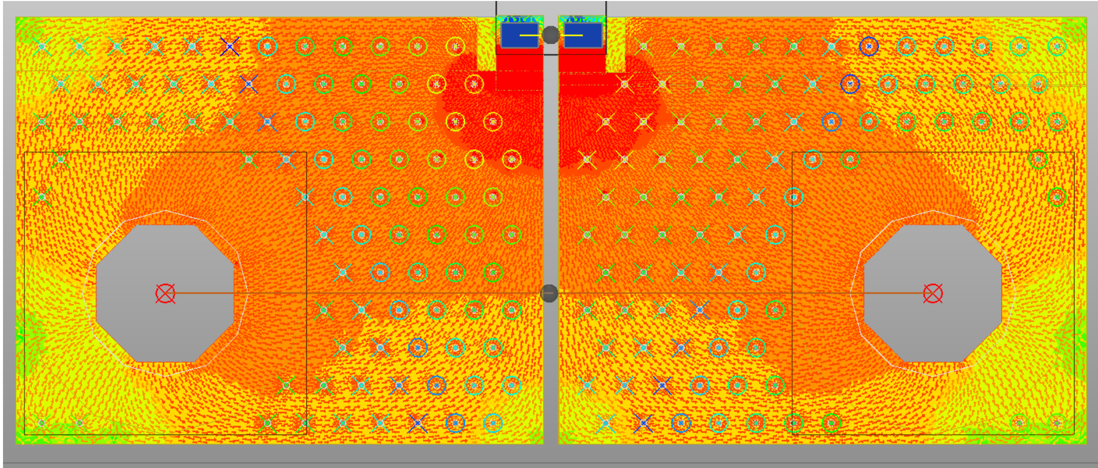

*Figure 50: Last iteration of the coupling. Arrows represents current density J, X and O represents via currents Iv and background colors represents power P, load current 25* A

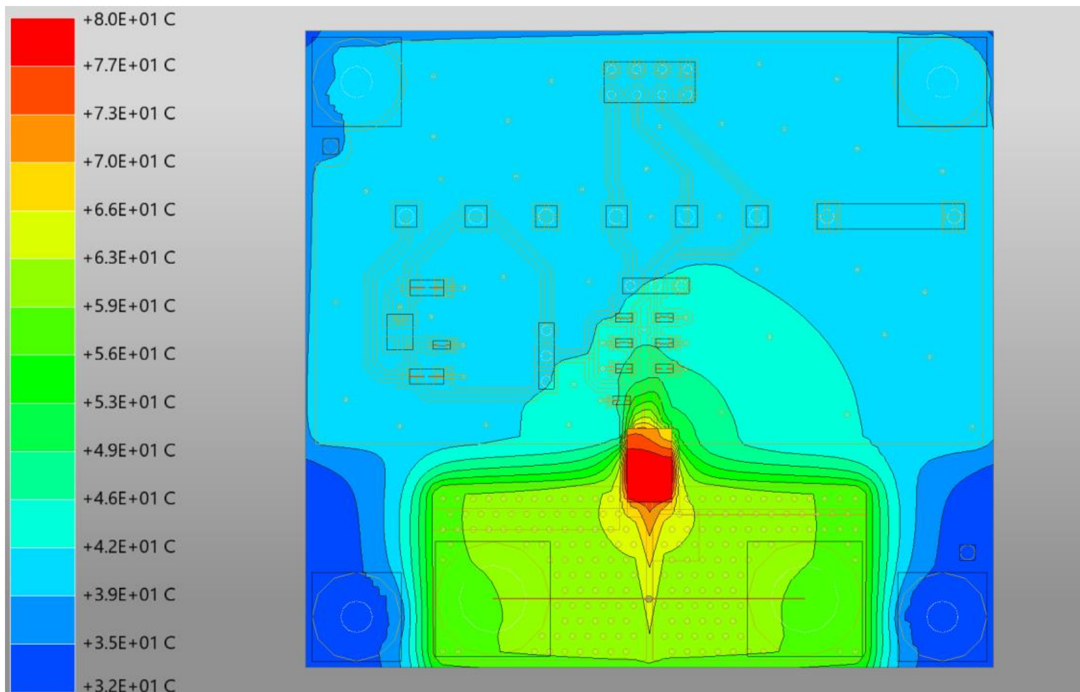


*Figure 51: Graph of the temperature distribution from the SIwave, load current 25 A*

## 15.2. Maxwell results

In the Maxwell tool are again simulated wires and a model of the package. The difference between this section and section 12 is the lower load current. The reason was described in previous paragraphs. Results are similar to section 12, but the current density and losses are significantly lower, which makes sense. The results are visible in Figure 52 and Figure 53.

For the model of the wires, the maximal current density due to the visualization is $J_{\mathrm{MAX}} = 1.79 \times 10^{6}\ \mathrm{A/m^2}$. It is visible on the ring terminal at the end of the wires. Total computed solid losses in the wires are $P_{\mathrm{solid}} = 0.32\ \mathrm{W}$.

For the model of the package, maximal current density due to the visualization is $J_{\mathrm{MAX}} = 5.15 \times 10^6\ \mathrm{A/m^2}$. As expected, the maximum is visible on the lead frame current loop under the die. Total computed solid losses in the package model are $P_{\mathrm{solid}} = 0.53\ \mathrm{W}$.

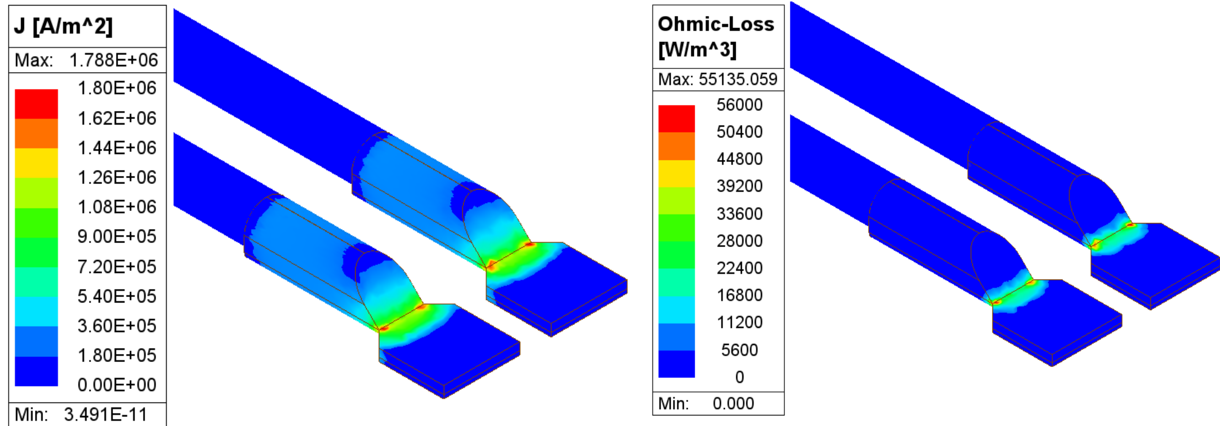


*Figure 53: Current density in the wires (left) an ohmic losses in the wires (right)*

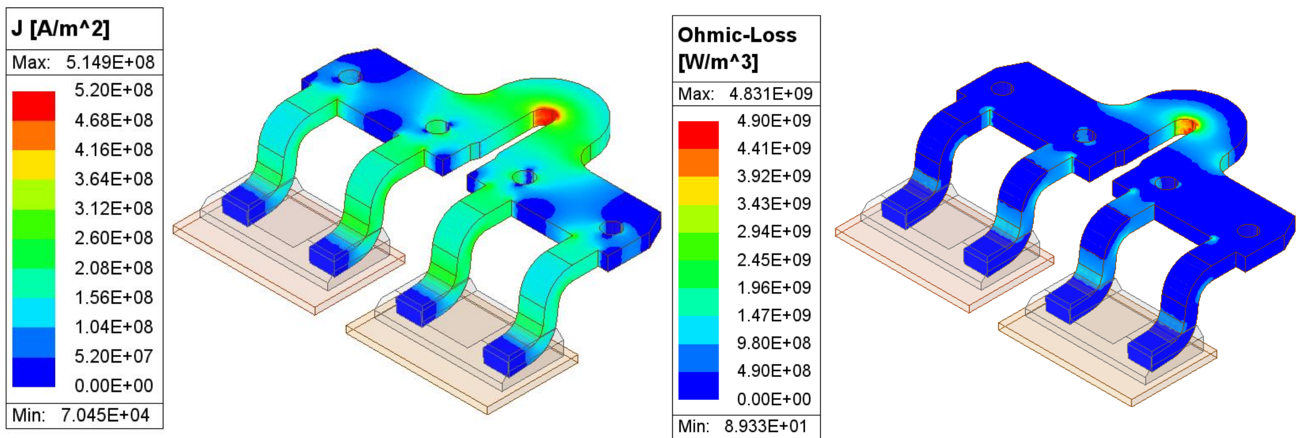


*Figure 52: Current density in the current loop (left) and ohmic losses in the current loop (right)*

## 15.3. Icepak results

The simulation ended after 2 successful passes. This means 2 calculations of the 2-way coupling. Each temperature calculation takes a maximum of 100 iterations. Again, this setting ensures that each pass will converge successfully. In this case, 2 passes were enough for the temperature stabilization.

Crucial results are shown in the next subsections. Here again, the main point of interest is the chip's die. Temperature distribution over the system and total temperature gradient over the die is the main goal. Also, other temperature dissipations are important. Some important results are shown below, some others are shown in the Appendix section at the end of the document.

### 15.3.1. Temperature gradient over the die

The next figures show the temperature distribution on the chips die. The temperature gradient is easily visible, but the shape differs from the previous simulations with the PCB TED-0004110. The highest temperature copies the shape of the current loop but as can be seen in Figure 51, temperature distribution over the PCB, especially around the chip is not ideal in all directions, and therefore distribution over the die is not the same as in previous sections. The highest calculated temperature on the surface is $\boldsymbol{T}_{\mathbf{MAX}} = \mathbf{40.7}\ {}^{\circ}\mathbf{C}$. The lowest temperature on the surface equals $\boldsymbol{T}_{\mathbf{MIN}} = \mathbf{38.6}\ {}^{\circ}\mathbf{C}$. The lowest temperature is visible in the bottom view of the die in Figure 55. For the same reason as mentioned in the section above, 4 cold spots are due to the connected copper pillars.

Due to this observation, the total temperature gradient over the die equals $\boldsymbol{\Delta T}_{\mathbf{visualization}} = \mathbf{2.1}\ {}^{\circ}\mathbf{C}$. Nonetheless, even though this PCB has worse parameters and so a lower biasing current was used, the thermal gradient over the die is lower which is a quite surprising result.

*Figure 54: Temperature gradient over the die, top view*

The used point monitors (**see Figure 61)** are here again placed on the same spots, where the measuring diodes lay on the real chip and are measured (**more details in chapter 16**). So, again here to confirm the model it is possible to determine the temperature gradient between those P-N junctions. These results are visible in Table 2. The lowest temperature is on the thermometer number 5 and the highest is on the number 0 which is the same as in the previous simulations. The total temperature gradient between the spots where measuring diodes lay equals $\boldsymbol{\Delta T}_{\mathbf{monitors}} = \mathbf{1.3}\ {}^{\circ}\mathbf{C}$.

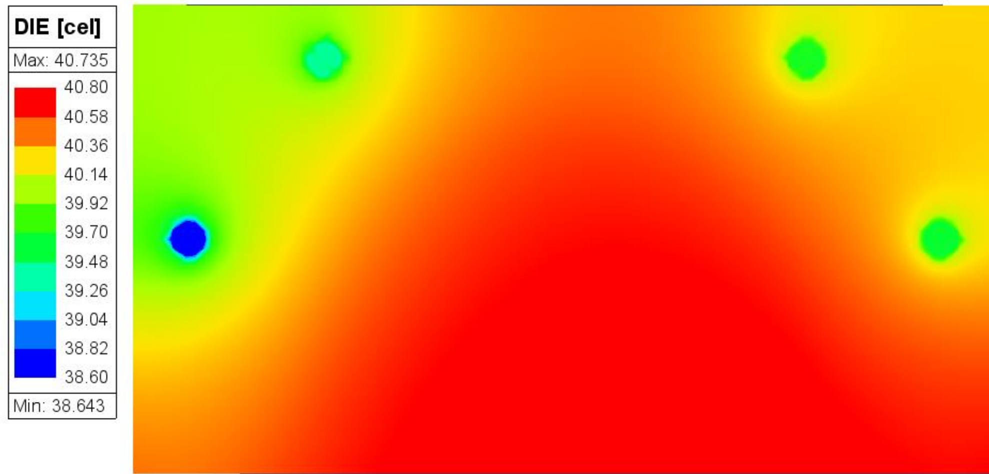


*Figure 55: Temperature gradient over the die, bottom view*

*Table 2: Temperature on the measuring diodes, TED-0003528*

| Name | Temperature [°C] |
|---|---|
| diode_0 | 42.6 |
| diode_2 | 42.0 |
| diode_6 | 41.9 |
| diode_1 | 41.7 |
| diode_3 | 41.5 |
| diode_4 | 41.4 |
| diode_5 | 41.3 |

### 15.3.2. Temperature distribution in the package

The temperature distribution here in the ACS37013 package reflects the temperature distribution on the primary current loop. On the loop is the highest temperature in the package. The maximal visualized temperature on the loop equals $T_{\text{loop-MAX}} = 52.2\ °\text{C}$ what can be seen in Figure 56.

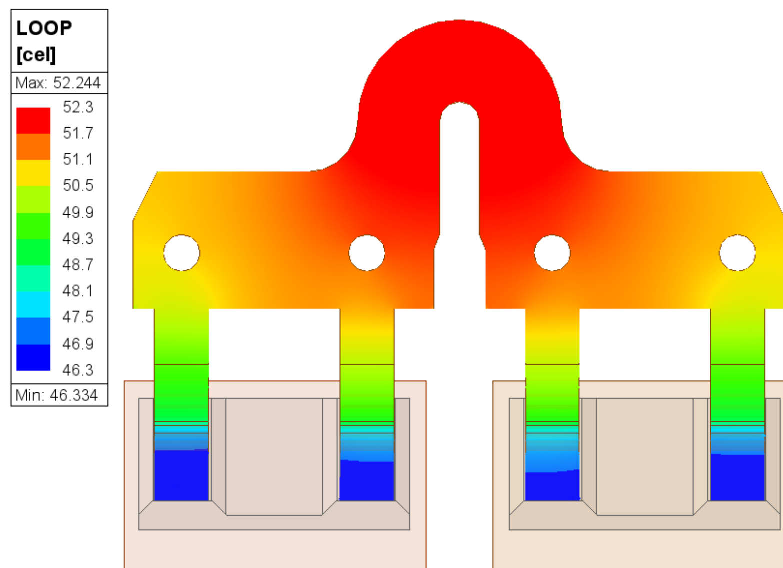


*Figure 56: Temperature distribution on the primary current loop*

The previous figure shows that the primary current loop is also here primary heat source. Again, it is visible that the current loop is cooled due to the connection to the PCB and therefore temperature on the terminals is significantly lower than the highest point in the middle. But in comparison to the PCB TED-0004110 temperature gradient in the loop is lower because the PCB heats up more than previously mentioned.

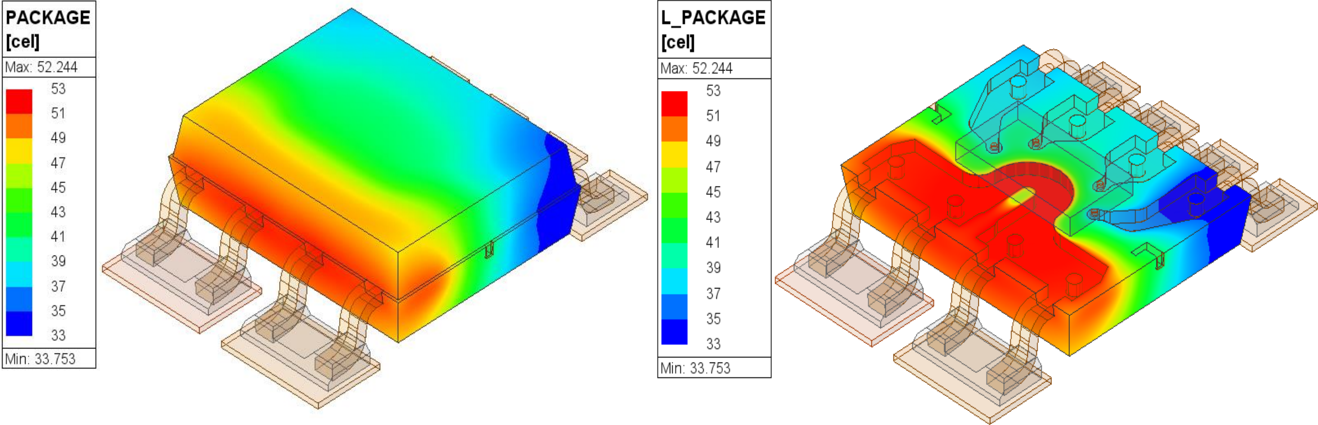


*Figure 57: Temperature distribution over the package (left) and detailed temperature distribution inside the package (right)*

In the Figure 57 can be seen the temperature distribution over the package especially over the epoxide. The warmest place is around the current loop which is not surprising. Due to the uneven distribution of heat on the PCB (see Figure 51) the coldest place in the package lies in the upper right corner. The total temperature gradient over the package equal $\Delta T_{\text{package}} = 18.5\ °\text{C}$.

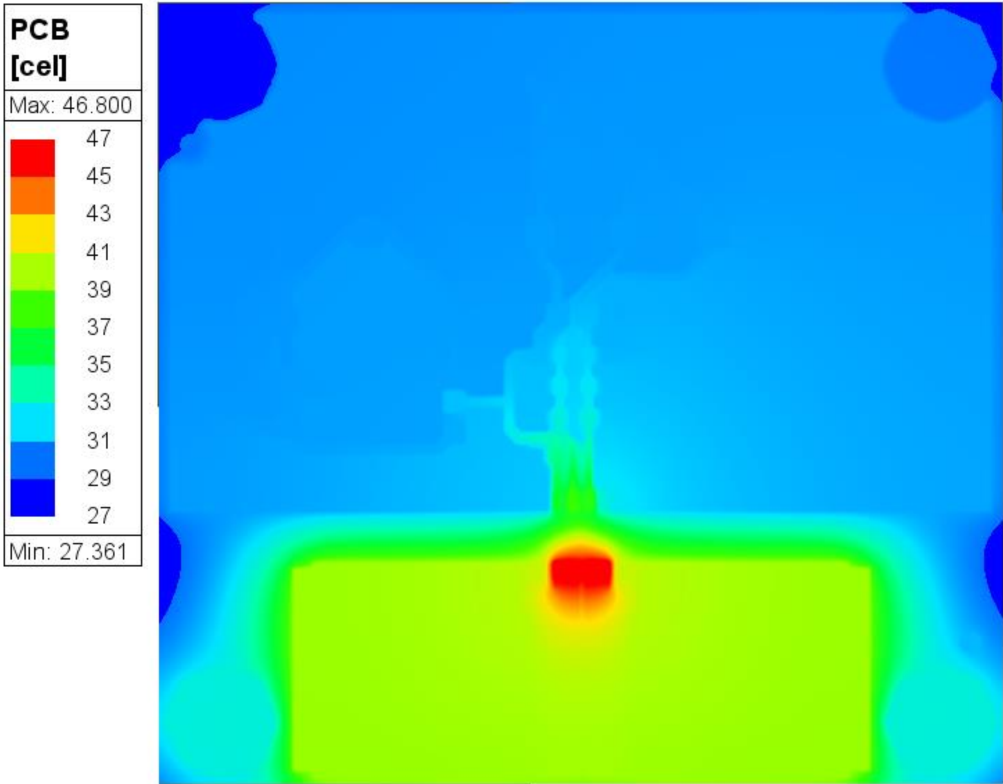


*Figure 58: Temperature distribution over the PCB TED-0003528*

### 15.3.3. Temperature distribution over the PCB

Temperature distribution over the PCB TED-0003528 reflects results from the SIwave solver. According to the visualization of the thermal conductivity of the PCB which again can be seen in the Appendix section, temperature distribution over the PCB has a similar shape but differs more than the results of the PCB TED-0004110. Due to fewer routes on the right side than on the left side, the heat spreads better to the right and so the left side heats up more (this is according to the equations mentioned in section 3). In the Figure 58 can be seen this visualization. The maximal temperature is $T_{\mathrm{PCB-MAX}} = 46.8\ °\mathrm{C}$. An interesting detail is a visualization of the temperature distribution on the routes above the package. Nonetheless, it is visible that PCB here works as a heatsink, and the temperature from the package is dissipated.

# 16. Measuring

To confirm the simulation results it is necessary to provide real laboratory measurements. It is the only way to confirm or deny the correctness of the created model. The measurement method is based on the one described in section 8 – measuring temperature via voltage drop on the P-N junction with 2 currents method.

## 16.1. Setup

The measurement setup is shown in the schematic diagram in Figure 59. It contains a measured device soldered to the PCB, an accurate multimeter, source meter, current source, programmer, Allegro validation board, and PC, concretely MATLAB scripts. The measured device is placed in the temperature chamber, where the ambient temperature can be set accurately.

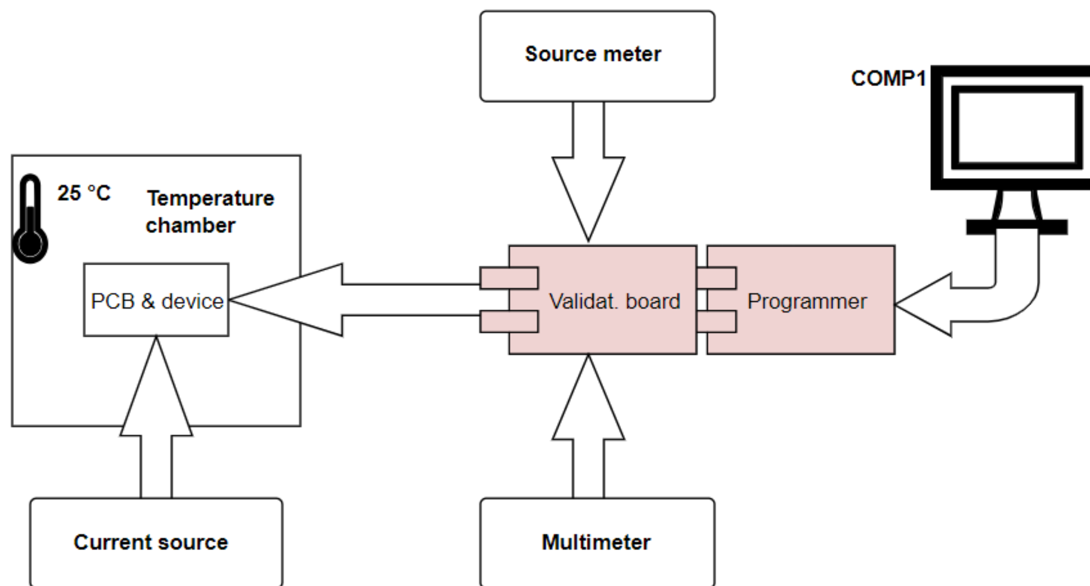


*Figure 59: Schematic diagram of the measurement setup crated with DigiKey's Scheme-it (https://www.digikey.com/en/schemeit)*

Used voltmeter is a digital multimeter **Keysight 34470A**. Its resolution is up to 7 and ½ digits, which is important for this measurement. The measured voltage drop on the P-N junction has relatively low values. The source meter is **Keysight B2901B**. This device can source or sense voltage or current. Important is, that this source meter can source low currents, which is important in this application. The power supply for the input load current is **Keysight N8732A**. It can source current up to the low hundreds of Amps with a total power of 3.3 kW. As was written before, the load currents are 50 A and 25 A, and the voltage drop on the whole system is low. The current source is connected to the PCB using two wires with a cross-section of 70 mm$^2$.

To achieve the best setting of the ambient temperature and do the measurement as close as possible to the conditions in the simulation I decided to close the system inside the thermal chamber **TestEquity chambers TE-115A**. Its temperature range is from -73 °C to +175 °C. The oven has access ports from the left and the right side. In the middle of the door, there is a small window for inspection. The oven can be controlled remotely via MATLAB scripts.

**The programmer** is a device ASEK-35, a device created by Allegro MicroSystems. It allows users to communicate with Allegro's devices, program them, or read some values. **A validation**

**board** is a device designed for simplifying measurement. It allows users to connect a variety of measuring devices, pick the one that is needed, and connect it to the specific pin.

The measuring procedure is fully controlled by the MATLAB scripts. First, the device soldered to the PCB is put inside the temperature chamber and the current loop is connected to the supply wires. Communication pins are connected to the validation board and the validation board is connected to the programmer. Measuring devices (multimeter and source meter) are connected to the validation board. The programmer is connected via USB to the PC. All devices are connected via ethernet to the LAN and so can be controlled from the PC. This is visible in Figure 60.

*Figure 60: Measuring setup (left), detail of the temperature chamber (right)*

First, the temperature in the chamber is set to 25 °C. Soak time for the temperature to stabilize is half an hour. The oven itself provides stabilization by heating up or cooling down the measuring chamber. The whole time, the fan is turned on. But the simulation calculates with a natural convection which means no fan and laminar flow only. So, after half an hour the fan is turned off and measuring begins.

The script starts with turning on the power for the device and some attempts of communication. Then it sets up communication with the measuring devices. The load current is set on the current source (50 A for TED-0004110 and 25 A for TED-0003528), and it is turned on with a soak time of 25 minutes. After the soak time, the current source is still turned on and the measuring of the temperature starts.

Due to the communication net across the chip, it is possible to address each diode (or P-N junction) which measures the temperature. The total number of thermometers on the die is seven and they are placed at important places. As can be seen in Figure 61, maximal temperature is expected on the diodes 0 and 2, because they are closest to the lead frame current loop. On the other hand, the lowest temperature is expected on the P-N junction number 5, because this

place in the corner is farthest from the primary current loop. Therefore, the maximal measured gradient is expected between those points.

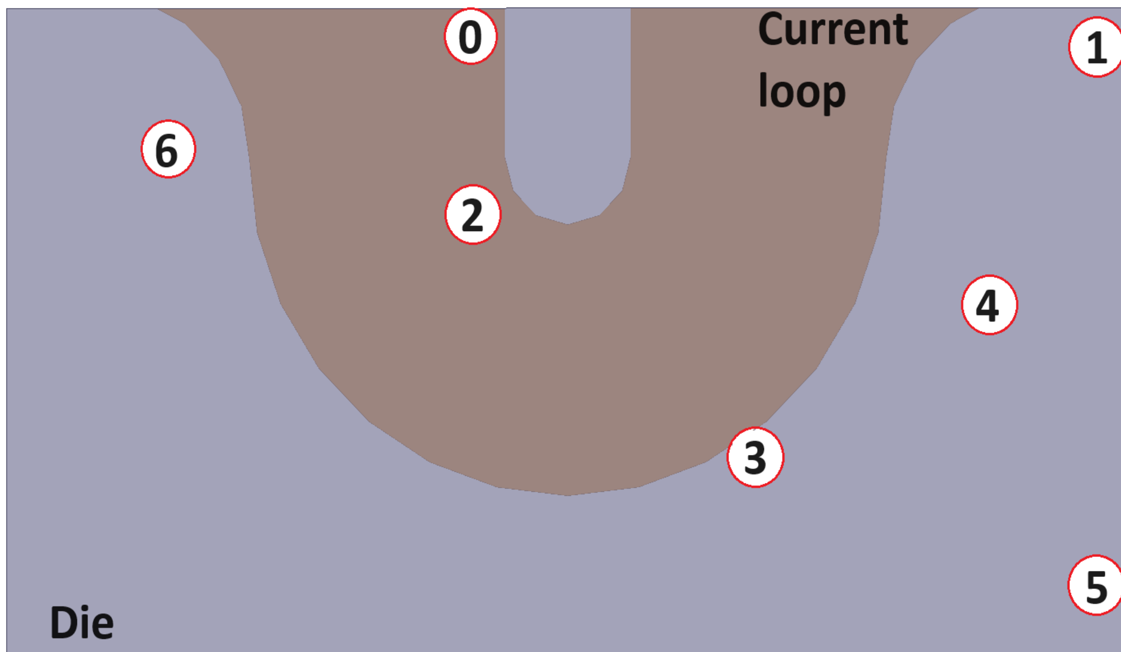


*Figure 61: Thermometer placement on the die*

The measuring then proceeds as follows: First current ($30\ \mu A$) is sourced from the source meter to the device, anode of the first diode (diode number 0) is addressed and the voltage here is sensed. Then cathode of the same diode is addressed and voltage here is sensed. From these data, it is possible to compute voltage drop on each diode. Other diodes are measured in the same way. It is important to measure anode and cathode voltage on one diode in the shortest possible time because only then it is ensured that temperature would be measured correctly. Each diode is measured 20 times at one biasing current, then each diode is measured 20 times at the second biasing current ($80\ \mu A$). After measuring the average drops are calculated. Temperature is calculated according to equations in section 8.

## 16.2. Measuring results

The results of the measuring are visible in the next chapters. Few devices were measured on the PCB TED-0003528 and on the PCB TED-0004110. All devices were measured repeatedly under the same conditions. After these measurements, the average temperatures on each device diodes were calculated. The next step was to calculate average temperatures on the diodes across all measured devices. After this, I calculated an average temperature gradient for both PCBs.

### 16.2.1. TED-0004110

Measuring showed that the highest temperature is measured with the P-N junction number 0, as expected. Temperature is mostly dissipated around the current loop according to Figure 61. The shape of the temperature distribution on the die presumably looks like the result of the simulations in section 13.3.

The highest measured temperature on the die is $\boldsymbol{T_{\mathrm{MAX}}} = \mathbf{79.9\ °C.}$ The lowest measured temperature on the die is $\boldsymbol{T_{\mathrm{MIN}}} = \mathbf{78.0\ °C}$. As can be seen in the Figure 62, the maximal thermal gradient is between the diodes number 0 and number 5, which according to Figure 61 makes sense. The total gradient is $\boldsymbol{\Delta T} = \mathbf{1.9\ °C.}$ The rest of the results can be seen in Table 3. All of the measured results are really similar to the results of the simulations. Crucial is the similar result of the thermal gradient on the die.

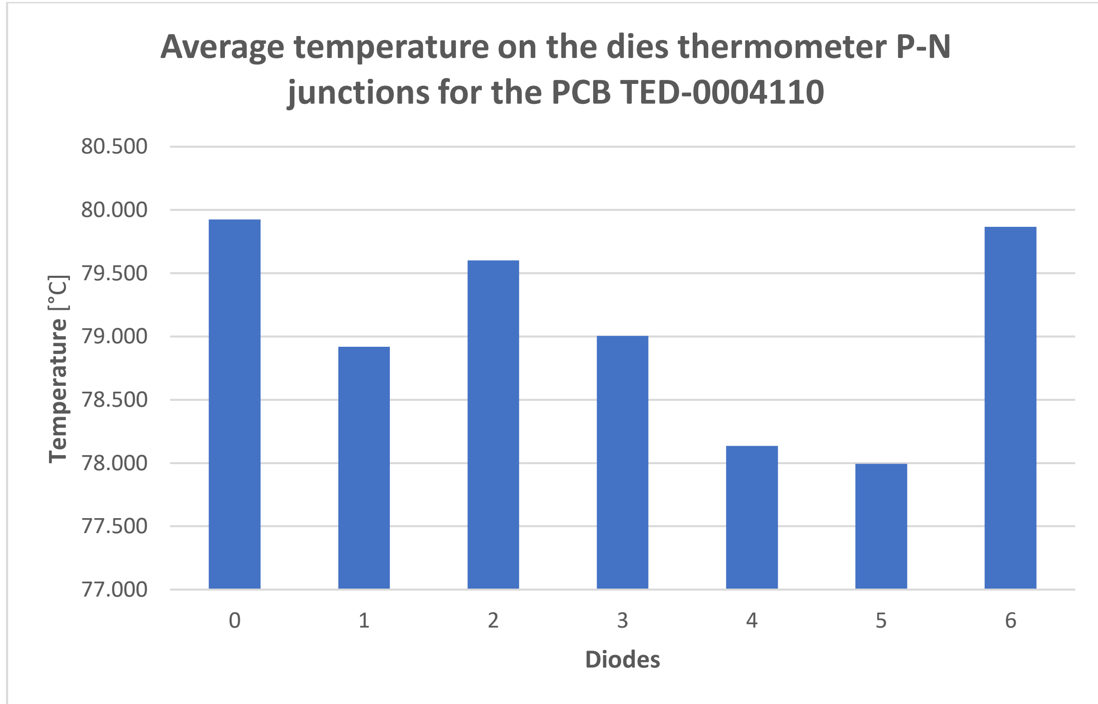


*Figure 62: Average temperature on the die's thermometer P-N junctions for the PCB TED- 0004110*

*Table 3: Average temperature on the die's thermometer P-N junctions for the PCB TED- 0004110*

| Average temperature on the thermometers | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Diode** | diode_0 | diode_1 | diode_2 | diode_3 | diode_4 | diode_5 | diode_6 |
| **Total average** (°C) | 79.9 | 78.9 | 79.6 | 79.0 | 78.1 | 78.0 | 79.9 |
| **Average Gradient** (°C) | **1.9** | | | | | | |

### 16.2.2. TED-0003528

As in the previous section, the highest measured temperature is also here on the P-N junction number 0. Temperature dissipation is here again around the current loop with a similar shape. Interesting is, that the lowest temperature is measured on the P-N junction number 4 compared to the number 5 in 16.2.1 which is according to Figure 61 more likely. This result reflects temperature dissipation shown for example in Figure 51.

The highest measured temperature on the die is $\boldsymbol{T_{\mathrm{MAX}}} = \mathbf{48.2\ °C}$. The lowest measured temperature on the die is $\boldsymbol{T_{\mathrm{MIN}}} = \mathbf{46.7\ °C}$. According to the previous paragraph, the maximal thermal gradient is between the diodes number 0 and number 4. The total thermal gradient is $\boldsymbol{\Delta T} = \mathbf{1.7\ °C}$. All of the results can be seen in Figure 63 and in Table 4.

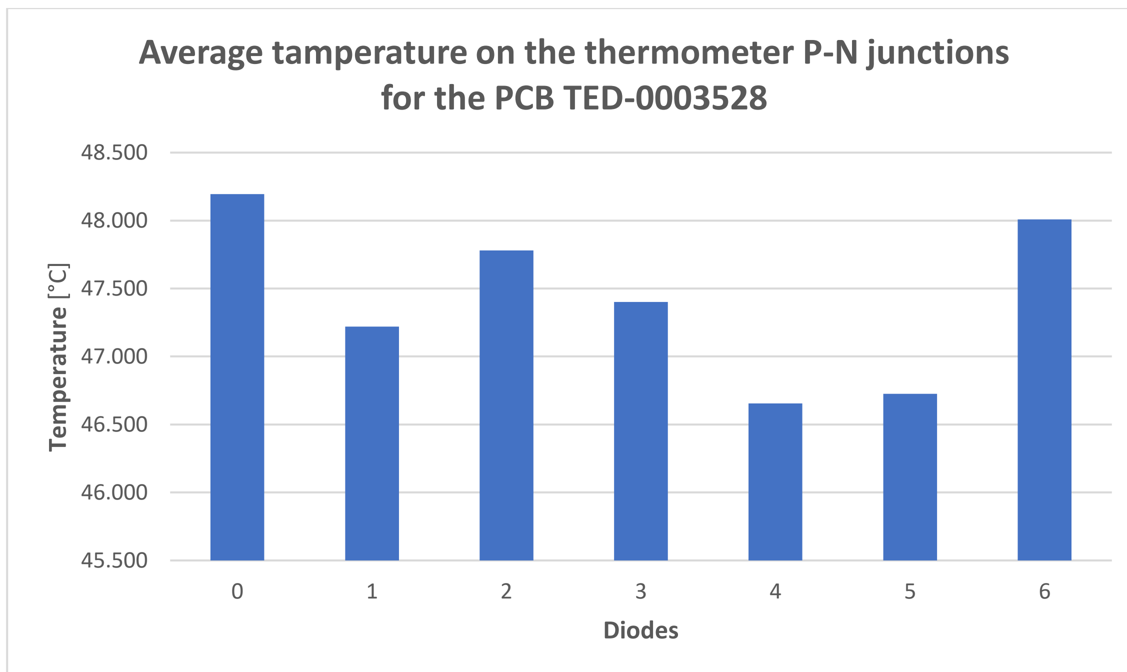


*Figure 63: Average temperature on the die's thermometer P-N junctions for the PCB TED- 0003528*

*Table 4: Average temperature on the die's thermometer P-N junctions for the PCB TED- 0003528*

| Average temperature on the thermometers | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Diode** | diode_0 | diode_1 | diode_2 | diode_3 | diode_4 | diode_5 | diode_6 |
| **Total average** (°C) | 48.2 | 47.2 | 47.8 | 47.4 | 46.7 | 46.7 | 48.0 |
| **Average Gradient** (°C) | **1.54** | | | | | | |

## 16.3. Comparison of the measured and simulated results

For the first measured PCB TED-0004110, the highest measured average temperature equals $\boldsymbol{T_{\text{MAX}-\text{TED}-0004110} = 79.9\ °\text{C}}$. The lowest temperature equals $\boldsymbol{T_{\text{MIN}-\text{TED}-0004110} = 78.0\ °\text{C}}$. The calculated temperature gradient was $\boldsymbol{\Delta T_{\text{TED}-0004110} = 1.9\ °\text{C}}$. These results are close to the simulated ones. The maximal simulated temperature on the diodes is $\boldsymbol{T_{\text{MAX}-\text{simulated}} = 78.0\ °\text{C}}$. So, this result is around 2 °C lower. The simulated temperature gradient equals $\boldsymbol{\Delta T_{\text{simulated}} = 1.8°\text{C}}$. This result is lower around 0.1 °C.

For the second PCB TED-0003528, the highest measured average temperature was $\boldsymbol{T_{\text{MAX}-\text{TED}-0003528} = 48.2\ °\text{C}}$ and the lowes equals $\boldsymbol{T_{\text{MIN}-\text{TED}-0003528} = 46.7\ °\text{C}}$. The calculated temperature gradient was $\boldsymbol{\Delta T_{\text{TED}-0003528} = 1.5\ °\text{C}}$. These results differ more than previous simulations, nonetheless, they are close. The absolute maximal simulated temperature equals $\boldsymbol{T_{\text{MAX}-\text{simulated}} = 42.6°\text{C}}$ which is around 5.7 °C. Simulated temperature gradient equals $\boldsymbol{\Delta T_{\text{MAX}-\text{simulated}} = 1.3\ °\text{C}}$. So, the difference in the temperature gradient is around 0.2 °C. These results are already on the verge but still acceptable.

# 17. Mechanical simulations

The last part of the systems simulation is a mechanical behavior with the rising temperature. These simulations are not simple, and many aspects can change results significantly. It is not easy to obtain exact material parameters because for example parameters of the epoxide which is the package made of probably need to be measured in a specialized lab. Therefore, parameters are set according to the available information.

The model is a simplification of the one used in the Icepak simulations. The whole PCB is approximated with an epoxide material. This is because FR-4 creates most of the PCB and the influence of the copper is not so significant. This was considered after a discussion with an expert on mechanical simulation. Mechanical changes are caused by increasing temperature which was obtained in the Icepak simulations.

## 17.1. Simulation results

As was described in the previous paragraphs, the results are more illustrative than absolutely accurate. Even though after the revision of the expected values of the stress on the die at room temperature, critical points are visible. Nonetheless, the total accuracy of the absolute values could be better. Many aspects influence this result. The first one is the previously mentioned material parameters, which are hard to obtain. The next issue is that the mechanical solver in the AEDT package is not as perfect as a separate Mechanical solver. Due to the compatibility of one GUI with the other solvers, some features are missing here.

Due to the lack of a license for the mechanical solvers in our company, I asked Ansys support to run the simulations of the created mode for us. Thankfully, due to the good cooperation, they did it. Some results are shown below. Figure 64 shows the displacement in the system. Wires are not simulated here. It can be seen that the whole system is bending. The maximal value of the bend is $\Delta L = 33.169\ \mu m$. Figure 65 shows the detailed view of the displacement of the package. It can be seen that epoxide flexes most in the outer surrounding layers. Also, a detailed view of the lead frame is visible in the same figure.

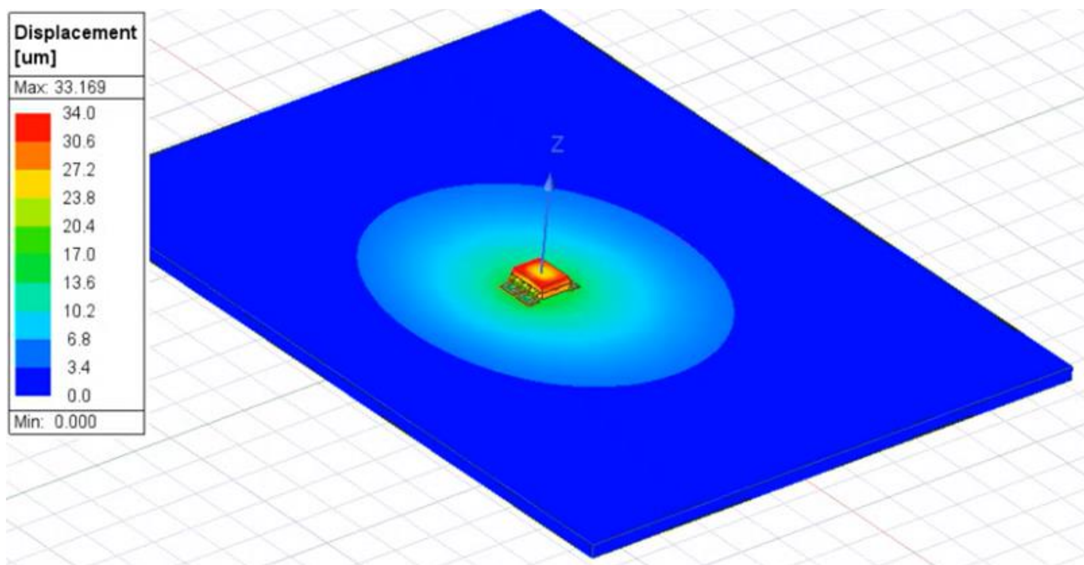


*Figure 64: System displacement*

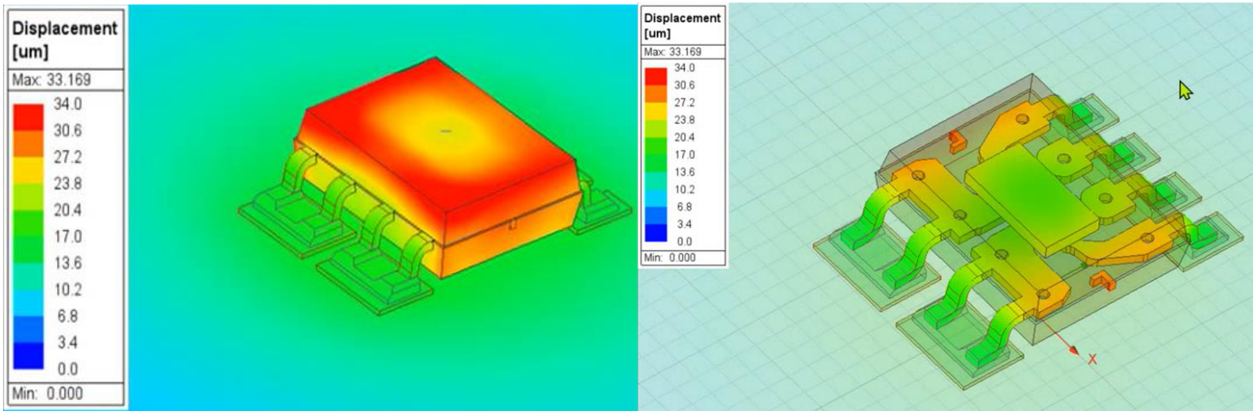


*Figure 65: Detailed view of the package displacement*

The last 2 figures in this chapter show the stress acting on silicon. Due to the movement of the epoxide and the possible movement of the die itself, the stress grows with temperature. As the copper pillars are holding the die, the stress here is the highest. Therefore, in Figure 66 it can be seen, that the maximal stress on the die is in those places. Stress across the die is around the $180\ \mathrm{MPa}$ but the peak around the copper pillars is over the $900\ \mathrm{MPa}$.

Figure 67 shows the stress plotted on the upper face of the die. It can be seen that it reflects the results from the Figure 66 and the maximums are placed on similar spots.

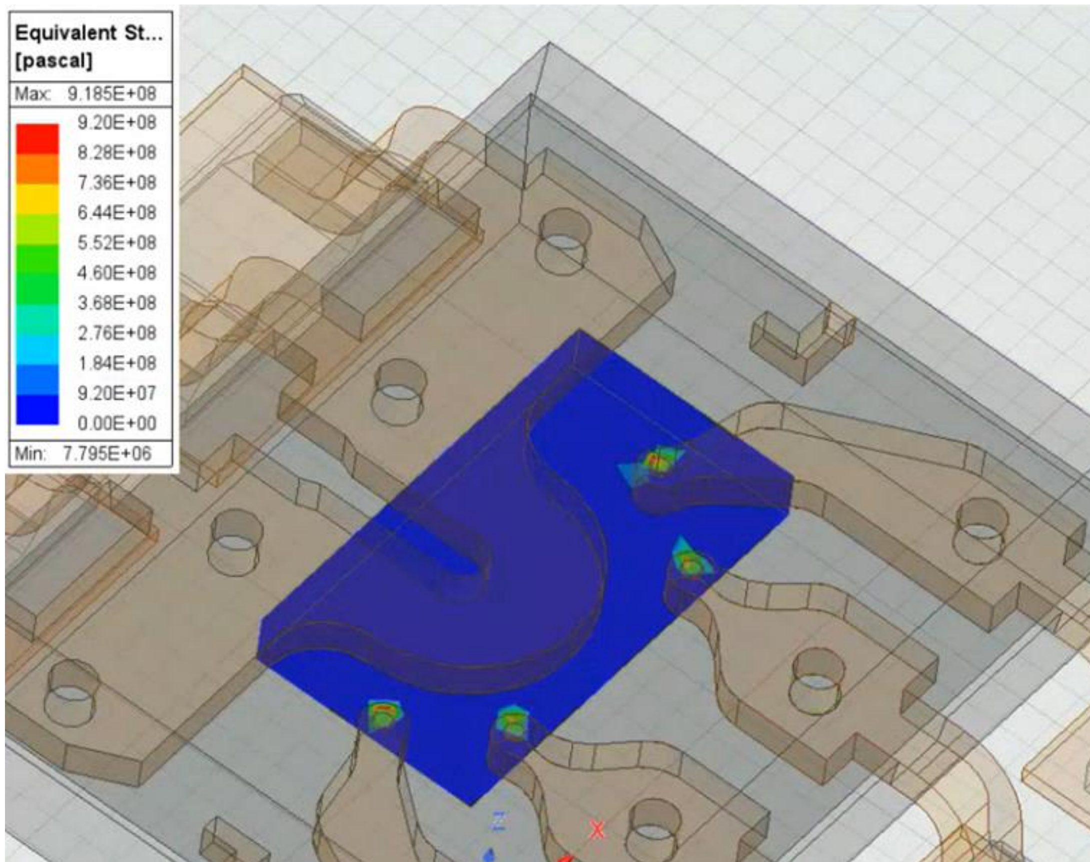


*Figure 66: Equivalent stress on the die*

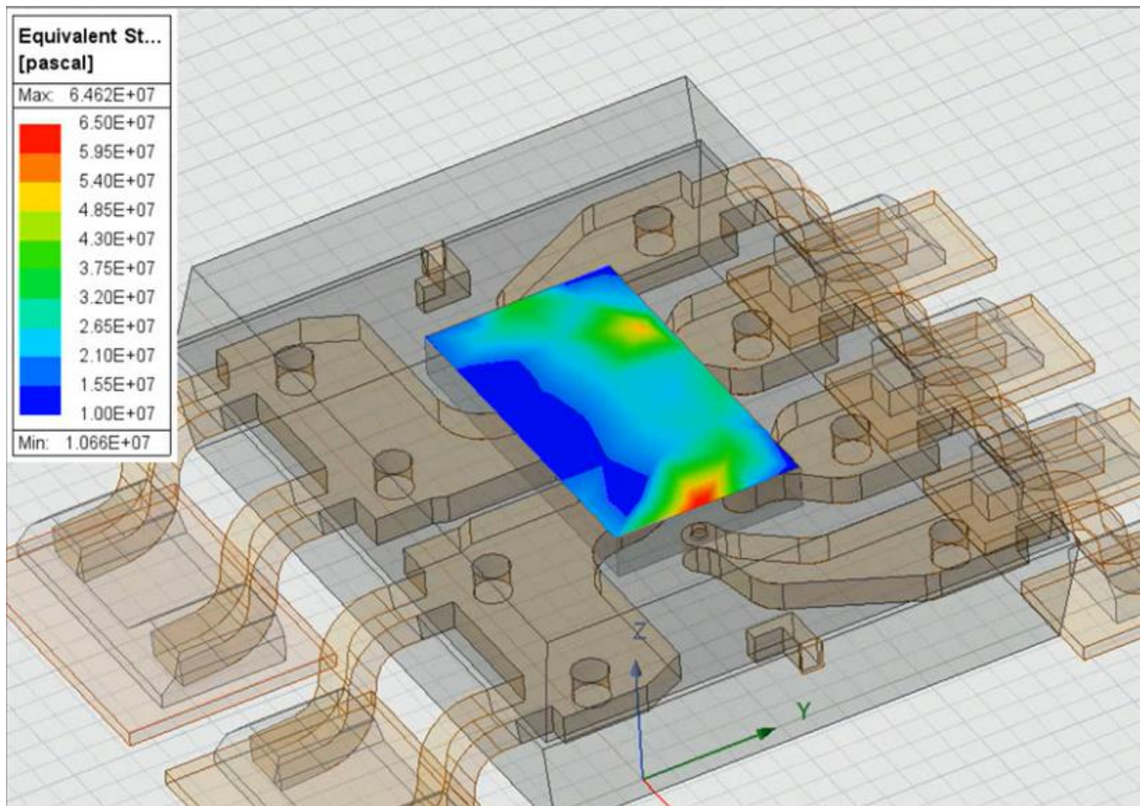


*Figure 67: Equivalent stress on the upper face of the die*

# 18. Package's thermal upgrades

Results from previous chapters show how temperature is dissipated across the die, across the whole package, and across the whole system. When a high load current is flowing through the current loop, the system is heating up and temperature distribution is due to some previous simulations far away from the ideal.

In this chapter, I tried to design upgrades that can provide lower temperatures on the die or whole chip. Another goal is to achieve better heat dissipation. These upgrades were designed regardless of the increased production cost per piece and except section18.4, only DC current was considered. The simulation conditions here are the same as in the sections 12 and 13. The used PCB is previously simulated TED-0004110.

## 18.1. Package with a heatsink

The first upgrade that I simulated is adding the basic heatsink on the top of the chip. The heatsink should have dimensions similar to the chip itself to fully cover it. The size of the used heatsink is the smallest that I found available. The size of the heatsink's base is 6.3 x 5 x 1 mm. The heatsink has 4 fins and the overall heigh is 4.8 mm. The heatsink is connected to the top of the chip. This upgrade should provide better cooling of the chip (especially of the epoxide) during natural convection. The model of this upgrade is in Figure 68 and the complete simulation model in Figure 70.

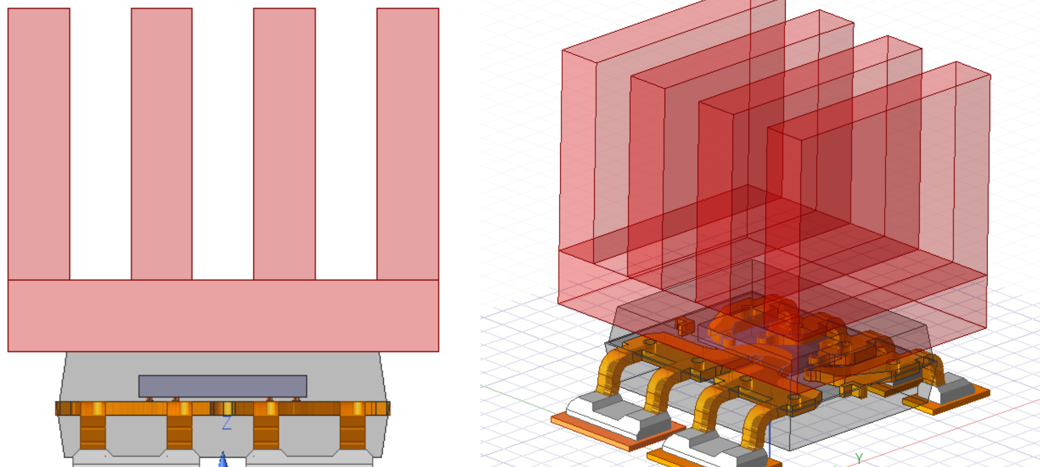

*Figure 68: The package upgraded with a basic heatsink above*

### 18.1.1. Simulations results – Icepak

In this section, I will demonstrate thermal simulations only, because losses in the package or in the wires are the same as in section 12. The model of the package is placed in the same system and the upgrade does not affect DC solutions, only thermal simulations.

Although the heatsink is quite small sized, it helps the natural convection to cool down the epoxide and so the die. The results can be seen in the figures shown below. The temperature on the die is reduced by approximately 5 °C. Gradient over the die is not affected by this solution. The most important result of this solution is the temperature on the die which can be seen in Figure 69. The next interesting result is the temperature distribution over the package which shows the impact of the connected heat sink. This is visible in Figure 71.

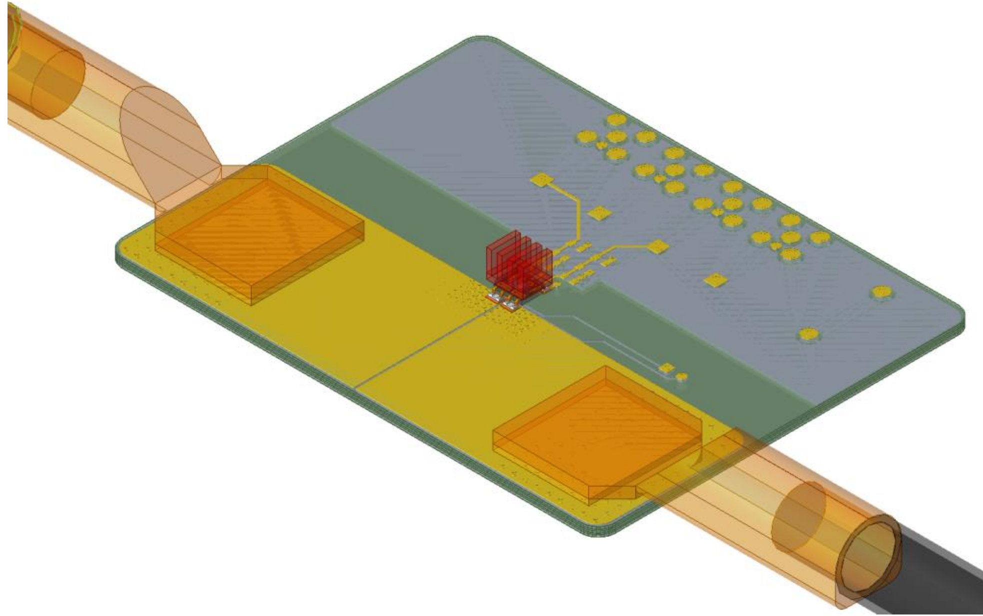

*Figure 70: Connected system with the heatsink upgrade*

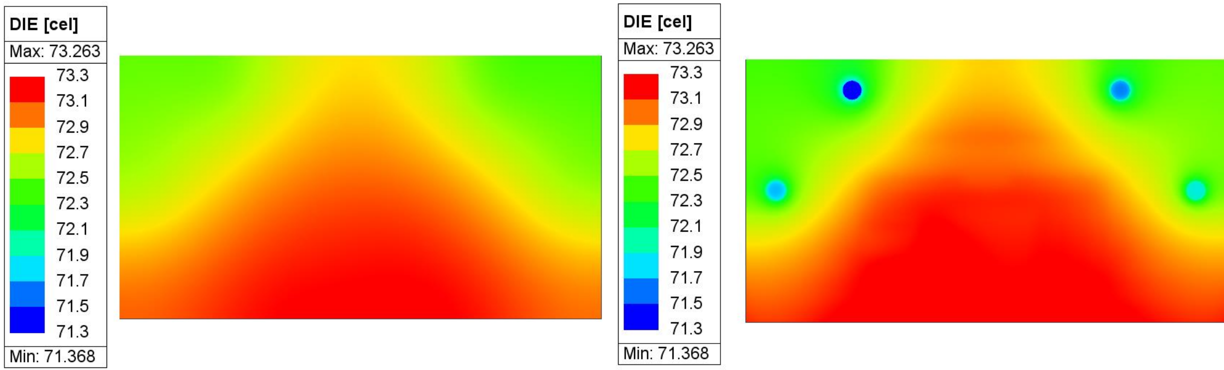


*Figure 69: Temperature distribution over the die in the system with connected heatsink*

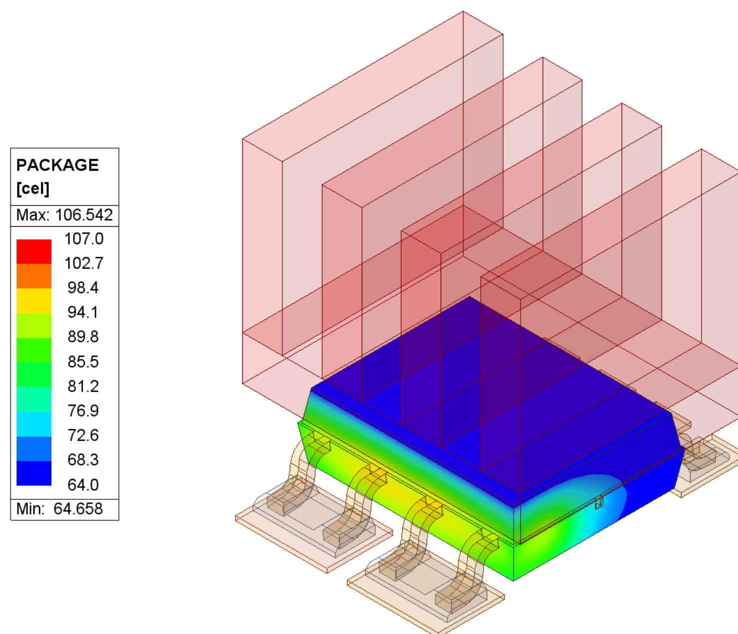


*Figure 71: Temperature distribution over the package with connected heatsink*

## 18.2. Package with a heatsink directly connected to the die

This chapter is an upgrade of the previous paragraph 18.1. The heatsink's size is the same as in the previous chapter, but it is connected directly to the chip's die. This means that above the die there is a small layer of TIM (Thermal Interface Material), which is a material with low electrical conductivity but high thermal conductivity. The TIM is connected to the copper plate above the die, which is used here as a thermal conductor or a thermal spreader. This conductor is connected to the heatsink on the top of the chip. So, the heat can flow directly from the die to the heatsink a dissipate to the surroundings. This upgrade is visible in Figure 72.

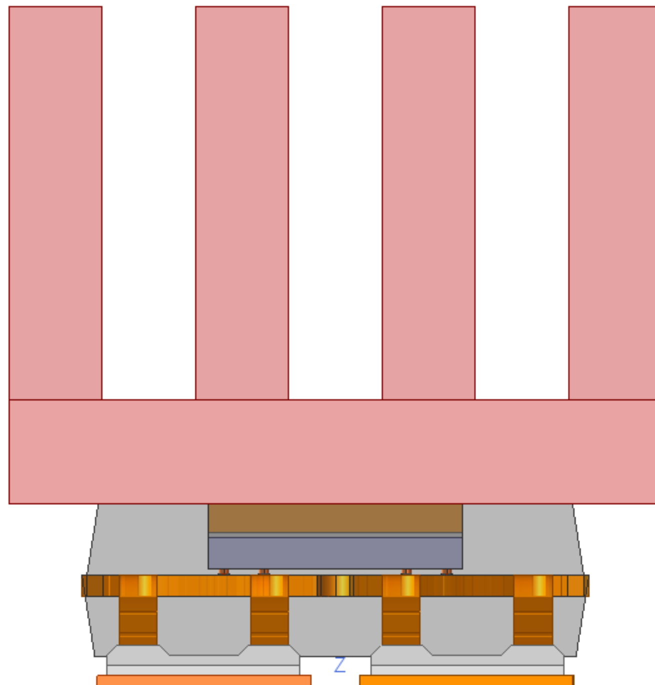

*Figure 72: The package upgraded with a heatsink connected directly to the die with a TIM and heat spreader*

### 18.2.1. Simulations results – Icepak

As in 18.1.1, only thermal simulations will be observed due to the same reason as in the previously mentioned chapter. According to the direct connection of the heatsink to the die, this solution gives better results than a solution with only a basic heatsink in section 18.1.

The temperature on the die decreases over 10 degrees Celsius, so the maximal temperature on the die is 67.3 °C. What is even more interesting, the temperature gradient over the die decreases either. Due to the TIM material and the spreader temperature distribution over the die is different from the other simulations because it is more uniform. The total gradient decreased about 1.6 degrees Celsius to 2.5 °C. And so, the minimal temperature on the die equals 64.7 °C.

Figures below show some obtained results. Remarkable is the previously mentioned temperature distribution over the die visible in Figure 73. The next interesting plot is the temperature over the package, which is modified from the previous simulations. This is visible in Figure 74 and Figure 75. Some other results can be seen in Appendix.

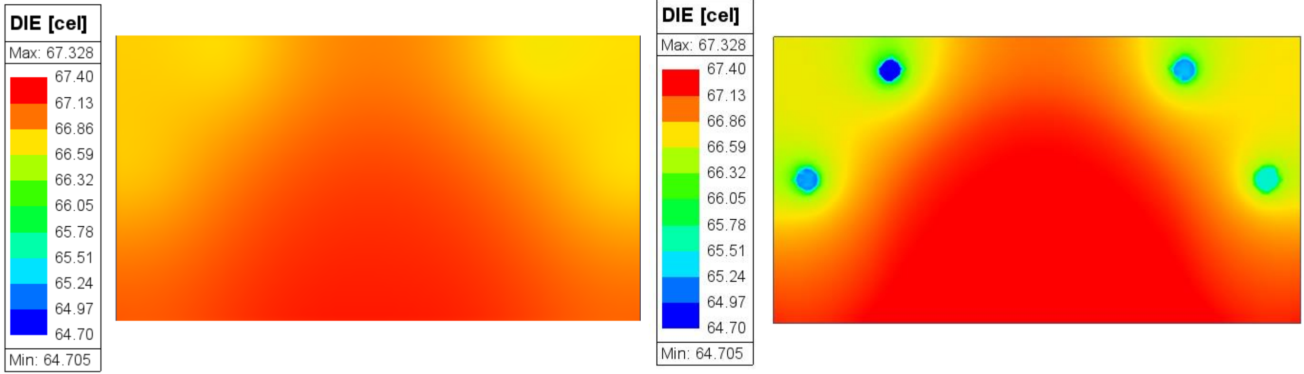


*Figure 73: Temperature distribution over the die, top view (left), bottom view (right) - upgrade with heatsink, TIM and heat spreader*

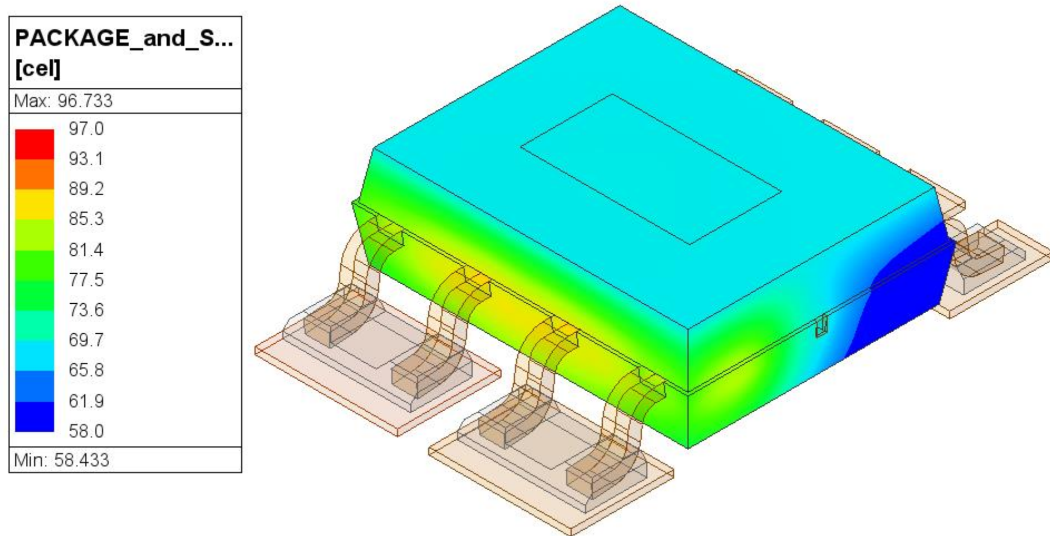


*Figure 74: Temperature distribution over the package upgraded with a heat spreader*

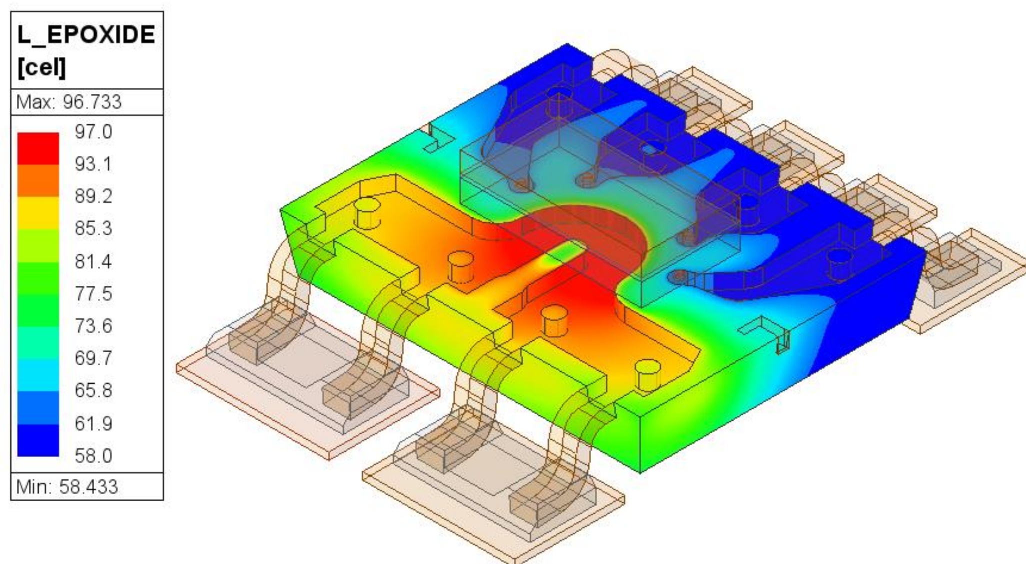


*Figure 75: Detailed view of the temperature distribution inside the package upgraded with a heat spreader*

## 18.3. Package with a thicker terminals

The upgrade described in this chapter comes from the idea of reducing Joule's heat in the current loop and so decreasing the temperature in the chip. The package used in the chapters above is SOIC- 8, the package with 8 terminals, where 4 of them create a current loop. To reduce resistance and so the Joule's heat, terminals are connected. The current loop is thicker, and the resistance is lower. This is visible in Figure 76.

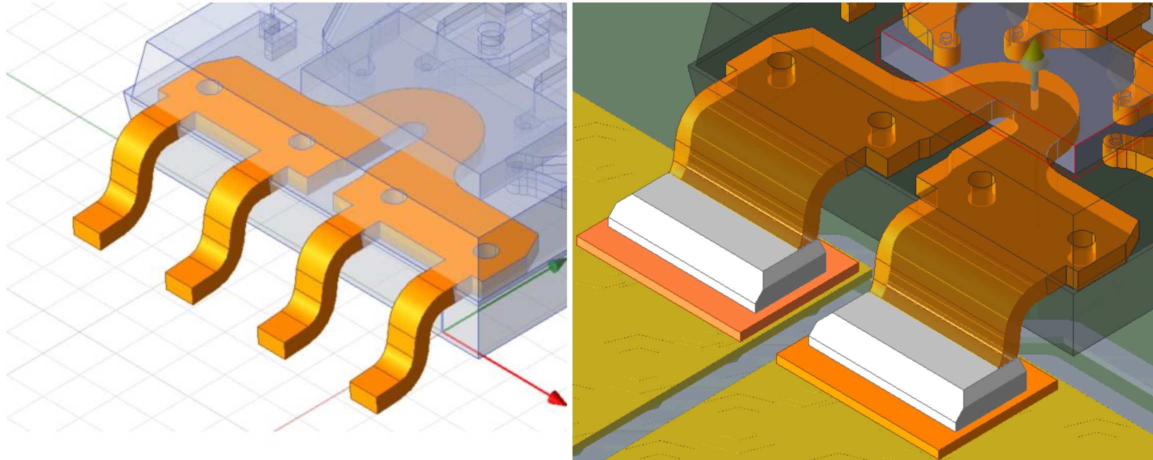

*Figure 76: Standard current loop (left) versus upgraded thicker current loop (right)*

### 18.3.1. Simulations results – Maxwell

The results of the simulations of this upgrade are satisfying. According to the lower ohmic resistance of the primary current loop, the losses in the solid are also lower. This can be seen in the results from the Maxwell solver. Total computed losses in the solid equal $\boldsymbol{P_{\mathrm{solid}}} = \mathbf{1.62\ W}$. This is a significantly lower number than by the basic current loop in section 12.2.

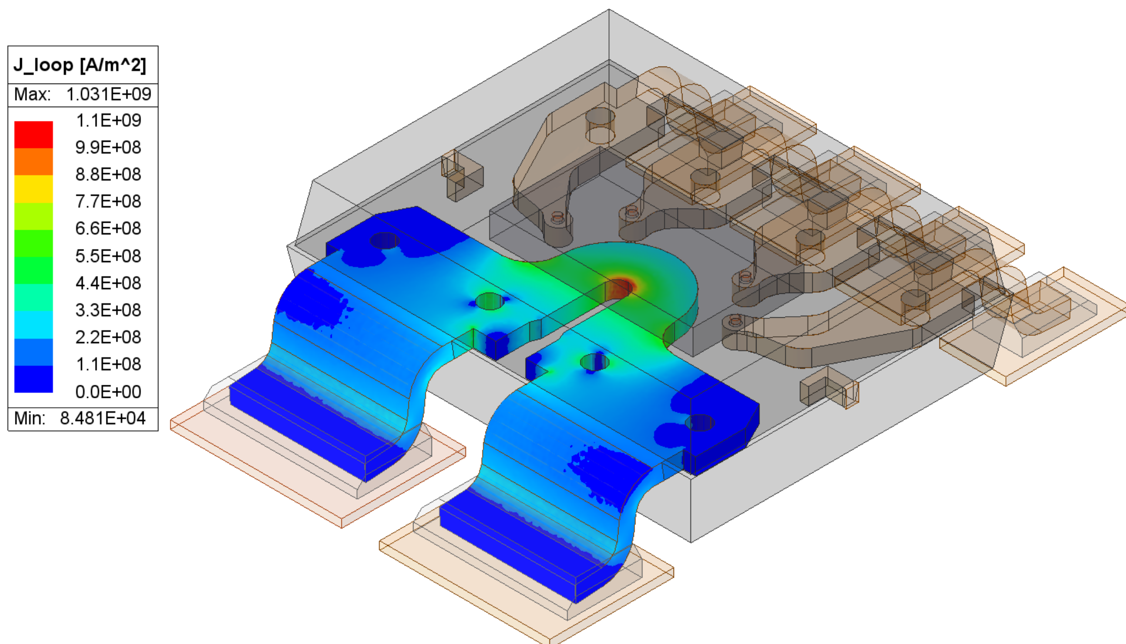


*Figure 77: Current density of the upgraded current loop*

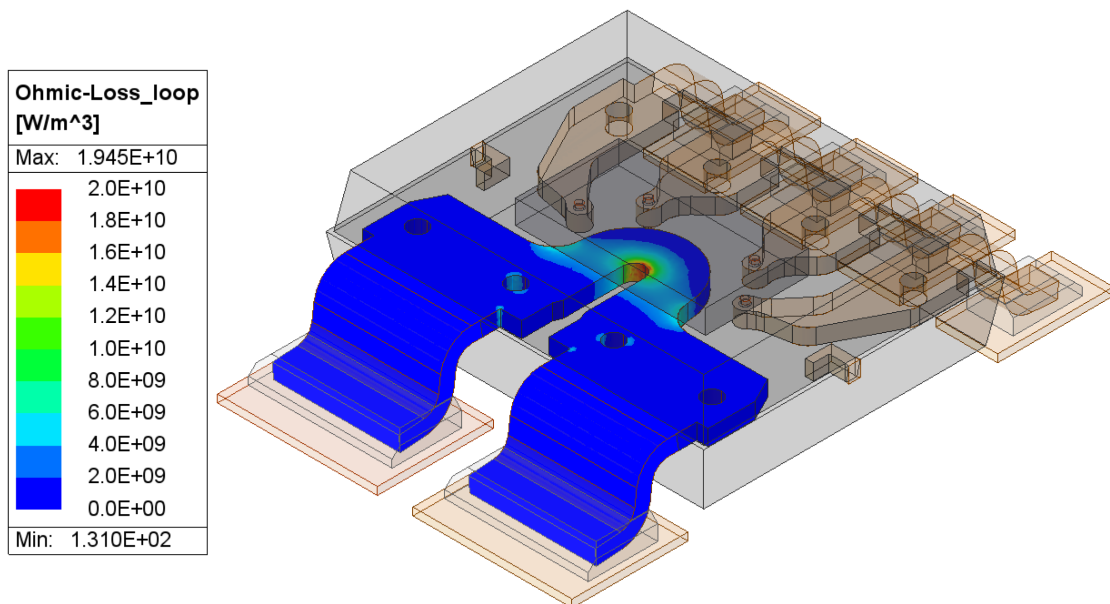


*Figure 78: Ohmic losses of the upgraded current loop*

Current density is visible in Figure 77 and losses are visible in Figure 78. The maximal simulated current density equals $J_{\mathrm{MAX}} = 1.03 \times 10^{9}\ \mathrm{A/m^2}$. Maximal simulated ohmic losses on the visualization equal $P_{\mathrm{MAX}} = 1.95 \times 10^{10}\ \mathrm{W/m^3}$. In comparison to the results calculated in section 12.2, all the mentioned results show improvement in the parameters. Therefore, thermal simulations were done, and the results are shown below.

### 18.3.2. Simulation results – Icepak

Thermal simulation results show an interesting function of the proposed upgrade. Due to the lower losses in the current loop, the total temperature is also lower. The next figures show important findings, and some more are shown in the Appendix section.

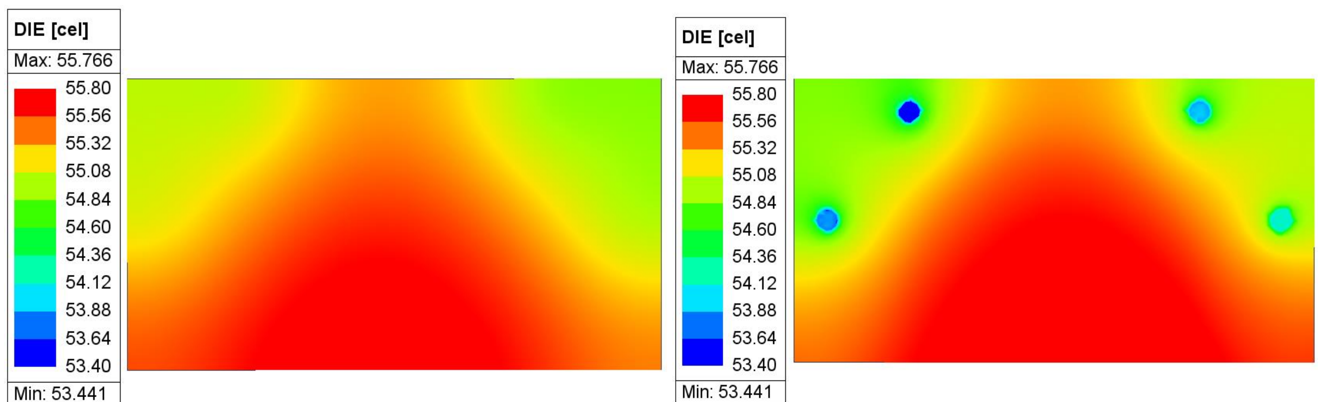


*Figure 79: Temperature distribution over the die in the upgraded package*

Figure 79 shows the temperature distribution over the die in the package with the upgraded current loop. The absolute temperature is significantly lower than simulated in 13. Also, the temperature gradient is lower. Nonetheless, the distribution has a similar shape.

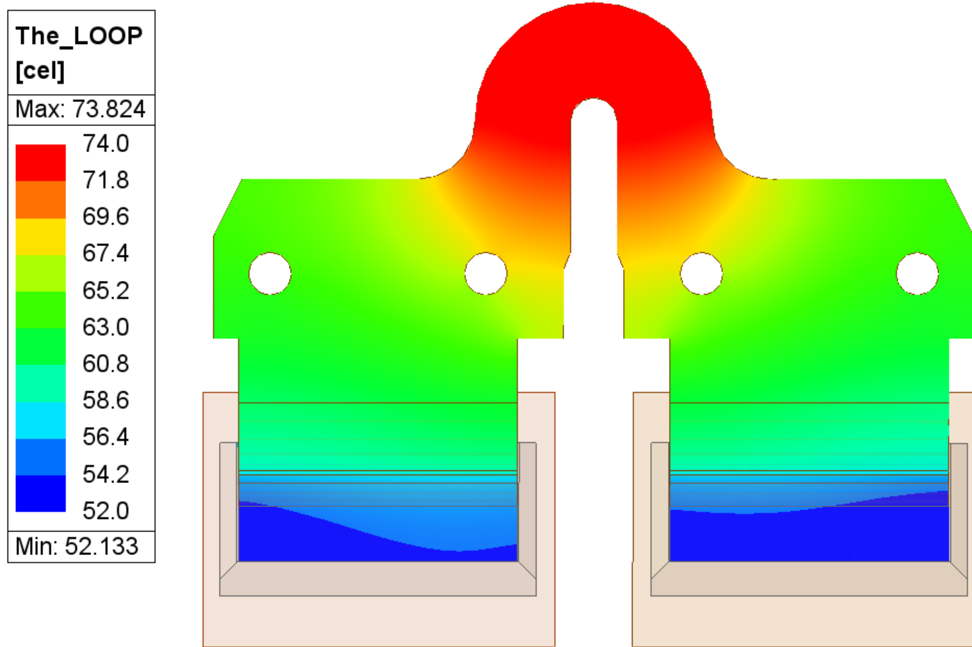


*Figure 80: Temperature distribution over the upgraded current loop*

In previous Figure 80 it is visible, that the temperature is also significantly lower than in section 13.3.2. Also, next figures show improvement in all aspects. Therefore, I find this solution to be functional.

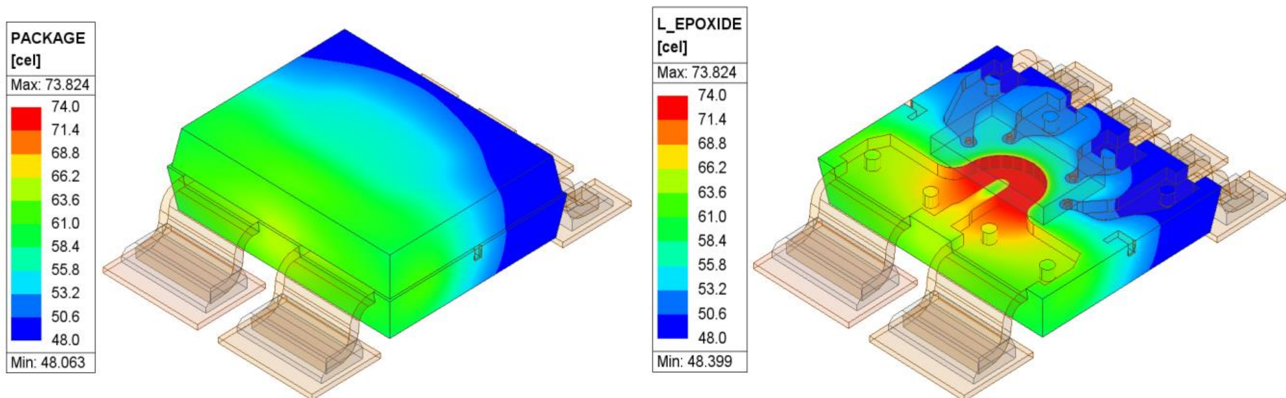


*Figure 81: Temperature distribution over the package (left) and detailed view on the temperature distribution in the package (right)*

In the Appendix section can be seen some other results from the simulations, for example velocity of the moving fluid around the system or the temperature on the supply wires.

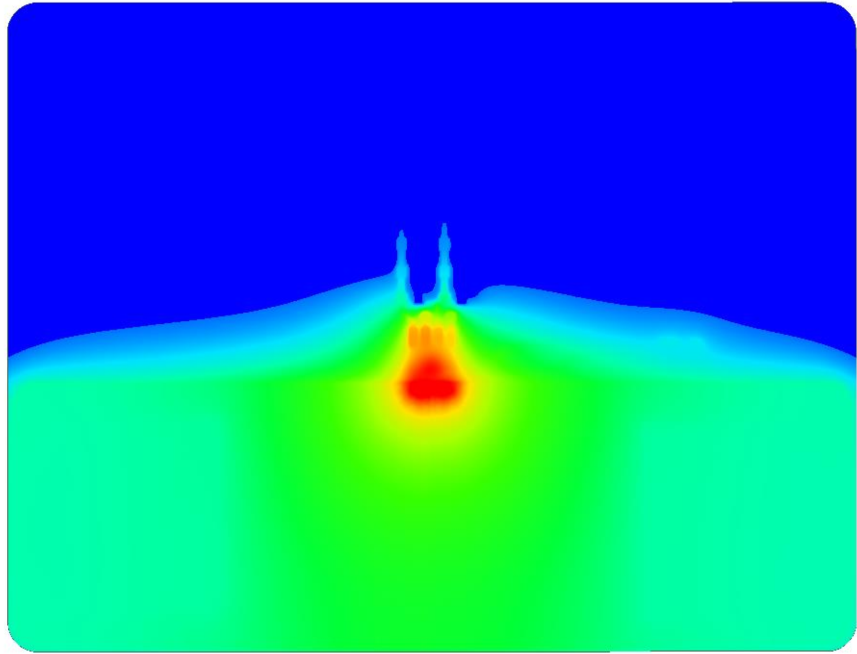


*Figure 82: Temperature distribution over the PCB TED-0004110 with upgraded package with the thick terminals*

## 18.4. Package with lead frame adjusted to the possible skin effect

The idea to create this chapter came from the knowledge about multi-strand wires. The skin effect here is lower than by single-line wires. It is a similar principle to the usage of the insulated sheets by the transformer design. The current loop is divided into many sheets insulated with a small air gap which are connected in parallel. The disadvantage is that the dividing loop into insulated sheets results in the lower thickness of the copper and so higher resistance and losses by the DC current. On the other hand, the advantage should be reduced losses caused by the skin effect on the high frequencies. The current loop is visible in Figure 83.

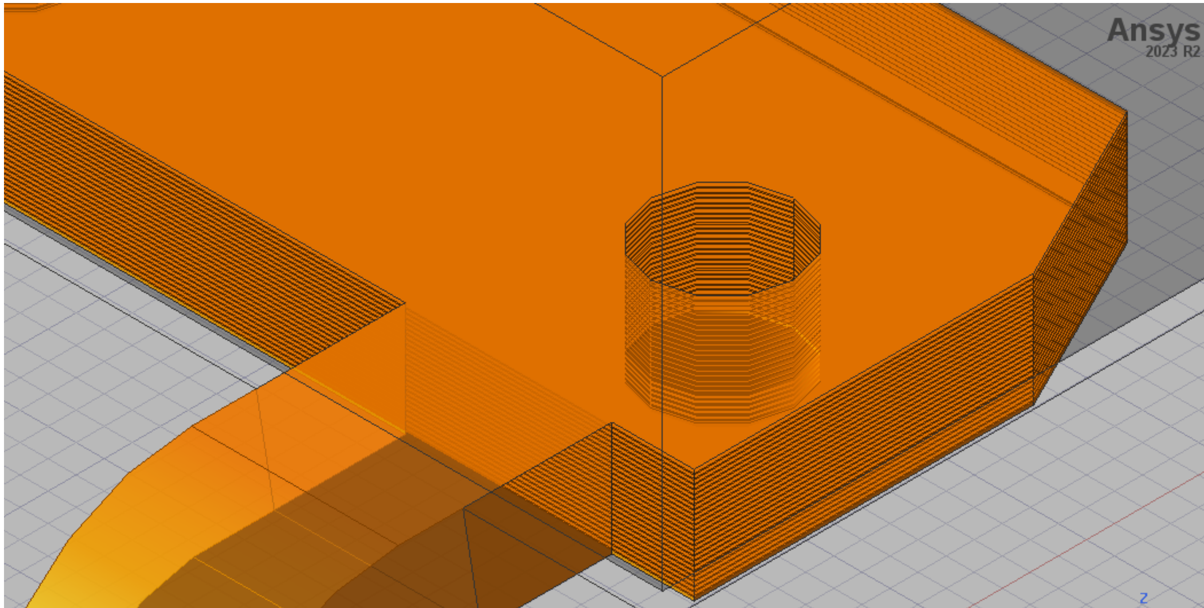


*Figure 83: The detailed view of the current loop divided into the copper sheets*

### 18.4.1. Simulations results

According to the lower mass of the copper in the current loop in comparison to the current loop from the basic package simulated in 12.2, DC losses are higher because the ohmic resistance is higher. However, this upgrade aims to the AC simulations. Also, it is important to consider if the decrease in the losses in the AC simulations and a small increase in the losses in the DC simulations is advantageous.

This type of device is used to measure current with a frequency of up to 300 kHz. The simulation shows that there is no skin effect on this frequency. So, this upgrade is nonsense for

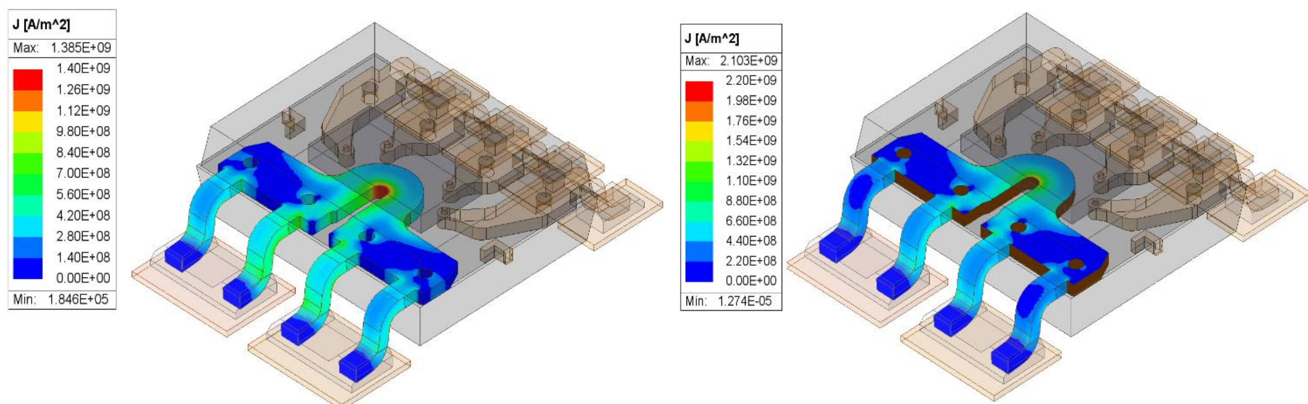


*Figure 84: Current density in the basic package (left) versus in the upgraded package (right)*

this application. However, the next figures show a comparison of the current density and the ohmic loss between the basic package and the upgraded package. As visible, both losses and current density are higher, and computed losses are higher: $\boldsymbol{P_{\mathbf{basic}}} = \mathbf{1.30\ W}$ vs $\boldsymbol{P_{\mathbf{upgraded}}} = \mathbf{1.48\ W}$.

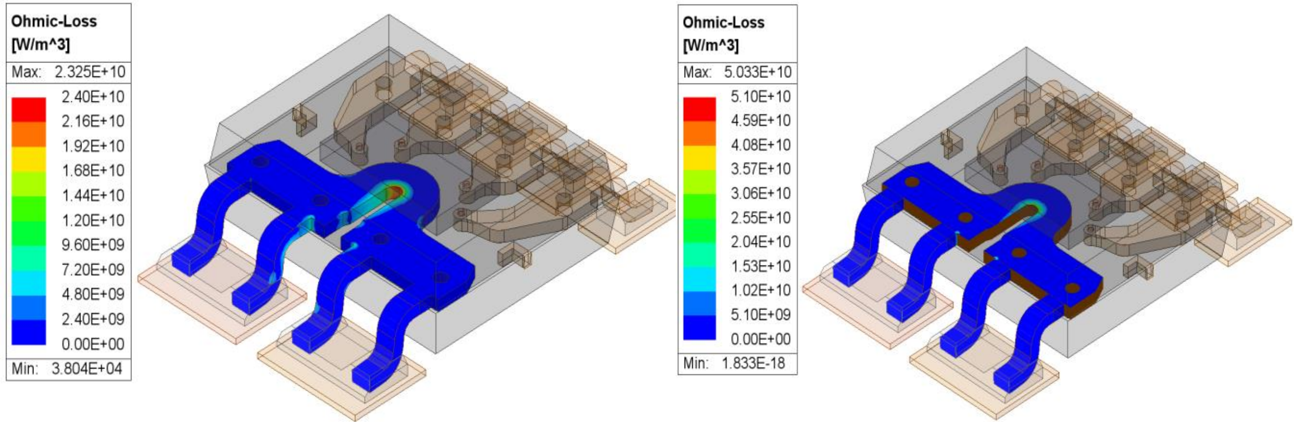


*Figure 85: Ohmic loss in the basic package (left) vs ohmic losses in the upgraded package (right)*

Nonetheless, I tried to simulate this upgrade on the higher frequency of 5 MHz which is the frequency at which chips with such technology still can be used. Figure 86 shows the visible skin effect in the current loop in the cut plane. Unfortunately, the idea of using this upgrade is not working as expected. The losses in the upgraded package are still higher: $\boldsymbol{P_{\mathbf{basic}}} = \mathbf{3.98\ W}$ vs $\boldsymbol{P_{\mathbf{upgraded}}} = \mathbf{4.48\ W}$. Therefore, I decided not to do thermal simulations.

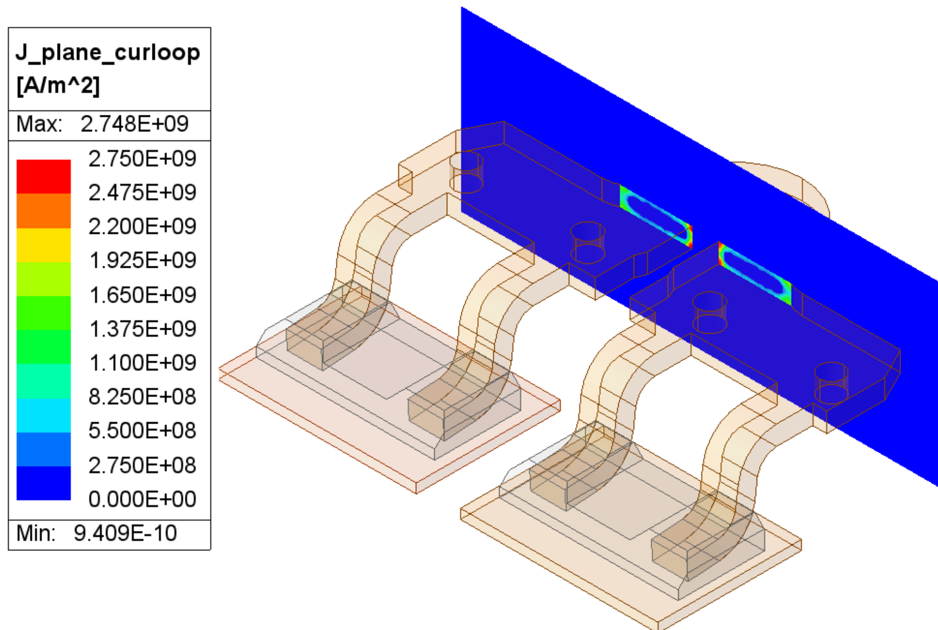


*Figure 86: Skin effect in the basic current loop*

# 19. Conclusion

In this thesis research was carried out on the topic of the multiphysics simulations of integrated circuits and whole systems. Specifically, about integrated current sensors. The motivation for multiphysics simulations was discussed as a part of the research. Next were discussed types of heat transfer concerning the integrated circuits, PCBs, and Joule's heating. Types of the current sensors were briefly described, and the Hall effect-based method was described in more detail. Then used integrated circuit ACS37013 was introduced closely.

The next part of the research was dedicated to the topic of simulation and measuring. Multiphysics simulations were described, and available simulation programs were introduced. Then was described the 2-currents measuring method used to measure temperature on the die due to the voltage drop on the P-N junction. As a last part of the research, the topic of the possible upgrades to achieve better temperature dissipation was mentioned.

After the research, some assumptions were made that I wanted to achieve. In the next steps, the creation of the simulation model started. First, the PCB TED-0004110 was simulated in the Ansys SIwave solver. Here the losses in the PCB were calculated and the electrical solver SIwave was interwoven with the Icepak thermal solver with the coupling possibility. Therefore, the thermal approximation model of the PCB was created and implemented into the Ansys AEDT.

In the Ansys AEDT, a model of supply wires was created. The wires were 1 meter long with a cross-section of 70 mm$^2$ and were terminated with a ring terminal. The model of wires was simulated in the Ansys Maxwell tool. The load current was set to 50 A. Total computed losses were $P_{\text{solid-wires}} = 1.33$ W. Next, the model of IC ACS37013 was implemented into the Ansys AEDT and was also simulated in the Ansys Maxwell tool. Total computed losses in the device were $P_{\text{solid-device}} = 2.12$ W.

After completing these simulations all parts were imported to the Ansys Icepak tool and connected into one complete system. The crucial parts of the whole system simulation were the precise setting of the mesh, the correct setup of the simulation, and defining the 2-way coupling between the electrical and thermal solvers. Then the simulation was set on the server due to the high computational demands. The results were presented in the form of a graphic display. Due to the point monitors temperature was calculated in the spots where the thermometers are placed. The temperature gradients were obtained. Temperature gradient over the die was $\Delta T_{\text{die}} = 4.1$ °C. The gradient between the thermometers on the die was calculated $\Delta T_{\text{thermometers}} = 1.8$ °C. Some other results were obtained and described e.g. the temperature over package, temperature on the primary current loop, or temperature on the PCB. The rest of the results were put in the Appendix section.

The same procedure was used for the different PCB – TED-0003528 which consists of 2 layers of copper and therefore has worse characteristics. PCB was simulated in the SIwave and put into the AEDT. Due to the worse parameters, the load current was decreased to 25 A. Therefore, the model of wires and model device were again simulated in the Maxwell tool. Obtained losses were $P_{\text{solid-wires}} = 0.32$ W and $P_{\text{solid-device}} = 0.53$ W. Then the system was connected inside the Icepak tool, and thermal simulations were made. As previously, the temperature gradients were obtained.

One section shows an alternative attempt of the simulation of the whole system. It differs from the ones mentioned above in the electrical simulations of the PCB. Here is the PCB simulated in the Maxwell tool and another input file is used. It was expected that the results would be more precise. Nonetheless, this solution turned out to be lengthy and unworkable and therefore I decided to leave it.

The next step was to provide measurements to confirm the simulation model or deny it. For measuring was used 2-current method which measures a voltage drop on the P-N junction according to the temperature. On the device's die 7 thermometers are placed and can be directly addressed. I made serval measurements for a few parts placed in the temperature chamber, then I calculated the average temperature on each diode and from where I could obtain an average temperature gradient.

For the PCB TED-0004110, the highest average temperature was $T_{\mathrm{MAX-TED-0004110}} = 79.9$ °C and the lowest was $T_{\mathrm{MIN-TED-0004110}} = 78.0$ °C. The obtained temperature gradient was $\Delta T_{\mathrm{TED-0004110}} = 1.9$ °C. These results are close to the simulated ones, even though the maximal simulated temperature is around 2 °C lower and the temperature gradient is lower around 0.1 °C. Therefore, I accept this measuring as confirmation of the model.

For the PCB TED-0003528, the highest average temperature was $T_{\mathrm{MAX-TED-0003528}} = 48.2$ °C and the lowes was $T_{\mathrm{MIN-TED-0003528}} = 46.7$ °C. The obtained temperature gradient was $\Delta T_{\mathrm{TED-0003528}} = 1.5$ °C. These results are close but differ more from the previous simulations. The absolute maximal simulated temperature differs by around 5.7 °C, which is still a good result, but the difference in the temperature gradient is around 0.2 °C. This result is already on the verge. Even though this PCB was not designed for this device and some issues due to soldering or to the bad connection of the wires may have occurred during measuring. Due to these circumstances, I accept this measuring as a confirmation of the model.

According to the results of the simulations and the measuring is obvious that the model with the PCB TED-0004110 is better. The results are more precise and due to the measurements, the real function is also better.

A short section is dedicated to mechanical simulations. According to the obtained losses and the calculated heat the mechanical behavior of the parts can be observed. Simulation shows 2 interwoven results: displacement and stress. The maximal displacement of the package was simulated to $\Delta \mathrm{L} = 33.17\ \mu\mathrm{m}$. The highest simulated stress on the die was around the copper pillars and equals $\mathrm{Stress} = 918\ \mathrm{MPa}$.

The last section of the thesis shows designed modifications of the package to achieve better thermal parameters of the system. First, the basic heatsink is used to help natural convection. This solution brought a reduction in temperature approx. by 5 °C and better cooling of the epoxide. The second upgrade is a die directly connected to the heatsink via TIM and heat spreader. This solution shows a significant reduction of the temperature on the die and also a lower gradient. Interesting is the more homogenous distribution of the temperature over the die. The third improvement of the package consists of widening the terminals to reduce electrical resistance and so Joule's heating. This solution brought a significant reduction of the temperature over the die and in the temperature gradient. The temperature reduction was also reflected in the temperature of the whole system. The last simulated upgrade was an attempt to reduce possible skin-effect which theoretically will increase total losses. Nonetheless, this solution was not successful.

Due to all the results described in this section, the best way to realize the whole system would be in this way. The used PCB should be the six-layer TED-0004110. The used device should be a combination of the upgrades shown in sections 18.2 and 18.3 – package with a heatsink connected directly to the die and an upgraded lead frame of the current loop with the thicker terminals.

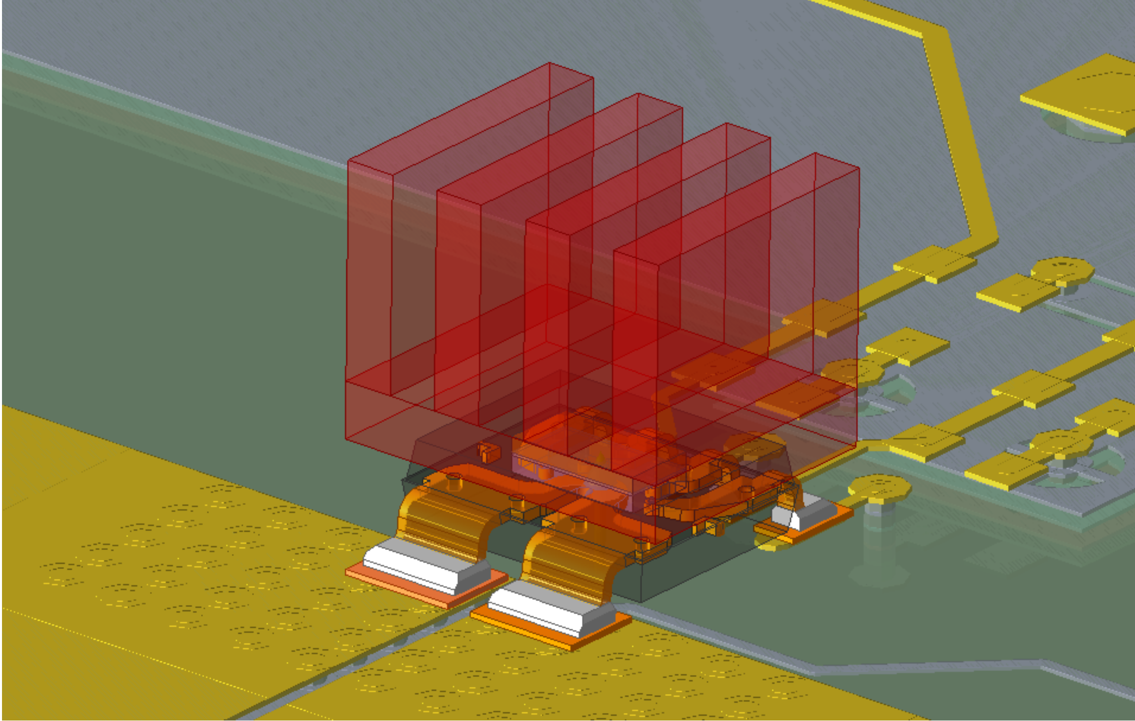

*Figure 87: Design of the ideal model based on the results of the Conclusion (not simulated)*

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# Appendix

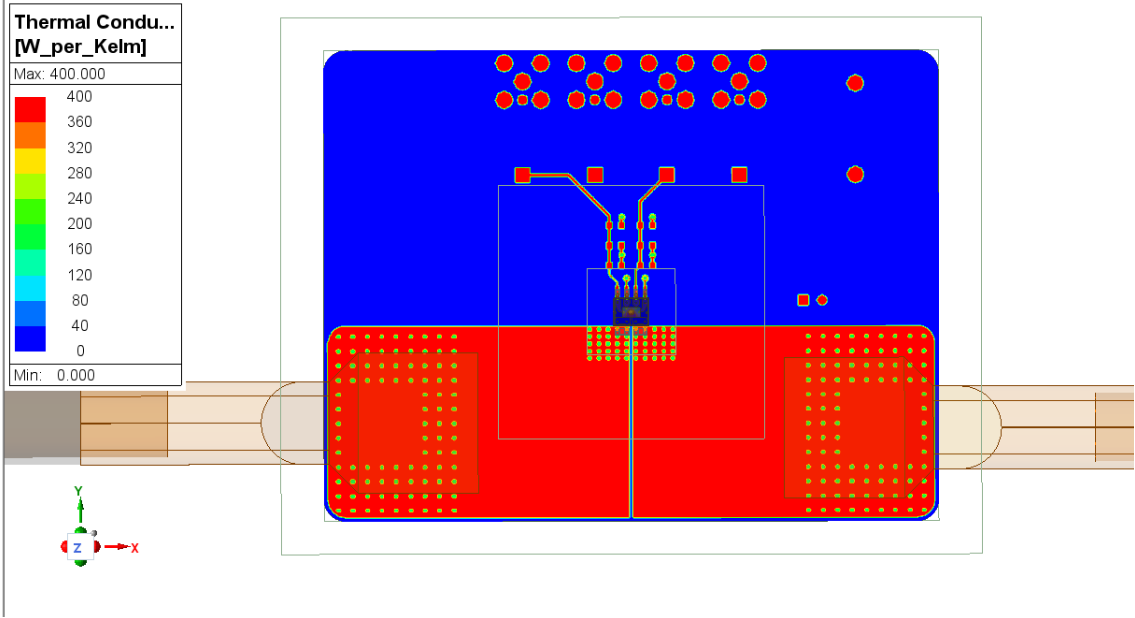


*Figure 88: Thermal conductivity of the TED-0004110*

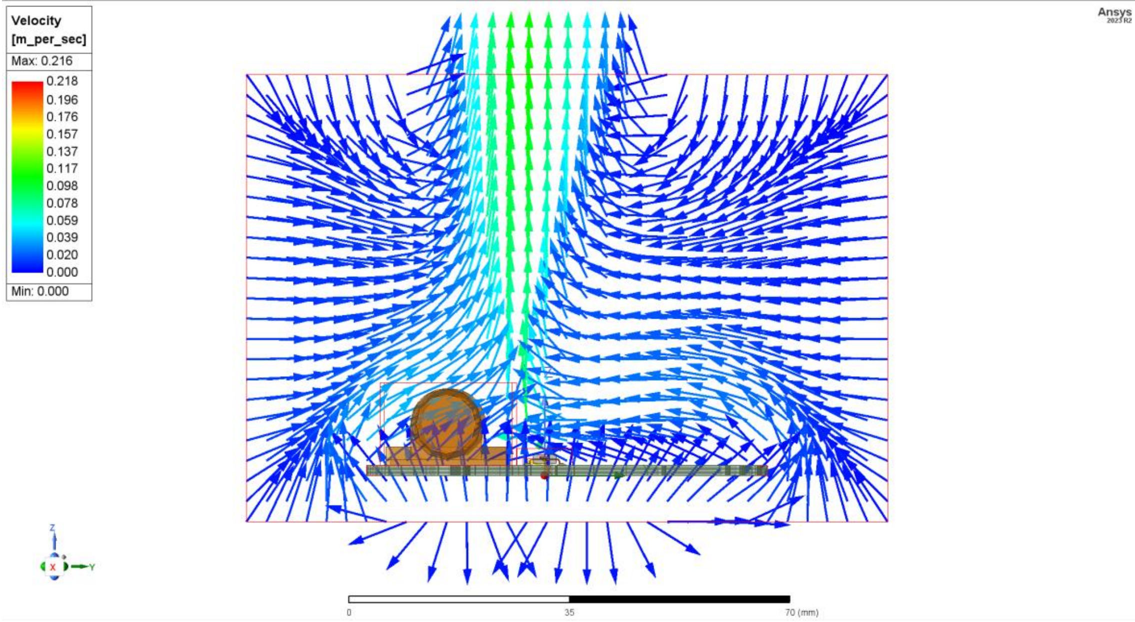


*Figure 89: Velocity vectors showing movement of the fluid around the system during natural convection of TED- 0004110*

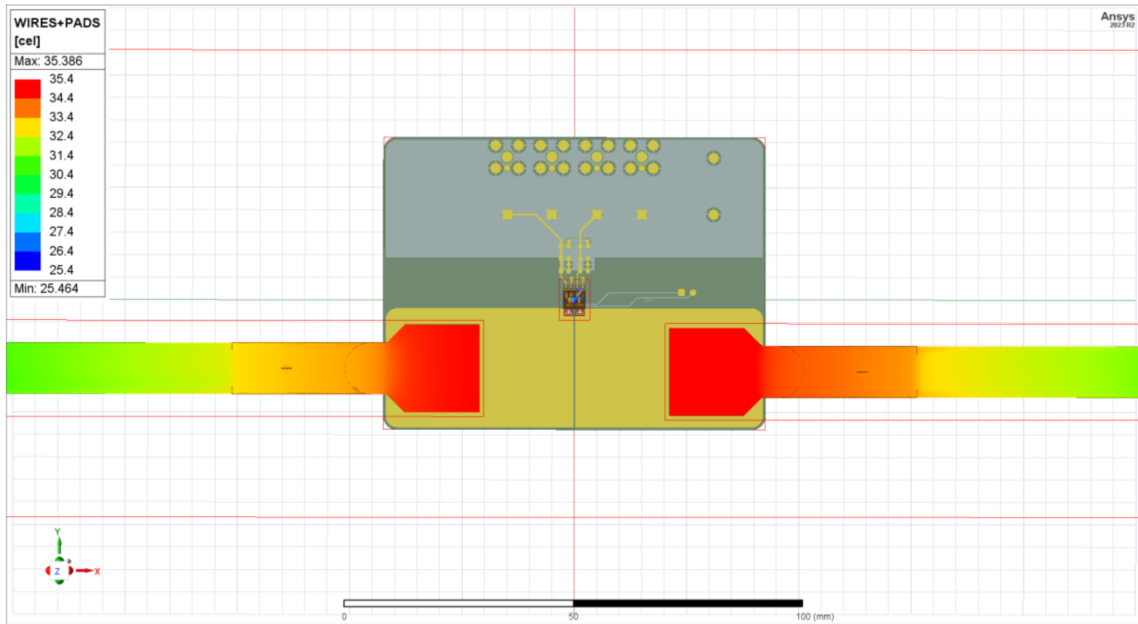


*Figure 90: Temperature visualization on the wires connected to the TED-0004110 in detail*

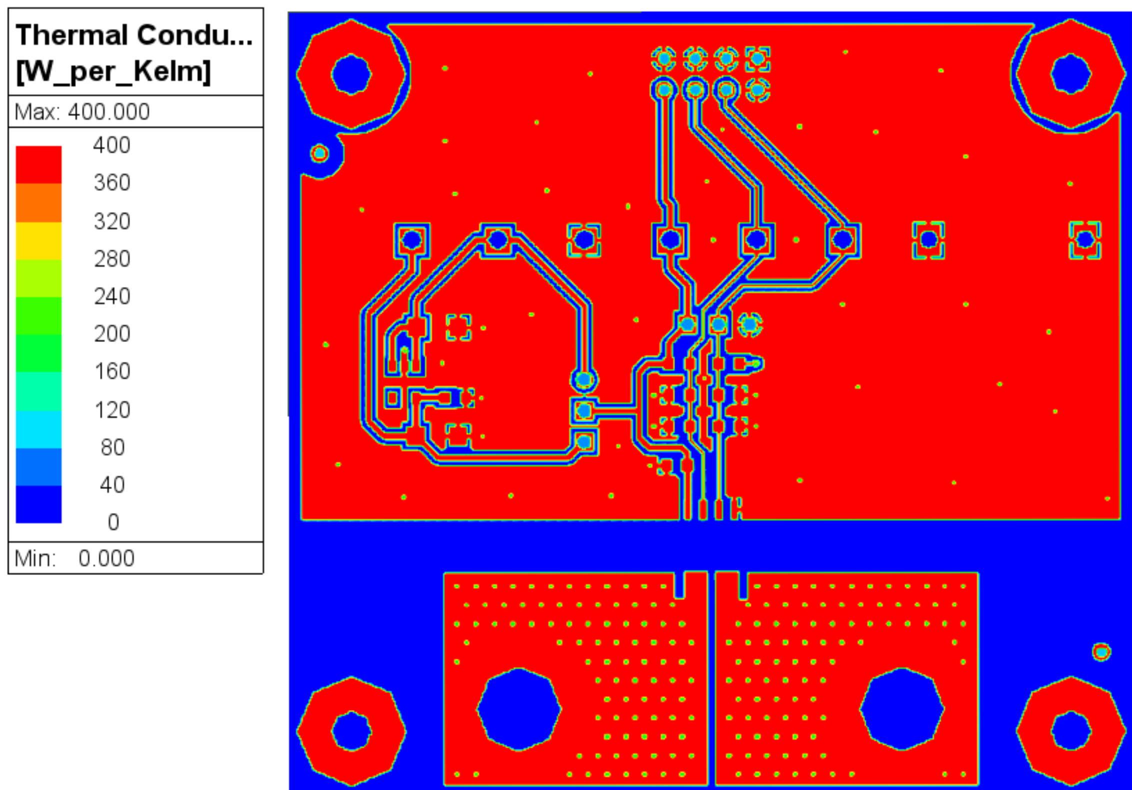


*Figure 91: Thermal conductivity of the TED-0003528*

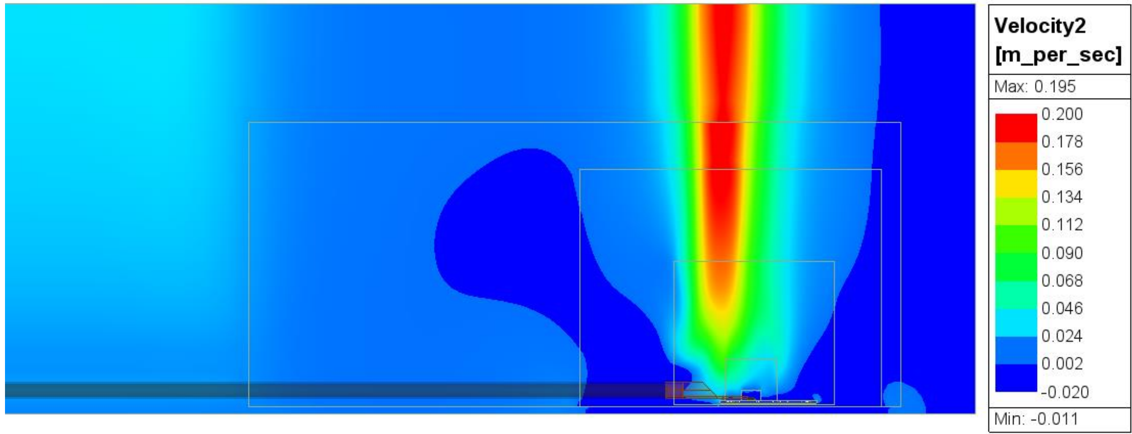


*Figure 92: Velocity visualization showing movement of the fluid around the system during natural convection of the TED-0003528*

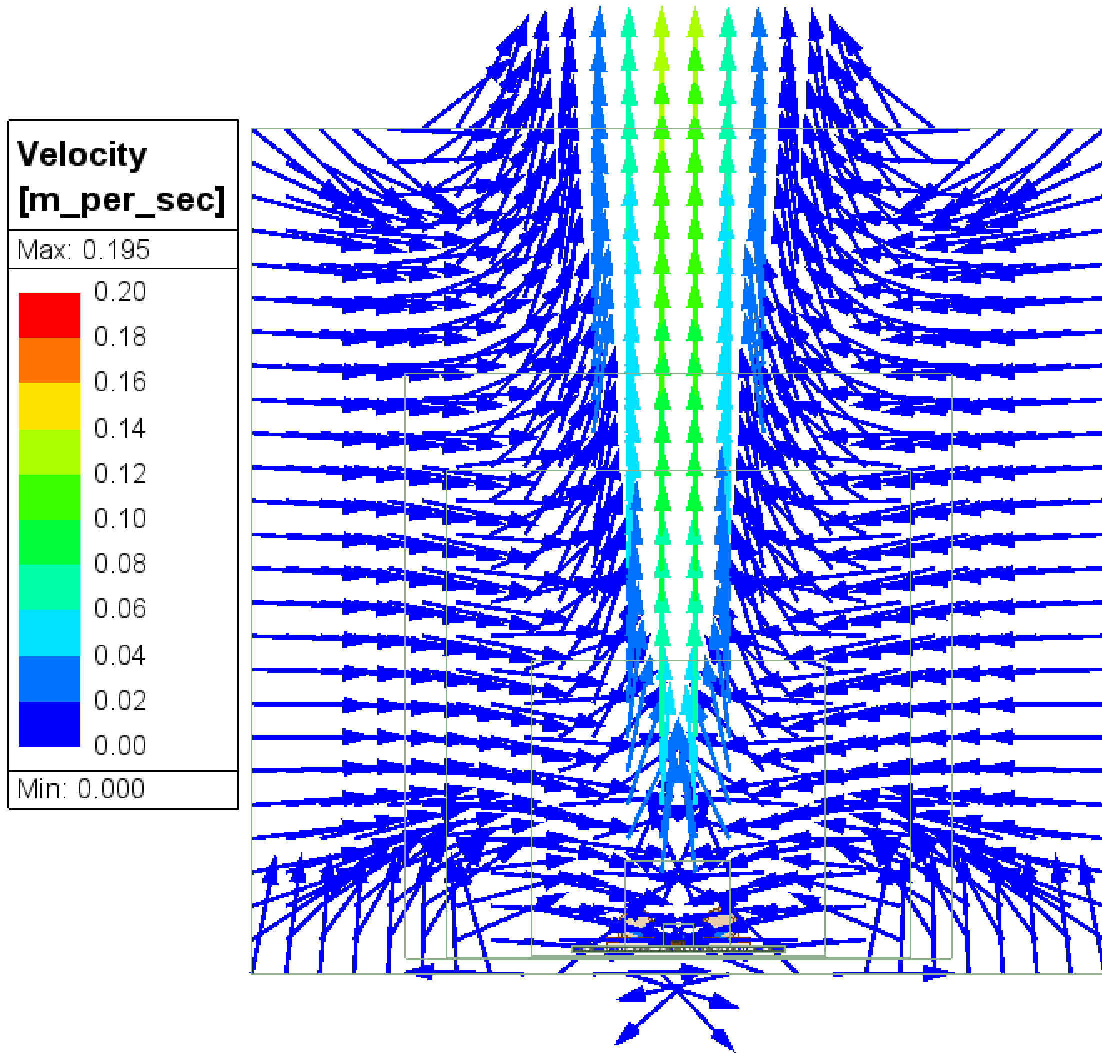


*Figure 93: Velocity vectors showing movement of the fluid around the system during natural convection of the TED- 0003528*

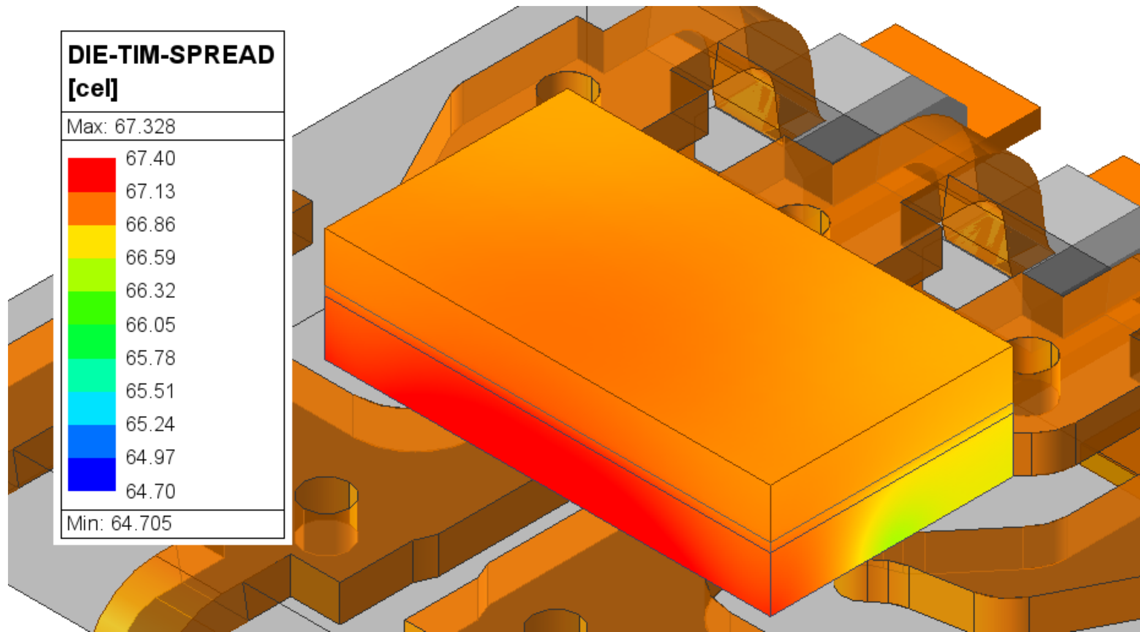


*Figure 94: Temperature distribution over the DIE-TIM-heat spreader structure*

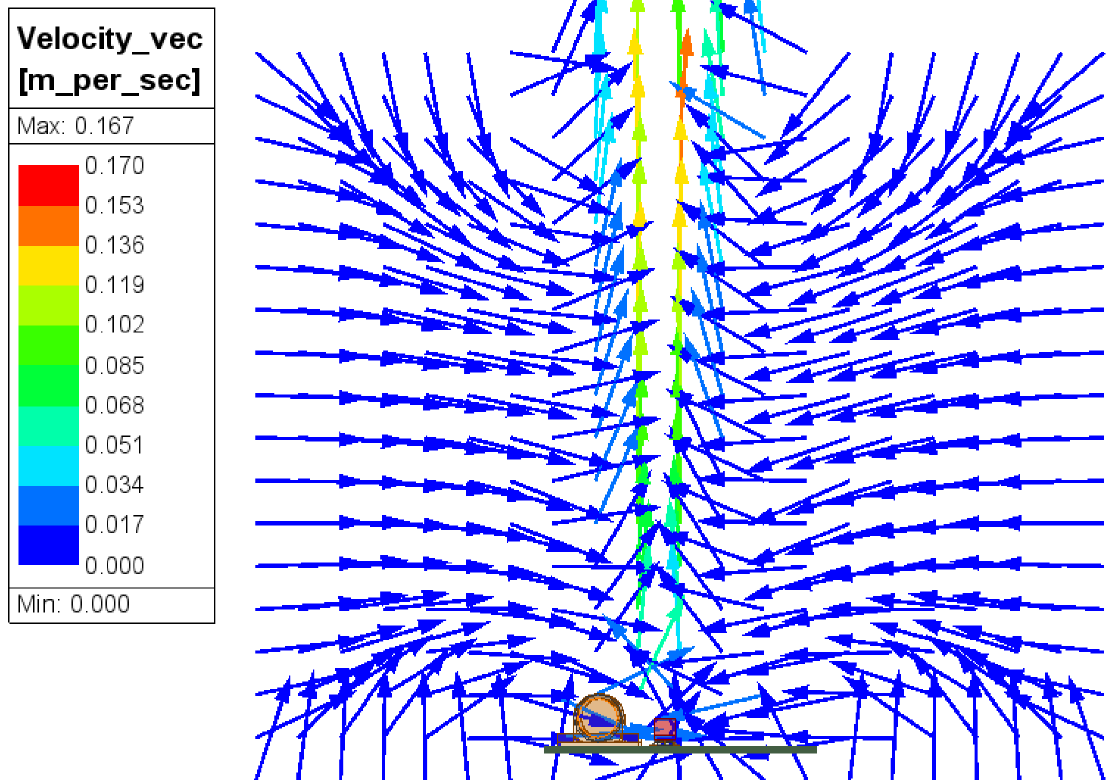


*Figure 95: Velocity vectors showing movement of the fluid around the system during natural convection of the upgraded package with heat spreader structure on TED- 0004110*

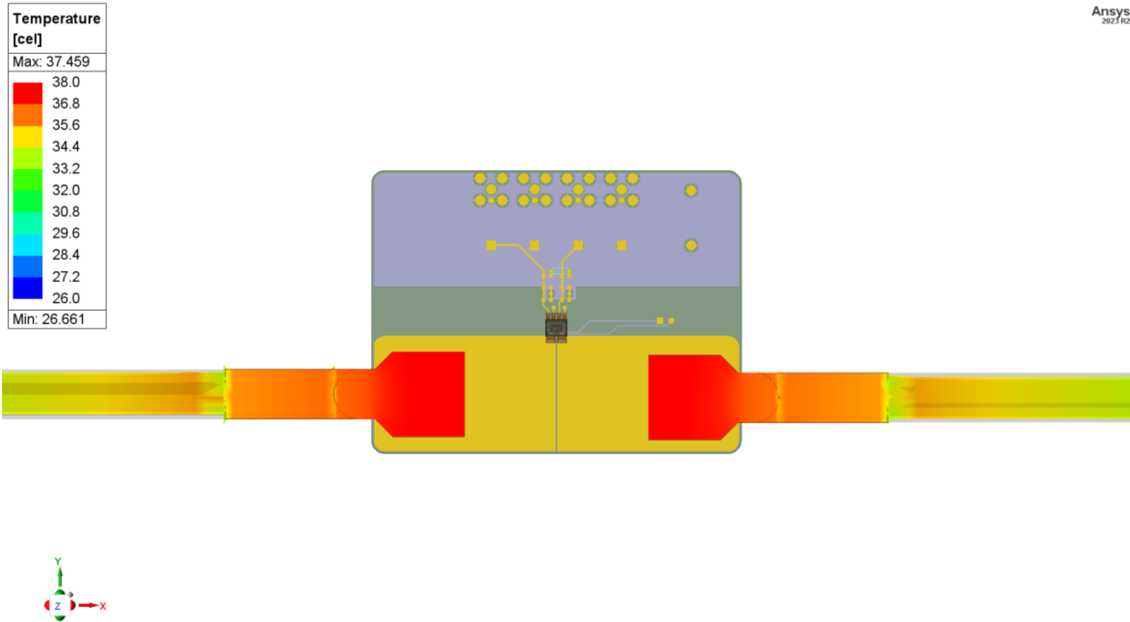


*Figure 96: Temperature visualization on the wires connected to the TED-0004110 with package with upgraded terminals in detail*

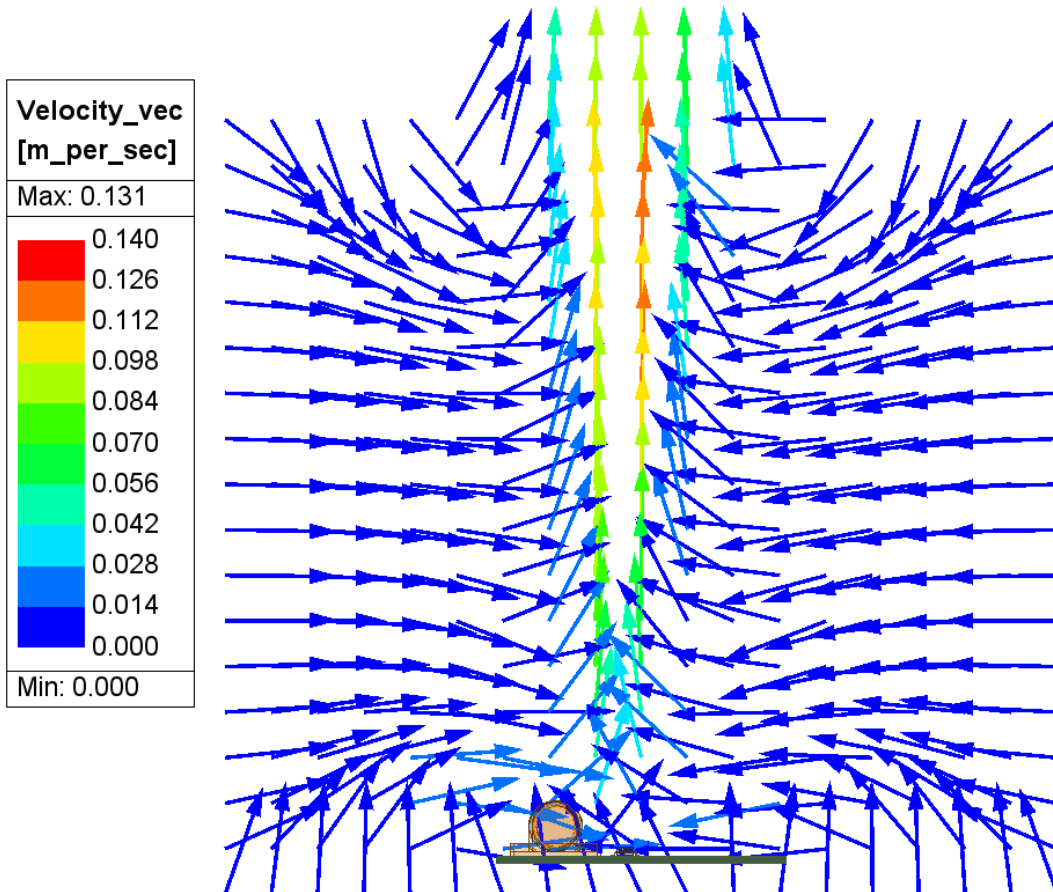


*Figure 97: Velocity vectors showing movement of the fluid around the system during natural convection of the upgraded package with thicker terminals on TED- 0004110*