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Doctoral Thesis

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IMPROVING THE ELECTRIC VEHICLE CONVERTER PERFOMANCE USING NEW SEMICONDUCTOR COMPONENTS

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Declaration

I hereby declare that I have written my doctoral thesis on my own and I have used only the literature listed at the end of the doctoral thesis in the references.

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Pavel Skarolek

Abstract

Semiconductor devices based on gallium nitride (GaN) are becoming to be used in power converters to increase the power density and improve the efficiency. Using the new technology of fast switching transistors in DC/DC converters and inverters brings new problems to be analyzed. The thesis covers complex area from GaN drivers design, cooling system, to minimizing losses in switch-on and switch-off state. Optimization of converter control algorithm achieved decrease of conduction losses caused by the current-collapse phenomenon. Additional optimum dead-time tracking algorithm decreased the losses caused by the transistor's reverse conduction region.

Keywords

Gallium nitride, GaN HEMT, gate driver, voltage source inverter, current-collapse, dead-time

Abstrakt

Součástky na bázi nitridu galia (GaN) pronikají do oblasti výkonových měničů a umožňují tak dosahovat vyšší hustoty výkonu a vyšší účinnosti. Použití nové technologie rychlých spínacích součástek v DC/DC měničích a střídačích přináší nové problémy, které je potřeba analyzovat. Práce se zabývá komplexní problematikou od návrhu driverů pro GaN tranzistory, jejich chlazení a snižováním ztrát v sepnutém a vypnutém stavu. Díky optimalizaci algoritmu řízení bylo možno dosáhnout snížení ztrát v propustném směru způsobených jevem „current-collapse“. Doplněním sledovacího algoritmu pro nalezení optimálního proměnného „dead-time“, byly sníženy ztráty způsobené vedením tranzistoru v závěrném směru.

Klíčová slova

Nitrid galia, GaN HEMT, budič gate, napěťový střídač, current-collapse, dead-time

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Abbreviations

2DEG	Two-Dimensional Electron Gas
BEV	Battery Electric Vehicle
CAN	Controller Area Network
CCM	Continuous Current Mode
DCM	Discontinuous Current Mode
DFF	Duty Feed Forward
EV	Electric Vehicle
FOC	Field Oriented Control
FR4	Flame Retardant glass-reinforced epoxy resin
GaN	Gallium Nitride
GIT	Gate Injection Transistor
HEMT	High Electron Mobility Transistor
ICE	Internal Combustion Engine
IGBT	Insulated Gate Bipolar Transistor
IMS	Insulated Metal Substrate
LCO	Lithium Cobalt Oxide battery
LFP	Lithium Ferro Phosphate battery
LMO	Lithium Manganese Oxide battery
LTO	Lithium Titanate Oxide battery
LUT	Look Up Table
MCU	Microcontroller
MDmesh	Multiple Drain mesh
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NCA	(Lithium) Nickel Cobalt Aluminium battery
NMC	(Lithium) Nickel Manganese Cobalt battery
PCB	Printed Circuit Board
PFC	Power Factor Correction
PHEV	Plug-in Hybrid Electric Vehicle
PLL	Phase Locked Loop
PMSM	Permanent Magnet Synchronous Motor
PWM	Pulse Width Modulation
RF	Radio Frequency
SiC	Silicon Carbide
SJ	Super-Junction MOSFET
SVPWM	Space-Vector Pulse Width Modulation
TO-247	Transistor Outline
VRB	Vanadium Redox flow Battery
VSI	Voltage Source Inverter
WoS	Web of Science

Nomenclature

C_{oss}	Output capacitance
D	Converter duty cycle
D_{MCU}	Microcontroller set duty cycle
d_a, d_b, d_c	Duty cycle of phase a, b, c
d_{limit}	Minimum duty cycle limit value
f_{sw}	Switching frequency
g_m	Device transconductance
i_a, i_b, i_c	Phase currents
i_α, i_β	Currents in α, β plane
i_d, i_q	Currents in d, q plane connected with rotor
i_{ch}	Channel current
i_{in}	Converter input current
i_{out}	Half-bridge output current
I_{Ltoff}	Reverse inductor current during off time
K	Clarke's transformation coefficient
P	Converter operating power
P_{cond}	Transistor conduction losses
P_d	Dissipated power
P_{out}	Converter output power
P_{sw}	Transistor switching losses
R_{DSon}	On-state resistance
R_{epi}	Epitaxial layer resistance
R_{ch}	Channel resistance
R_{sub}	Substrate resistance
R_{thcs}	Case to substrate thermal resistance
R_{thsr}	Substrate to radiator thermal resistance
R_{thjc}	Junction to case thermal resistance
$t_{d(rise)}, t_{d(fall)}$	Delay time of the rising and falling edge of the driver
t_{dt}	Dead-time duration
t_{on}	Transistor on time
T	Switching period
V_a, V_b, V_c	Phase voltages
$V_\alpha, V_\beta,$	Voltages in α, β plane
$V_d, V_q,$	Voltages in d, q plane connected with rotor
V_{BR}	Breakdown voltage
V_{DC}	Converter DC-link input voltage
V_{DS}	Drain to Source voltage
V_{GS}	Gate voltage applied from driver
$V_{GS(th)}$	Gate threshold voltage
V_{out}	Converter DC output voltage
V_{SD}	Transistor reverse voltage
$V_{GS(off)}$	Gate driver negative voltage in off state

1 Introduction

Electric vehicles were popular at the end of the 19th and beginning of the 20th centuries [1]-[4]. They were easy to operate, immediately ready to ride compared to early combustion engine vehicles and were clean. When the internal combustion engine was improved and the fuel became cheap and available around the year 1920, electric vehicles with battery storage practically became extinct except golf carts [2].

A problem with early electric vehicles existed regarding the low energy density of their lead-acid batteries, storing about 0.3 % of the energy of petrol for a given mass. The result of the low energy density was very short range, limited only to the inner city. With the growth of urban zones people needed long range vehicles which the then-current battery technology could not support [5].

In recent years the development of lithium-based cells leads to new electric vehicles (EVs) appearing on the market. From 2010 to 2021 6.8 million EVs (including hybrid vehicles) were sold worldwide according to [6] presented in Fig. 1.

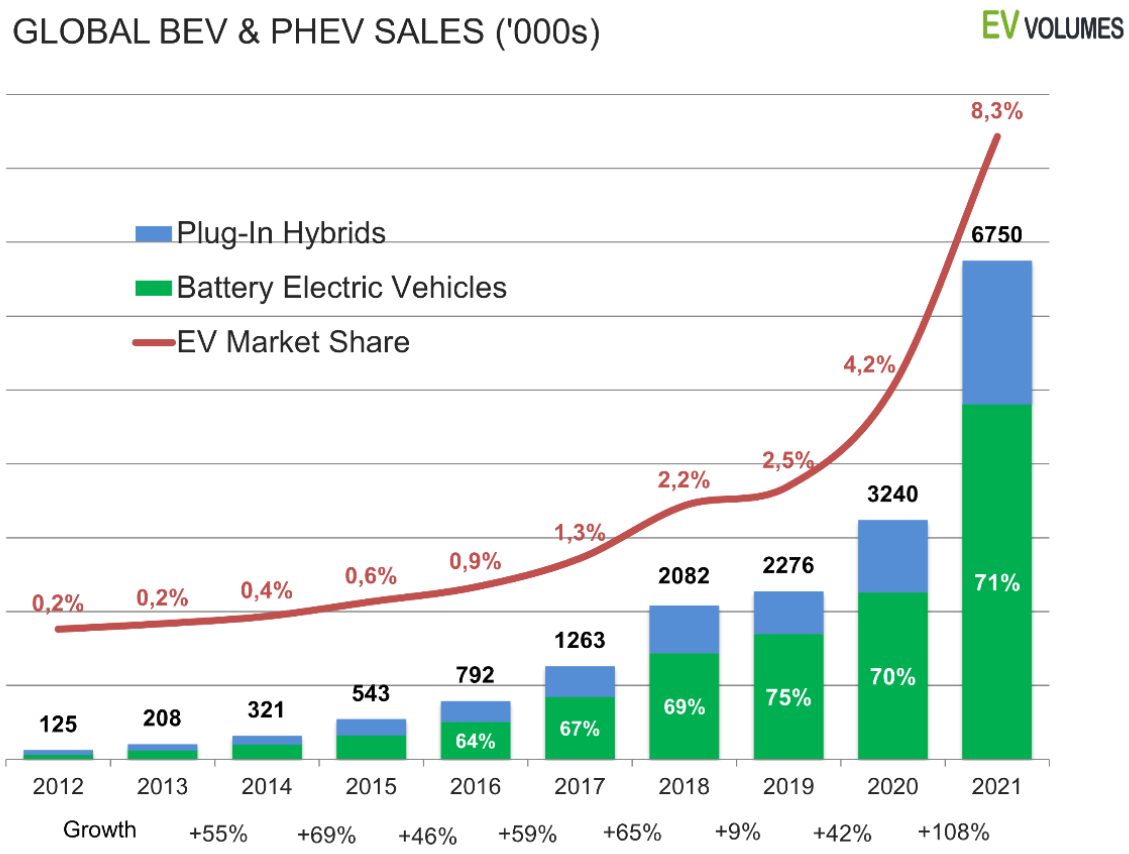

Fig. 1 Global EV sales [6]

Due to the emerging legislation and the growing societal demands in many countries worldwide, the requirements for the efficiency of electrical equipment are constantly increasing. This trend is also driven by the ongoing boom in electric mobility, where it is essential to achieve a high power density of the on-board and off-board electronic components. Therefore, in the field of power electronics and electric drives, significant effort is put into developing more efficient and compact devices and converters [7].

The design of small and highly efficient power converters for electric motors demands wide bandgap semiconductors such as those based on silicon carbide (SiC) and gallium nitride (GaN). Due to a significant reduction in switching losses, GaN-based transistors offer superior performance in high-frequency hard-switched converters than silicon transistors [8], [9]. For these advantages, they are started being used in electrical drives, too [10].

Within electrical drives, especially when powered by batteries, efficiency and power density are essential aspects. The design of small and highly efficient power converters for electric motor control demands wide bandgap semiconductors such as those based on SiC and GaN. These materials, with a high inner electric field, improve the transistor's parameters, such as the current density and on-state resistance. Furthermore, the low parasitic capacitances allow them to operate at higher switching frequencies than silicon devices [7], [8] and [9], [10]. Besides, GaN-based transistors have no reverse recovery charge due to the absence of the freewheeling diode. However, fast-switching devices also bring challenges to the circuit board design and control strategies [11].

The main motivation of this thesis is to analyse the problems that limits usage of GaN transistor in power converters and brings improvements resulting in GaN-based converters to be more efficient in the future.

1.1 The State of Art

1.1.1 Hybrid Electric Vehicles

The hybrid vehicle contains both an internal combustion engine (ICE) and an electric motor. There are multiple options how to connect them. Hybrids are divided into series, parallel and series-parallel drive systems.

The series hybrid contains an ICE with a generator that charges batteries that supply the electric motor.

The parallel hybrid has both an ICE and an electric motor connected to the transmission.

By adding a rotary power splitter, the combination of both can be made.

The parallel hybrid topology is shown in Fig. 2. The optional bidirectional DC/DC converter between battery and motor inverter is implemented in case small capacity low voltage batteries are installed while the DC-bus voltage of the motor inverter is higher.

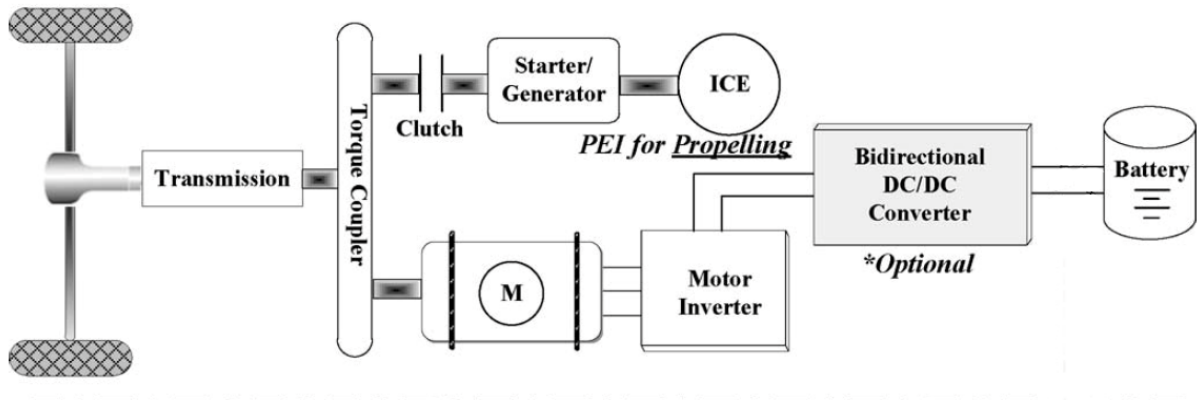

Fig. 2 Parallel hybrid vehicle topology [12]

1.1.2 Battery Electric Vehicles

When we remove ICE completely from the vehicle and increase the battery capacity we can call it battery electric vehicle (BEV).

1.1.2.1 Lithium-based Batteries

Due to the lithium cell's high energy density making the battery lightweight it is the mainstream type of traction battery today. A comparison of energy densities of multiple types of battery technologies [13] is shown in Fig. 3.

An example of the discharge curves for one cell is pictured in Fig. 4. The voltage remains relatively stable during discharge compared to previously used lead or nickel-based cells.

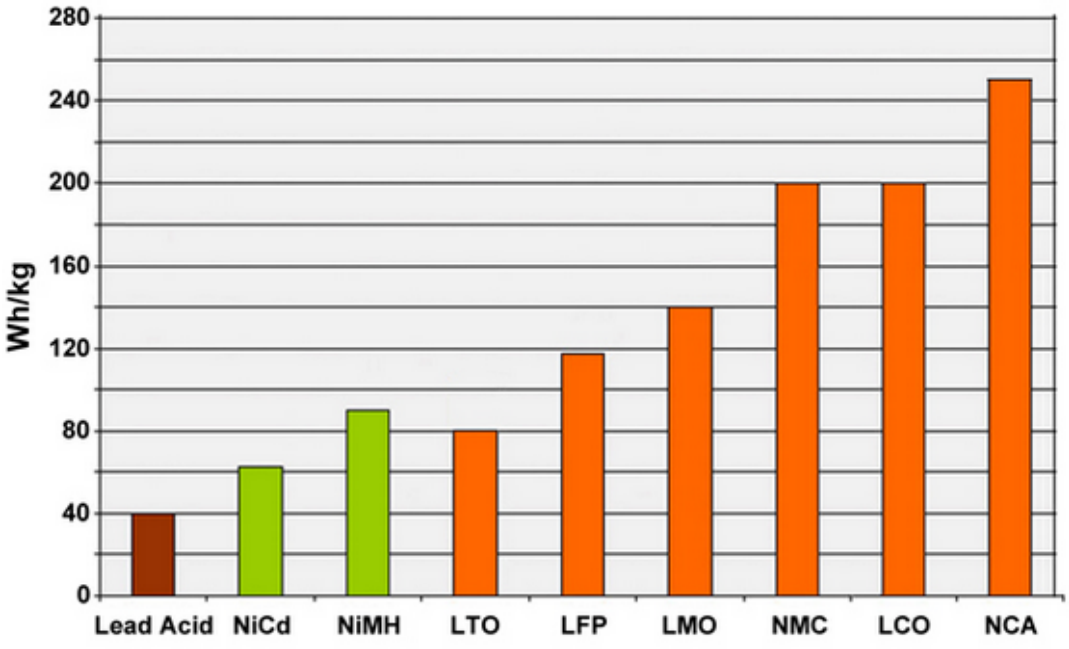

Fig. 3 Energy density comparison for lead, nickel and lithium-based cells [13]

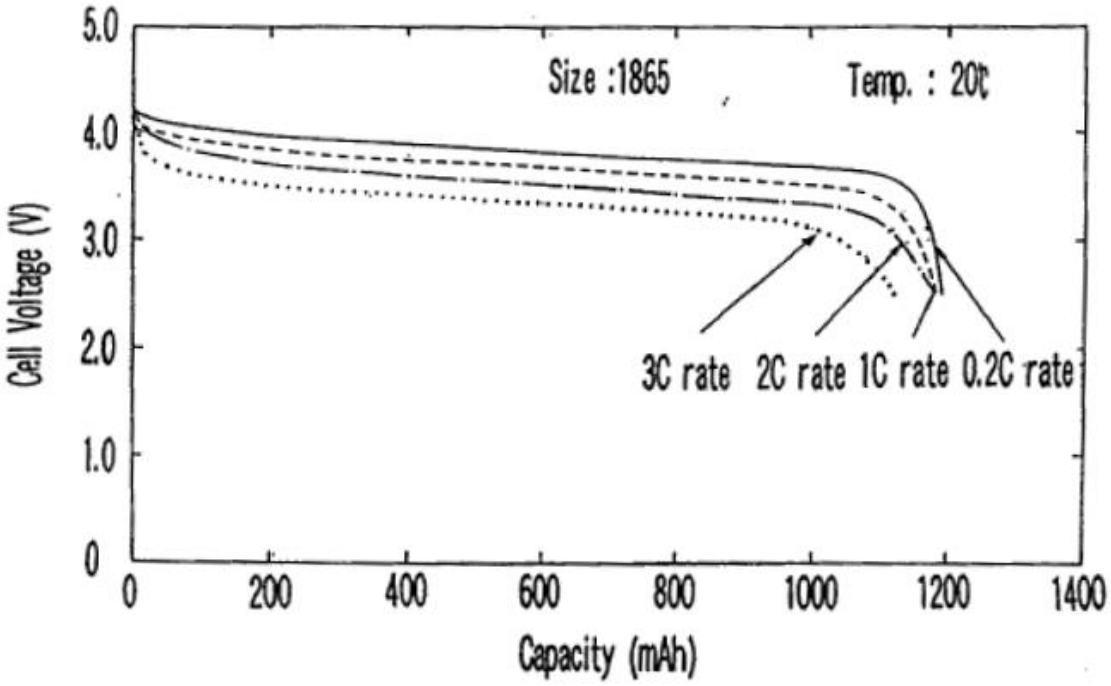

Fig. 4 Discharge curve of lithium-based cell [14]

To increase the specific energy while keeping the cost low, traction batteries are currently made of a large number of series-parallel connected cylindrical cells. An example of a 500 Wh battery pack of lithium-based cells is shown in Fig. 5. The benefit of cylindrical cells is their mechanical stability and the fact that, due to common usage, they became more affordable.

Fig. 5 Example of 500 Wh battery pack of lithium cells

1.1.2.2 Flow Batteries

The main difference from the batteries mentioned above is that the energy in the flow battery is not stored in the cell itself but in tanks of liquid electrolyte. The storage topology makes the flow battery easily scalable from small storages for off-grid houses to large scale on-grid energy storages [15].

The flow battery gives us two independent parameters by which to scale it. The battery's energy capacity is defined by the volume of the storage tanks for electrolyte and the power by the design of flow cells.

The active surface area of the cell's electrodes defines the maximum current, and the number of cells defines the battery voltage [16].

In the case of using a flow battery for an electric traction vehicle the energy density can outperform the lithium-based battery [17], [18]. A recently developed prototype of flow battery powered vehicle called QUANT 48VOLT by Nanoflowcell is achieving a range of 1600 km [19].

Liquid electrolyte stored in tanks gives the opportunity to charge the EV simply by pumping the discharged fluid out of the tanks, positive and negative separately, and pumping back a charged one as fast as refilling of petrol-fuelled cars is done.

The discharged electrolyte is put into another flow battery system to be recharged, for example, in large scale energy storage as part of a solar plant.

The energy is stored in different oxidation states of a given chemical, for example vanadium ions in the case of a vanadium redox flow battery (VRB). Since both positive and negative electrolytes are the same chemical, there is no degradation process in the electrodes [20]. The lack of degradation allows the flow battery to outperform the above mentioned technologies in lifespan. A large scale energy storage system for wind turbines

equipped with flow batteries is already reaching over 270 000 charge-discharge cycles [16].

In the flow battery energy is stored in tanks with liquid electrolyte. Positive and negative electrolytes are stored separately. The electrolyte is pumped through a pack of cells; charged electrolyte enters the cells and is returned to the tank in a discharged state. Due to mixing of the charged and discharged electrolyte, the cell voltage decreases during the discharge process. The interdependence of cell voltage and concentration of V^{2+} ions [20] is demonstrated in Fig. 7.

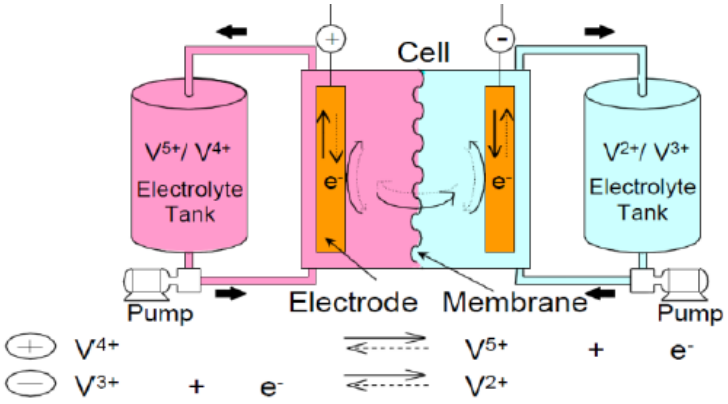

Fig. 6 Vanadium redox flow cell principle [20]

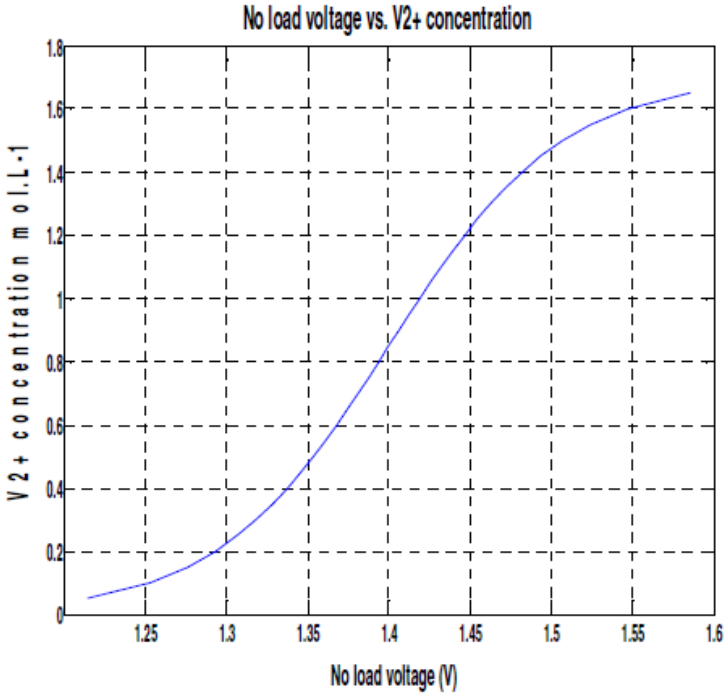

Fig. 7 Vanadium redox flow cell voltage [20]

The result is a significant difference between charged and discharged flow battery voltages compared to lithium-based batteries. The DC/DC converter has to stabilize the battery voltage to provide constant DC-bus voltage for the traction motor DC/AC converter.

Individual cells can be stacked in series to reach higher terminal voltage [21] while they share the same electrolyte that is pumped through them from the same tank as seen in Fig. 8 and Fig. 9. Increasing the number of cells increases the leakage current that goes through the liquid between cells that are at different potentials. The solution for leakage current is increased length of tubing with smaller diameter between cells however, generally speaking, the flow battery operates better at low voltage, for example 48 V, and high current depending on the needed power.

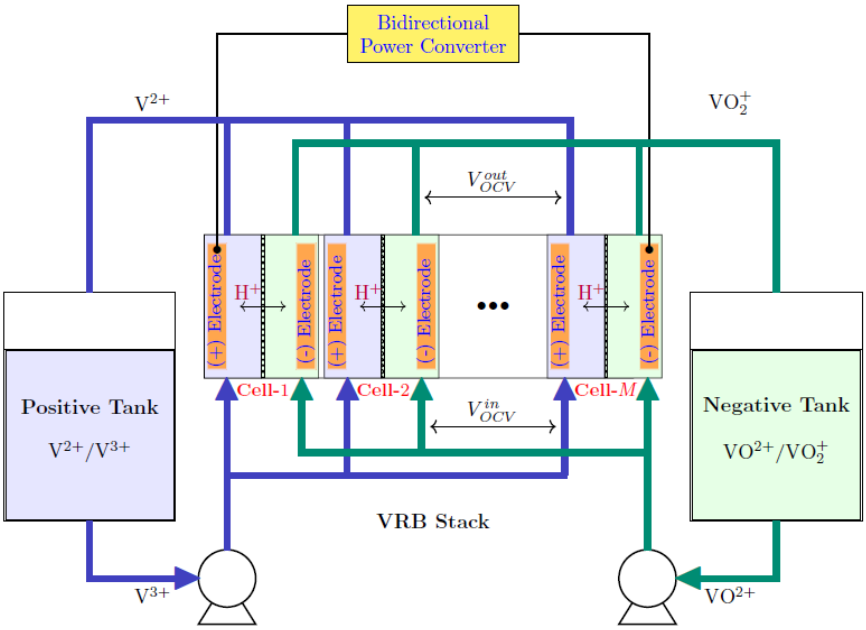

Fig. 8 Multiple cell vanadium redox flow battery [21]

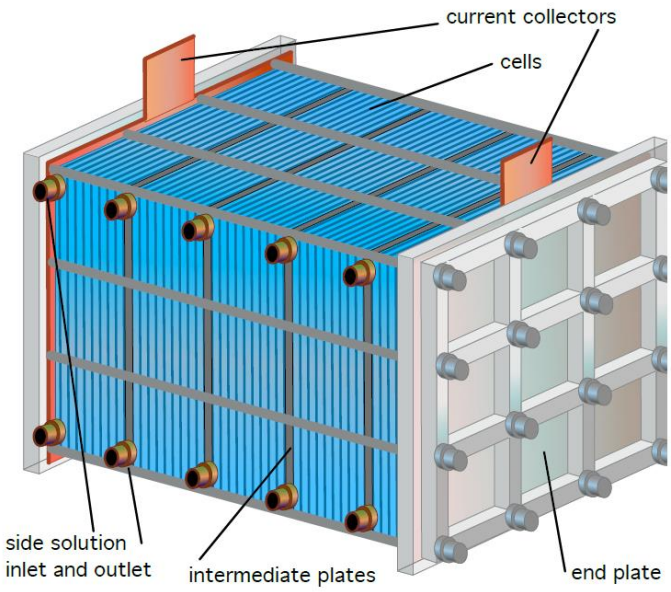

Fig. 9 Vanadium redox flow battery stack [16]

1.1.3 Power Converters in Electric Vehicle Tractive System

A typical diagram of the vehicle tractive system topology is shown in Fig. 10.

The traction battery is arranged as a series or series-parallel combination of cells that have a total voltage usually equal to the DC-bus voltage of the motor controller. These days regular EVs are using 400 V or 800 V. Optionally there can be a bidirectional converter placed between the battery pack and the DC-bus. This is often omitted to increase the system overall efficiency and the regulation is done in the motor converter. It means the motor is designed to utilize the available DC-link voltage equal to the battery.

Non-isolated boost converters are optionally present in vehicles with 800 V battery to enable them be fast-charged from 400 V DC chargers.

Isolated DC/DC converters are used in on-board chargers to provide the required safety. To decrease the amount of converters to reduce the amount of expensive power semiconductors, the charger can be made of a DC/AC traction converter and a motor winding according to [22]. On-board chargers are designed in range of power from 3.6 kW single phase to 11 kW or 22 kW three phase.

Unidirectional isolated DC/DC is used to supply the low-voltage on-board components. On-board grid usually operates on 12 V or 24 V. To reduce the losses in the wiring the on-board grid voltage can be also designed at 48 V. These converters are designed typically in 1 kW power range.

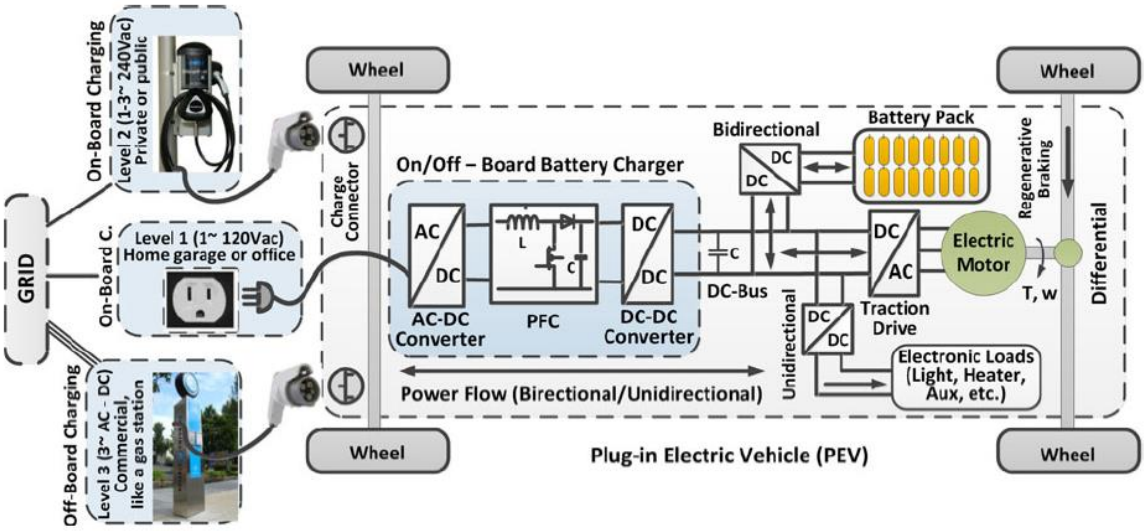

Fig. 10 EV power converters [22]

1.1.4 Semiconductor Devices

The following chapter focuses on the comparison of power semiconductors available for today's converter designs. Among the wide spectrum of different technologies on the market today, the following selection was chosen for comparison.

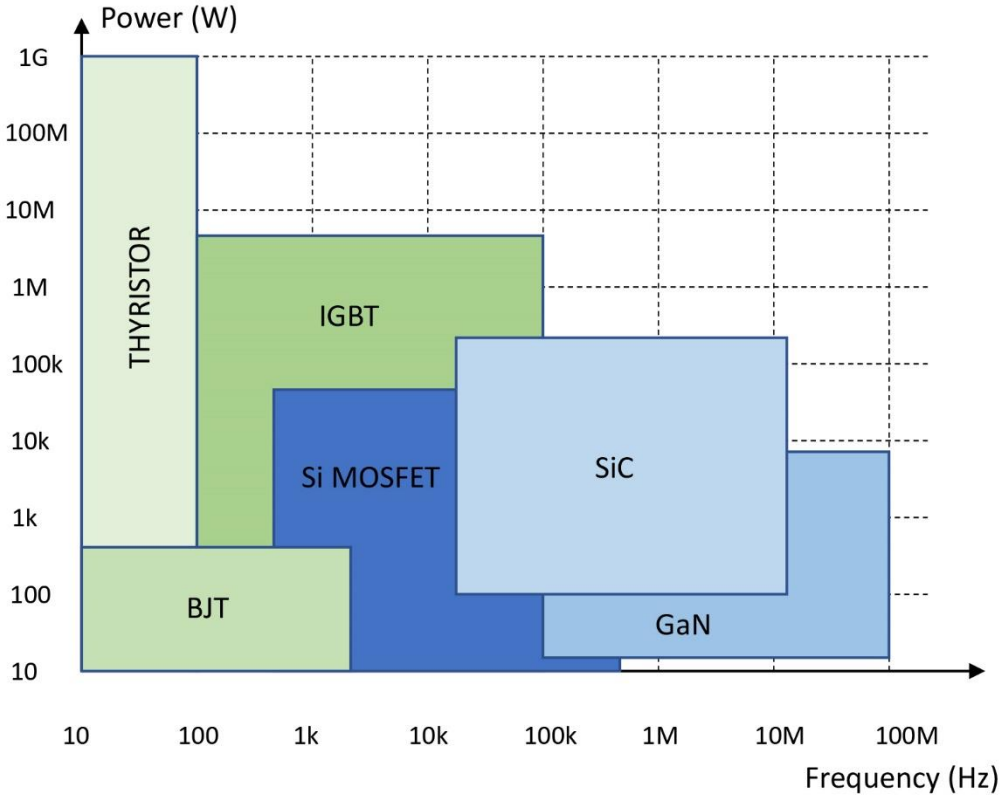

Fig. 11 Power semiconductors typical application for power and switching frequency [23]

1.1.4.1 Si MOSFET

The technology of the classic metal oxide semiconductor field effect transistor (MOSFET) structure performs well at low voltages. For higher voltages the R_{DSon} rises rapidly [23]. Components of the R_{DSon} are shown in Fig. 12.

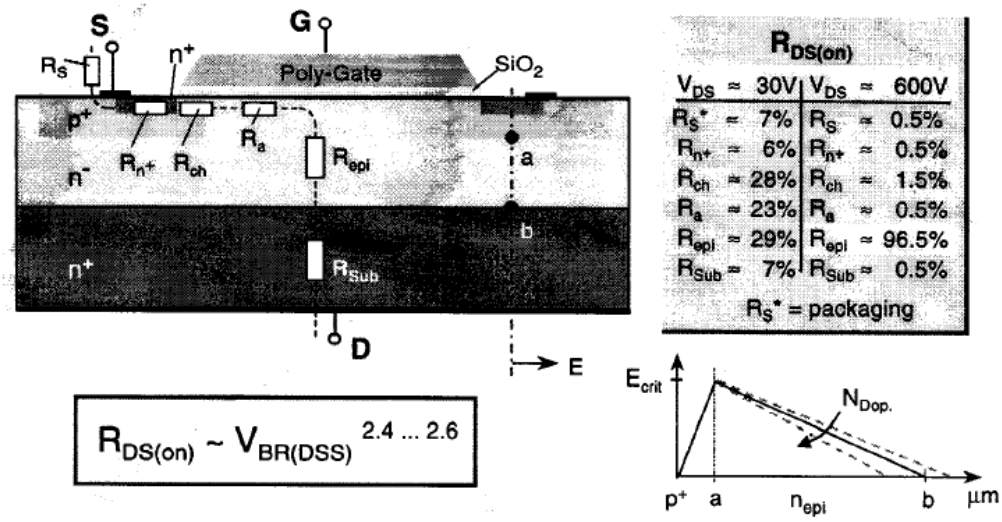

Fig. 12 Classic MOSFET structure R_{DSon} components [23]

For higher voltages the R_{epi} becomes significant so other technologies were developed to reduce this resistance while keeping a high breakdown voltage V_{BR}.

Classic MOSFETs with V_{BR} = 100 V reach very low R_{DSon} and are relatively cheap compared to other technologies. However, for higher voltages it is better to look for a different type of MOSFET structure, super-junction (SJ) such as CoolMOS for example.

Today's technology enables the thickness of the structure be thin while keeping the high breakdown voltages so the R_{epi} becomes least significant compared to the channel resistance R_{ch}.

1.1.4.2 Si SJ MOSFET (CoolMOS)

When trying to decrease the R_{DSon} of the classic MOSFET structure at higher breakdown voltages, the structure with vertical p-doped areas as shown in Fig. 13 was developed.

Due to the fact that only majority carriers conduct the current, switching losses remain the same as those of the classic structure while R_{DSon} is decreased even at high breakdown voltages.

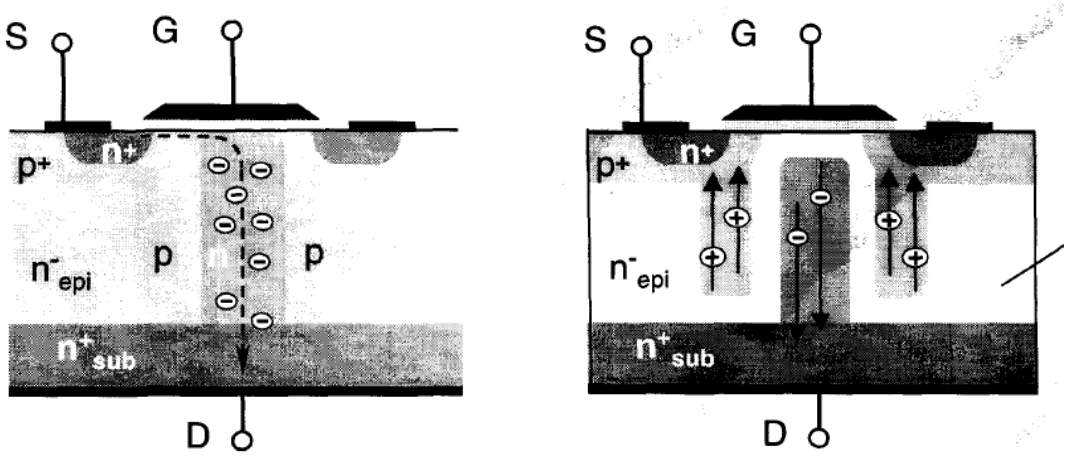

Fig. 13 CoolMOS structure in turn-on (left) and turn-off state (right) [23]

CoolMOS technology now provides 10 times lower R_{DSon} compared to the classic MOSFET structure while keeping equal gate charge [24].

Switching losses equal those in classic MOSFETs so CoolMOS achieves higher efficiency in resonant converters compared to classic MOSFET structure just due to lower R_{DSon}.

1.1.4.3 Si SJ MOSFET (MDmesh)

The multiple drain mesh (MDmesh) structure shown in Fig. 14 appeared in 2000 and is in its fifth generation, achieving one of the lowest R_{DSon} values in the field of Si MOSFETs [25]. When developed, this technology decreased the conduction losses per area to 50 % compared to regular Si MOSFETs [26]. MDmesh allows transistors of half the conventional die size, giving 50 % lower gate charge for applications of the same power.

This technology makes a good alternative to CoolMOS that is, due to lower output capacitance, more suitable for hard-switching applications.

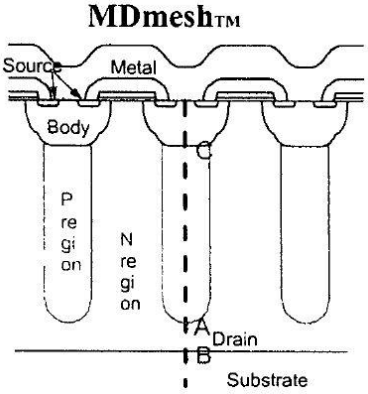

Fig. 14 MDmesh structure [26]

1.1.4.4 Si IGBT

Unlike in MOSFETs, insulated gate bipolar transistor (IGBT) structure needs a significant voltage drop of 0.7 V when turned-on to increase the concentration of charge carriers in the drift zone to provide conductivity. Due to the voltage drop, the drift zone is filled with both electrons and holes which cause a tail current when turned-off. Because of this tail current, IGBTs have higher turn-off switching losses compared to MOSFETs [23]. The structure is shown in Fig. 15.

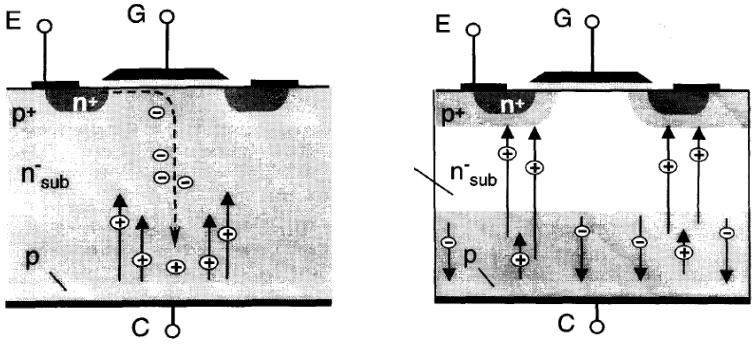

Fig. 15 IGBT structure in turn-on (left) and turn-off (right) [23]

IGBT transistors are still very popular in high power converters in the 1.2 kV voltage range. High switching losses associated with IGBT turn-off tail current are reduced by decreasing the switching frequency.

When high frequency is needed in high voltage applications the better option presently is the SiC MOSFET.

1.1.4.5 SiC

Silicon carbide (SiC) based semiconductors are real competitors for IGBT transistors in high power, high voltage converters [27]. The device to device comparison according to [30] is shown in Tab. 1.

Tab. 1 SiC to IGBT converter efficiency comparison [30]

	IGBT system	**SiC system**
Conduction loss (per device)	IGBT 114W	MOSFET 36W
	Diode 20W	Diode 25W
Switching loss (per device)	164W	36W
Inverter total loss	1789W	584W
Output power	61.2kW	61.2kW
Efficiency	$\eta = 97.1\%$	$\eta = 99.1\%$

SiC as a MOSFET structure has lower conduction losses compared to IGBT but the significant difference is in switching losses.

SiC MOSFET structure is close to the classic Si MOSFETs as shown in Fig. 16. The proposed asymmetric structure in [31] with better channel mobility decreases the on-resistance while the deep p-wells provide the function of freewheeling diode.

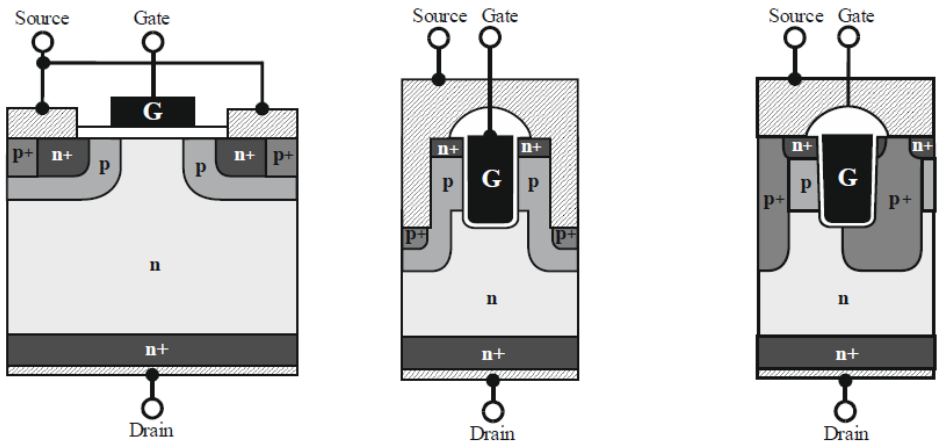

Fig. 16 SiC MOSFET classic structure (left), trench structure (center), proposed improved asymmetric trench structure (right) [31]

To improve the freewheeling diode characteristics, an external SiC Schottky barrier diode can be added to provide fast switching while the slower body diode conducts the current after the completion of the switching transition because the body diode has lower on-resistance [32].

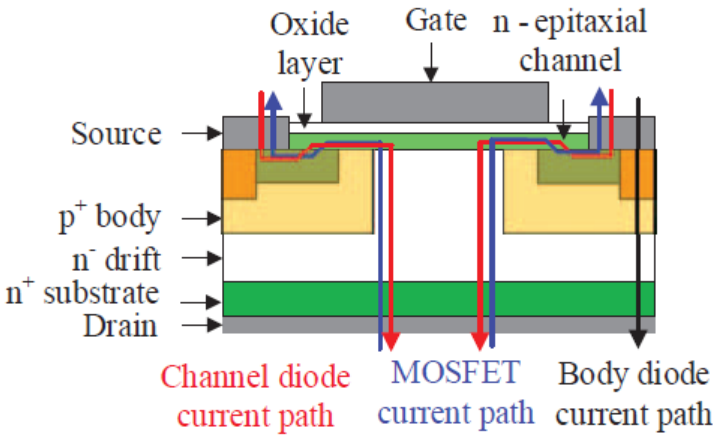

Fig. 17 External Schottky diode in SiC transistor [32]

The main negative aspect of SiC technology is its cost which is now about 5 times that of a Si IGBT module of the same rated voltage and current. Due to the cost, SiC technology is limited to use in a specific range of converters where high power density is required, such as traction converters for electric vehicles. However small power 650 V SiC transistors have recently appeared and are available in similar packaging and in the same price range as IGBT or Si MOSFETs and, promising to operate with standard drivers, will be great competitors to Si transistors.

1.1.4.6 GaN

High-electron mobility transistors (HEMT) based on gallium nitride (GaN) in recent years have appeared in the power electronics field [28], [29]. Earlier depletion-mode GaN transistors have been used in RF applications. For power electronics the enhancement-mode is needed so multiple ways to obtain it have been developed.

Similar to early SiC technology, the cascade topology has been applied [28] to high voltage depletion-mode GaN structures on Si substrates to produce enhancement-mode devices as shown in Fig. 20. The lateral structure provides low channel resistance due to the existing 2-D electron gas (2DEG) formed by strong polarization in the GaN layer. Normally, to deplete this region a negative gate voltage must be applied. The cascade topology simply adds a classic Si MOSFET transistor in series with the source electrode to obtain the required negative gate bias during turn off.

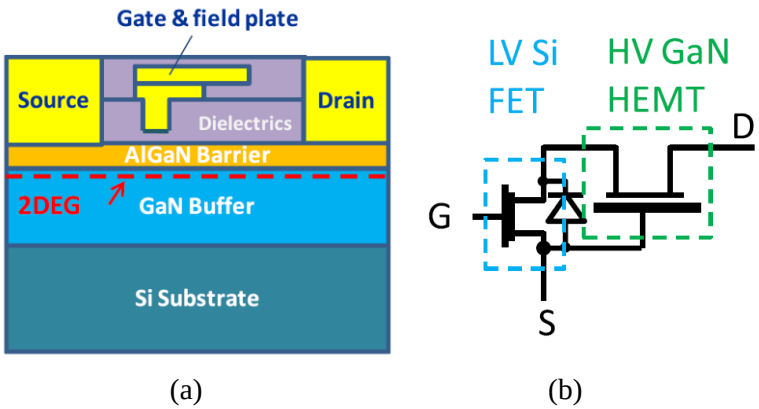

Fig. 18 Depletion mode GaN on Si (a) as a part of the cascade (b) [7]

The main problem of the cascade connection is increased on-resistance because of two channels being in series.

To produce an enhancement mode GaN transistor, the gate threshold voltage Vth needs to be increased. Using the p-doped layer under the gate, the channel is depleted when no voltage is applied to the gate [33]. Such a transistor is called gate injection transistor (GIT) whose structure is shown in Fig. 19.

When a positive voltage higher than Vth is applied on the gate electrode, hole injection from the p-doped layer under the gate enables the channel to conduct current with R_{DSon} similar to that of a normally-on GaN structure.

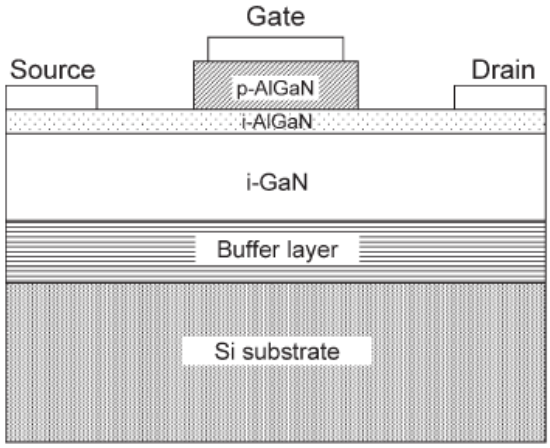

Fig. 19 GaN on Si GIT structure [33]

The main benefit of the GaN transistor structure is the reverse conduction region. The reverse characteristic is able to perform as a freewheeling diode in classic converter applications. Since there is no substrate diode, this transistor has no reverse recovery charge. While the reverse on-state resistance is controlled by positive gate voltage, the structure conducts reverse current even with zero gate voltage [34].

The GaN structure offers linear change in output capacitance during turn-on/off compared to Si or SiC [8], as it is depicted in Fig. 20.

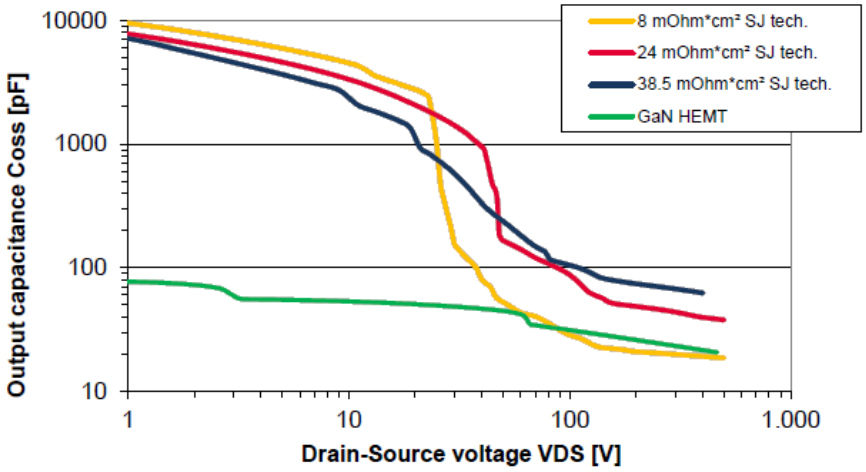

Fig. 20 Output capacitance dependence on V_{DS} [8]

The output capacitance linearity is important for converter efficiency at high frequencies. The mechanical design of the converter limits the maximum di/dt capability and output capacitance linearity makes the di/dt slew rate constant during the whole process of turn-on and turn-off.

According to [35] the GaN transistor has approximately 10 times less gate charge compared with Si MOSFETs chosen for converters of the same power category. On the other hand, the gate driver must be fast enough for the transistor to work at high frequencies where the above described benefits become useful.

Si, SiC and GaN technologies are compared in Tab. 2 in [8] with selected transistors being of the same power range.

Tab. 2 Si, SiC and GaN transistor parameter comparison [8]

	Silicon	SiC	GaN
Concept	super junction	planar MOSFET	eMode HEMT
Blocking voltage	600V	900V	600V
On-state resistance (typ.)	56 mOhm	65 mOhm	55 mOhm
Reverse recovery charge	6000 nC	130 nC	0 nC
Energy stored in Coss @ 400V	8.1 µJ	8.8 µJ	6.4 µJ
Charge stored in Coss @ 400V	420 nC	70 nC	40 nC
Turn-off loss @ 10A / 400V	15 µJ	10 µJ	10 µJ

The main trouble remaining is that the available parts suit relatively small power converters only in the range of a few kW. Compared to SiC the base material is cheaper so GaN has the potential to replace Si transistors in the future.

In Fig. 21 currently available GaN transistors are shown.

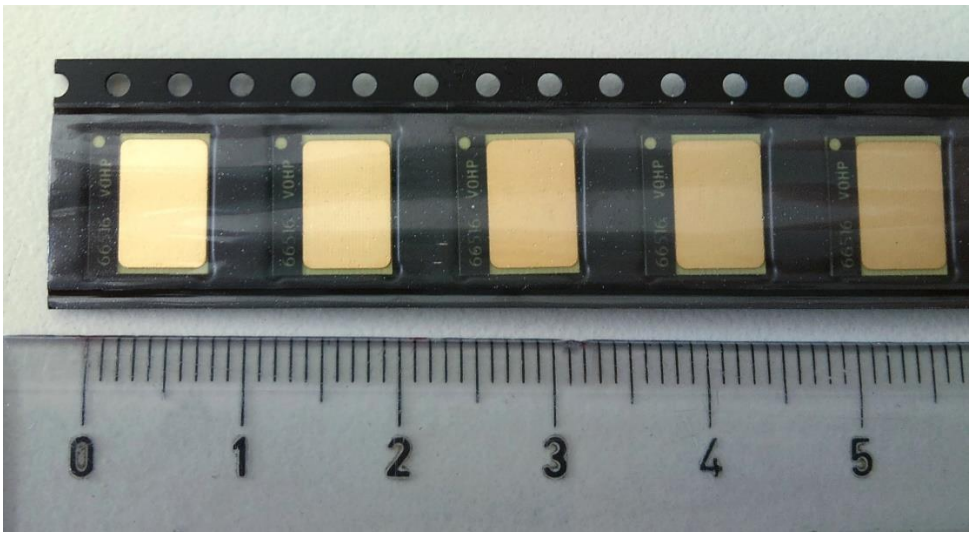

Fig. 21 GaN-based 650 V 60 A transistors

1.2 Motivation

During my bachelor and master studies I was interested in electric vehicle tractive system and gained some experience when designing and testing an IGBT based DC/DC converter for a separately excited DC traction motor in Citroën Berlingo Electrique. Utilizing the new generation IGBT enabled to increase the vehicle tractive converter efficiency significantly which resulted in a small fully air-cooled design.

At the time I entered the doctoral studies, new SiC and GaN-based semiconductors were entering the field of power electronics suggesting new possibilities in efficiency improvement and power density increase. Based on previous interest in electric vehicles the framework topic “Analysis of Power Electronic System of Electric Vehicle with Energy Storage” was chosen.

Based on the stated thesis objectives the thesis title “Improving the Electric Vehicle Converter Performance Using New Semiconductor Components” was adopted. It represents a concretization of the original framework topic.

1.3 Thesis Objectives

Based on the state of the art and discussed problems the global objective has been defined as minimizing losses in GaN-based converters. To succeed this global objective, the following five thesis objectives were taken into account.

1. Improving drivers' performance to maximize utilizing the devices' capability.

The idea is to create a fast driver that will ensure safe operation of the GaN transistor in power converters when utilizing fully the transistor operation area. This leads to the fast current limiting driver development that will respect specific behaviour of fast switching GaN transistors.

2. Analysing the new perspective devices' cooling possibilities.

Analysis of the new cooling possibilities in comparison with regularly used means of cooling needs to be done with respect to the new design of GaN devices. Their high current density brings challenges in the cooling system design for transistors with small packages.

3. Minimizing the new devices' losses in their switch-on state by the software control algorithm extension only.

Analysing software possibilities that will optimize the switch-on state performance of the GaN transistor in respect to the dynamic behaviour of the on-state resistance. The dynamic resistance, especially current-collapse phenomenon present in HEMT devices needs to be studied.

4. Minimizing the new devices' losses in their switch-off state by the software control algorithm extension only.

Analysis of switch-off state behaviour of GaN transistor and its losses that significantly decrease the performance of HEMT devices when operated in reverse conduction region. This leads to a development of an algorithm that tracks the optimum dead-time to minimize the time of high reverse voltage drop operation.

5. Reducing the converters' output voltage drop by the on-line dead-time control.

Dead-time in converters' half-bridge causing voltage drop can be reduced by optimum dead-time setting. However, the optimum dead-time changes due to transistors' switching delays are current depending. A software on-line control based on actual measured half-bridge current can improve the overall efficiency curve of AC converters.

2 Current Limiting Driver for GaN Transistor

This chapter was partly published in Proceedings of the 2017 International Conference on Applied Electronics, see [39].

The quickly developing technology of GaN power transistors is calling for a new sophisticated high speed driver. The fast switching GaN transistors with no reverse recovery charge allows us to design a new level of high frequency converters with high efficiency and power density. Together with the transistors we have to keep improving other components to meet their requirements. One key component is the gate driver this chapter is dealing with.

The goal of the driver is to operate the transistor within the whole range of its parameters. High speed current limiting driver was described in [40] for SiC transistors but GaN transistor has the potential to operate at higher frequencies and therefore the driver should be even faster.

For most types of converters, the main benefit of the increased operating frequency is increasing the power density. The higher the frequency, the smaller inductance is needed. Thereafter the inductors' cores can be smaller and number of turns lower, which means that the conductivity losses in copper are substantially reduced and the efficiency significantly increased.

For off-grid operating inverters, the output short circuit or time limited overload is common and the converter has to handle it without troubles. These high efficiency converters provide very low output impedance compared to the grid which causes much higher short-circuit currents. The driver has a possibility to be able to turn off the transistor safely when the maximum allowed drain current value is being exceeded.

2.1 Gallium Nitride Basis

2.1.1 No Reverse Recovery

GaN transistor does not contain parasitic substrate free-wheeling diode compared to Si or SiC MOSFETs. Nevertheless, GaN transistor allows reverse conduction without reverse recovery charge. Reverse conduction is used after turning-off the opposite transistor in the half-bridge, as illustrated in Fig. 22.

In reverse conduction the positive gate voltage can be applied to reach low switched-on state resistance. When looking into datasheets of today's available GaN transistors [34], the channel resistance in reverse conduction can substitute the freewheeling diode, see Fig. 23. In this case the conduction losses are not higher compared to other switching devices.

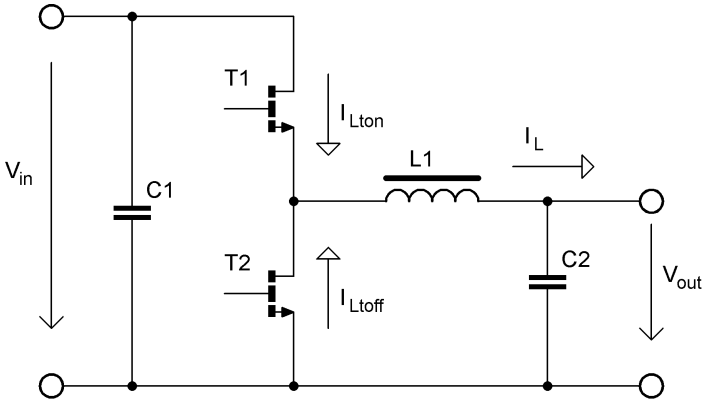

Fig. 22 Reverse current (I_{Ltoff}) in GaN-based half-bridge

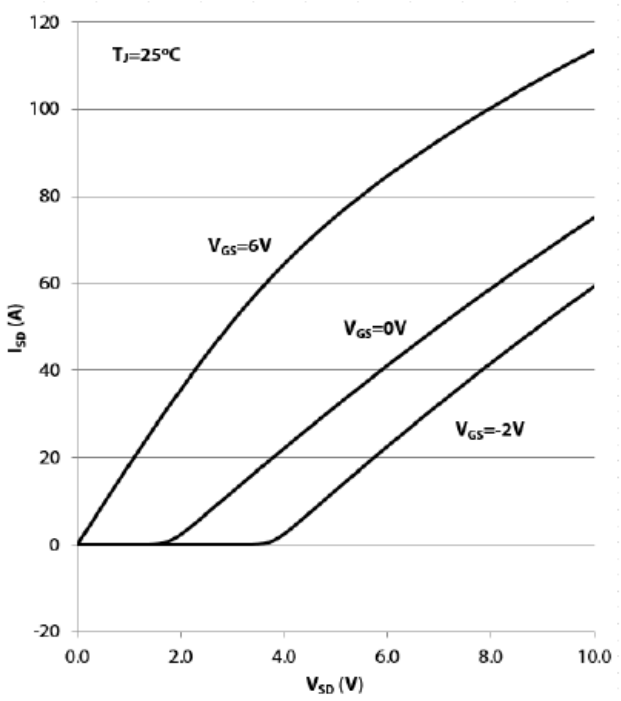

Fig. 23 Reverse conduction region [34]

2.1.2 Gate Driving Requirements

The GaN transistor has approximately 10 times lower gate charge compared to Si MOSFET of the same power category [8]. The gate threshold voltage depends on the technology. The E-mode HEMT forward characteristic example is shown in Fig. 24.

More important is to choose a driver operable at the desired frequency. Propagation delays of the driver output stage are now important because they cause pulse width modulation (PWM) signal distortion when on and off delays are not equal.

In datasheets some MOSFET drivers are labelled as ultrafast [41], but unfortunately nowadays they became too slow for GaN transistors and the driver is actually the part that limits the maximum PWM frequency.

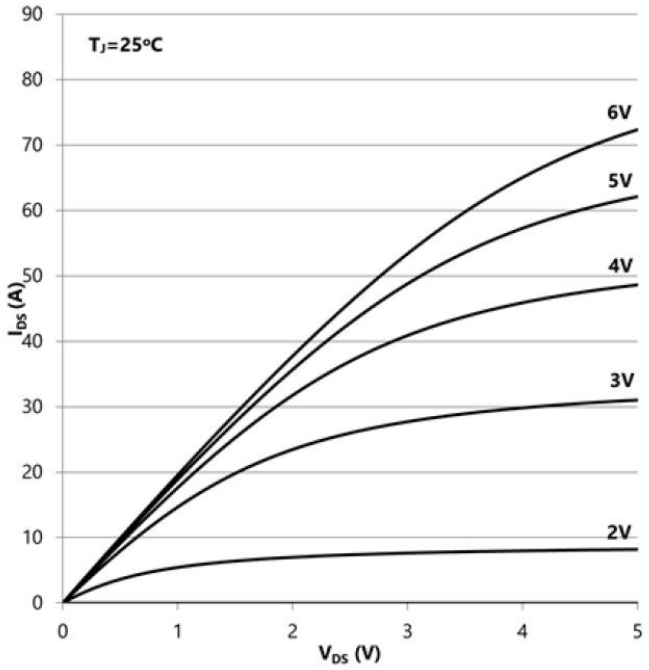

Fig. 24 Forward conduction region [34]

2.2 GaN Driver Design Requirements

2.2.1 Current Measuring

The method of measuring the transistor's on-state resistance voltage drop has been chosen to determine the current value. The on-resistance R_{DSon} is a temperature dependent quantity defined in the datasheet, so it can be used for calculation of the allowed maximum voltage drop across the drain-source channel. The R_{DSon} temperature dependency varies with the transistor's technology, for an example see Fig. 25.

The calculated maximum voltage drop is then set as a reference for fast comparator that is measuring the voltage to determine the maximum current allowed.

The pulse by pulse current limiting consists of RS flip-flop, so the transistor remains turned off until the next rising edge of the input signal is received. However, the controller receives the error signal and it depends on the controller only if the next rising edge will come.

The output stage of the driver is equipped with a high speed tri-state buffer controlled according to the Tab. 3.

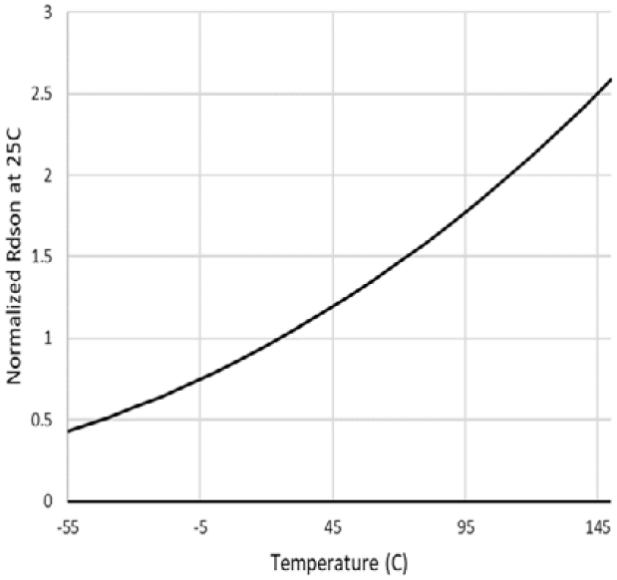

Fig. 25 R_{DSon} temperature dependency [34]

Tab. 3 Gate control logic

PWM Input	Over-current detected	Gate output
0	X	Off
1	0	On
1	1	Slow turn off

2.2.2 Safe Turn-Off Over-Current

The bigger the current the higher is the di/dt during turning off when the fall time determined by the gate resistor does not change. High di/dt is causing overvoltage spikes on the parasitic inductances in the circuit. To prevent the damage of the transistor during turning off the over-current state the gate is discharged through an extra path with higher gate resistance compared to normal turn-off. Higher gate turn-off resistance is discharging the gate slower which causes the transistor to turn off slower, reducing the di/dt.

Fig. 26 compares the desired turn off with the one caused by the driver delay.

The threshold current is set to reasonable value but the peak current will be higher due to the propagation delay of the driver.

Compared to Si IGBT and SiC where this method is also used [40], the turn-off delay of the driver itself is significant. GaN is much faster, even compared to today's IC drivers. The delay from the over-current detection till the actual beginning of turning off has to be considered.

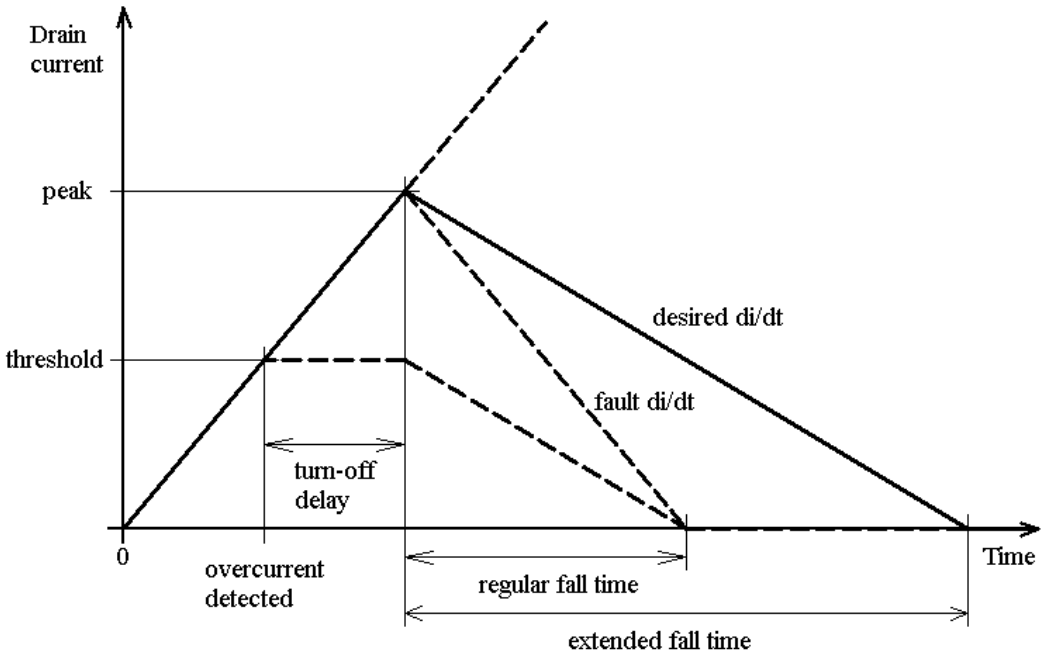

Fig. 26 Fall time extending

2.2.3 **PCB Design**

The path that consist of the low side transistor, high side transistor, and DC-link capacitor has to be designed with the lowest possible parasitic inductance.

Parasitic inductances in the path are causing voltage spikes during the transistors' switching on and off. The printed circuit board (PCB) design methods how to decrease this problem and utilize the voltage and current capability of the transistor are described for example in [42].

A basic one is to connect the path on the PCB using short but wide polygons instead of thin and long paths. Multiple layer board allows to cancel most of the inductance when routing the path in a different layer the opposite direction creating a parasitic inductor with a minimum area. This leads to the design where the DC-link capacitor is placed in-line with the half-bridge transistors [43].

An example of the GaN half-bridge board design is in Fig. 27 where the transistors are placed on the bottom side right below the temperature-stable ceramic (C0G) DC-link capacitor. This board was designed for the converter in chapter 6.

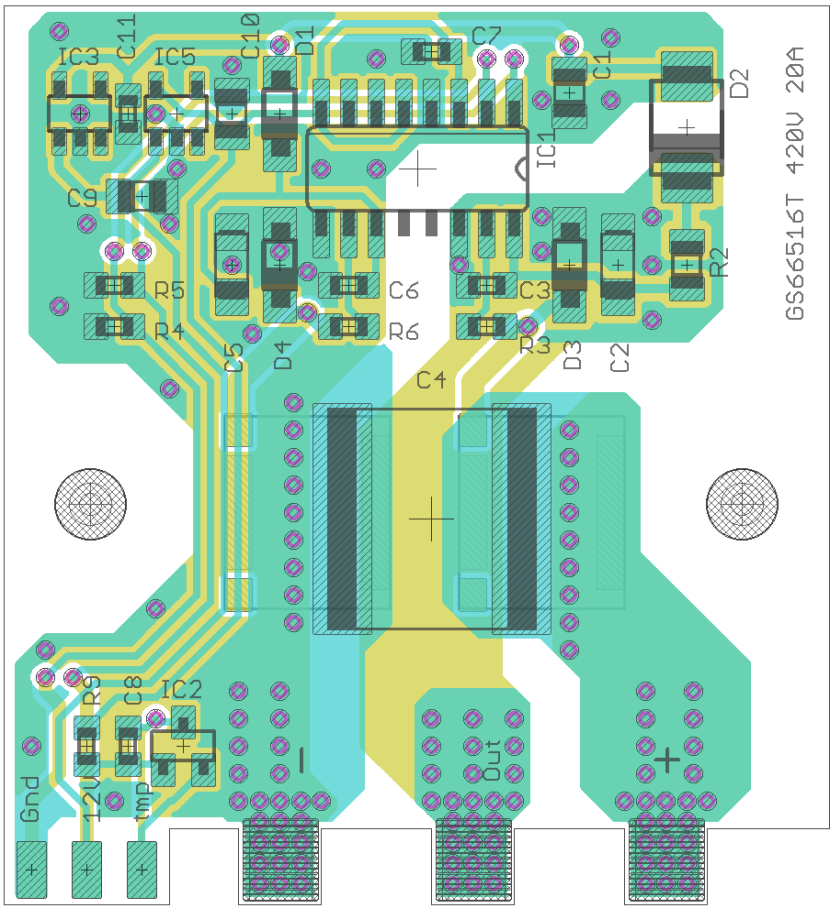

Fig. 27 Current loop minimizing example

2.3 Designed Prototype

Based on the requirements of GaN transistors a new driver circuit have been designed.

2.3.1 Proposed Driver Schematic Diagram

In Fig. 28 a block diagram of one side of the half-bridge driver is described. The detailed schematic diagram is in Fig. 29.

The isolation barrier is equipped with bidirectional isolators for input PWM signal and fault output. A DC/DC converter provides the power for logic and output stage of the driver, too. Both low and high sides have their own isolators and DC/DC isolated converters.

The PWM signal feeds directly the output tri-state buffer that controls the gate in normal operation.

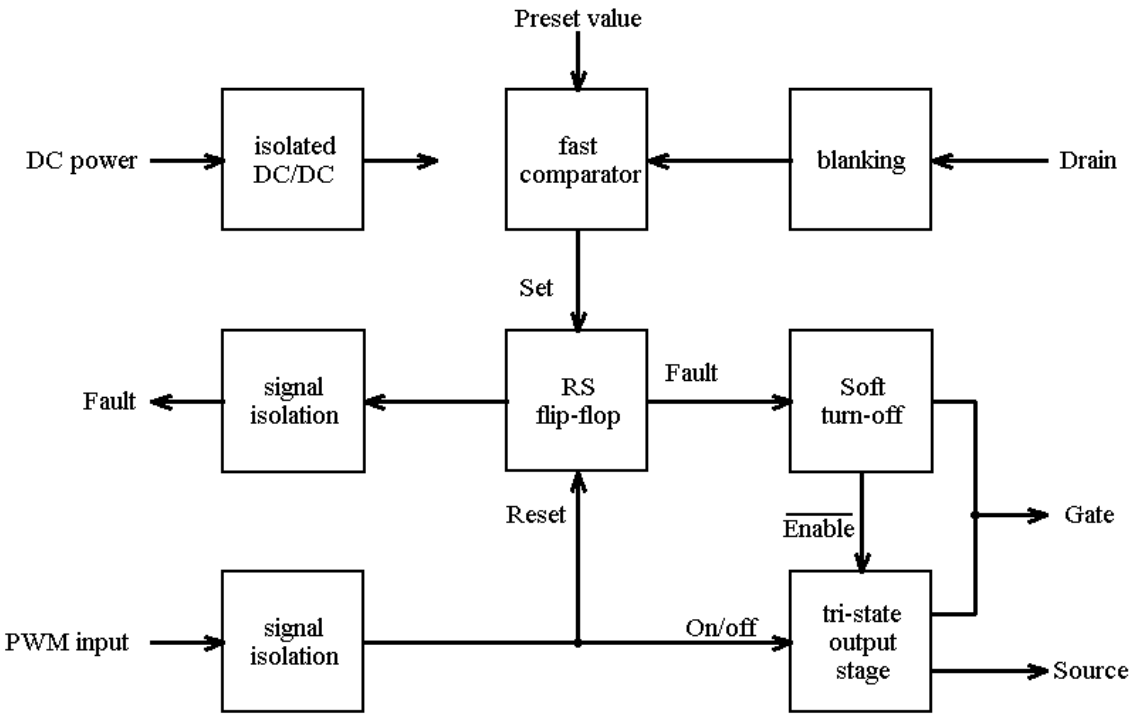

Fig. 28 Block diagram of the current limiting driver

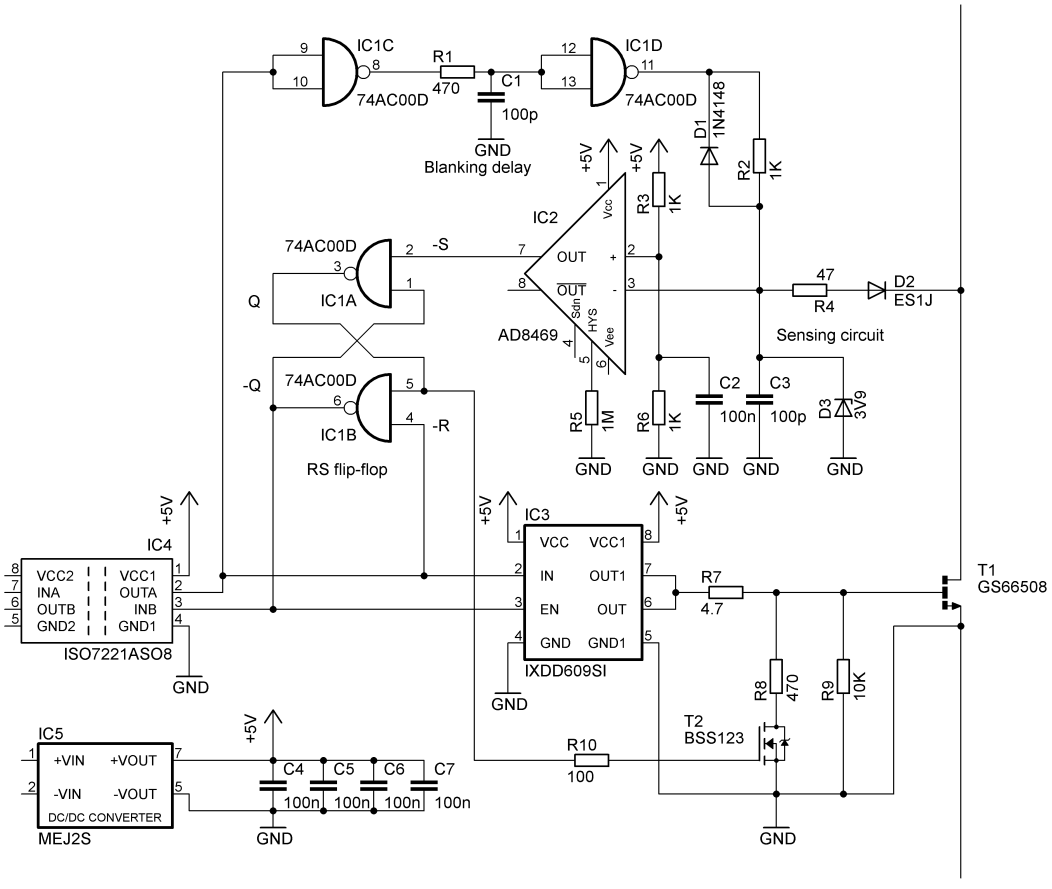

Fig. 29 Circuit diagram of the current limiting driver

Current is measured using a voltage drop across the transistor which is sampled through a diode. Sampling circuit is necessary to measure the low voltage only when transistor is turned on. It also adds a small delay that respects the propagation delay of the signal path so that the comparator doesn't receive a false voltage before the transistor is turned on.

Fast comparator has a pre-set value of maximum drain to source voltage and when the measured value is higher the output fault signal is set.

Fault signal changes the state of the RS flip-flop in the way that the output stage is forced to high impedance and gate is discharged through an extra path with a higher gate resistance to achieve the desired over-current soft turn off.

2.3.2 **Testing the Prototype**

The designed prototype half-bridge is shown in Fig. 30. For testing the over-current protection, one more board with high-side GaN only and SiC Schottky diode in the low-side was made. The over-current protection was then tested according to a simplified circuit diagram in Fig. 31

Measured delay times are presented in Tab. 4 in comparison with datasheet listed values of two other selected fast drivers equipped with similar over-current protection Si8286 and ACPL339J [40].

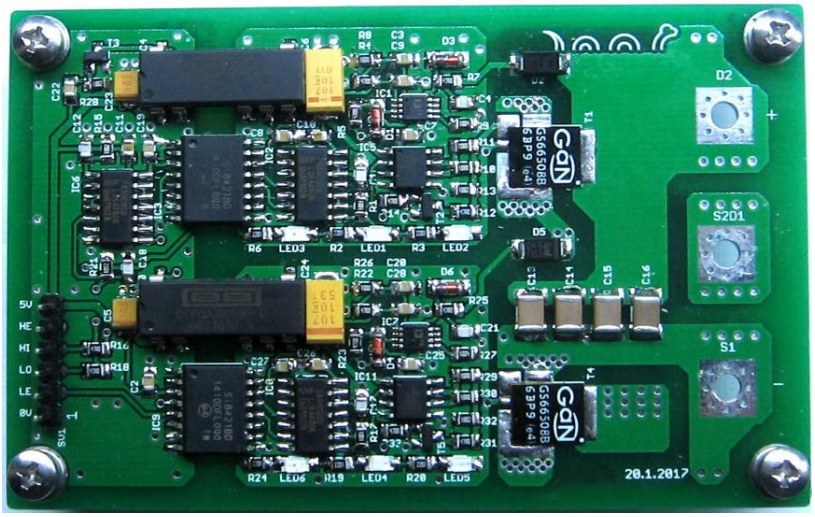

Fig. 30 PCB prototype

Tab. 4 Current protection response time

Time [ns]	ACPL339J	Si8286	Designed driver
Blanking	200	270	50
Turn-off delay	300	50	50
Turn-off fall	300	320	100
Total	800	660	200
Response time	500	340	100

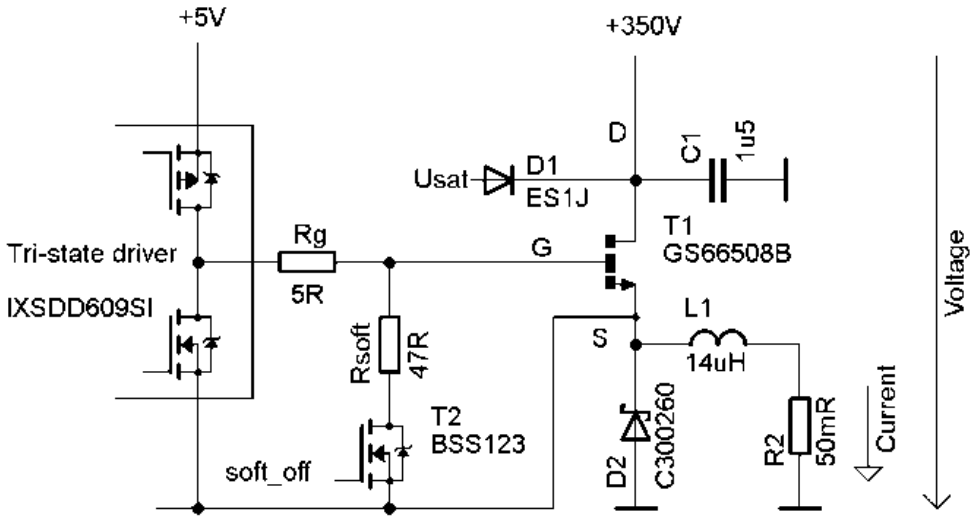

Fig. 31 Simplified circuit for testing the over-current protection reaction on short circuiting of the converter output

Response times were measured with two different R_{soft} resistors of 47 Ω and 470 Ω which means 10 times and 100 times higher resistance compared to the regular turn-off resistor R_g = 4.7 Ω.

Higher resistor value prolongs the turning-off delay since the voltage has to drop below the gate threshold. Simple clamp circuit from [40] will improve it.

Measured results are shown in Fig. 33 as a peak current and converter on-time depending on the applied voltage. The inductance remains the same which means that different voltage gives different di/dt for each point.

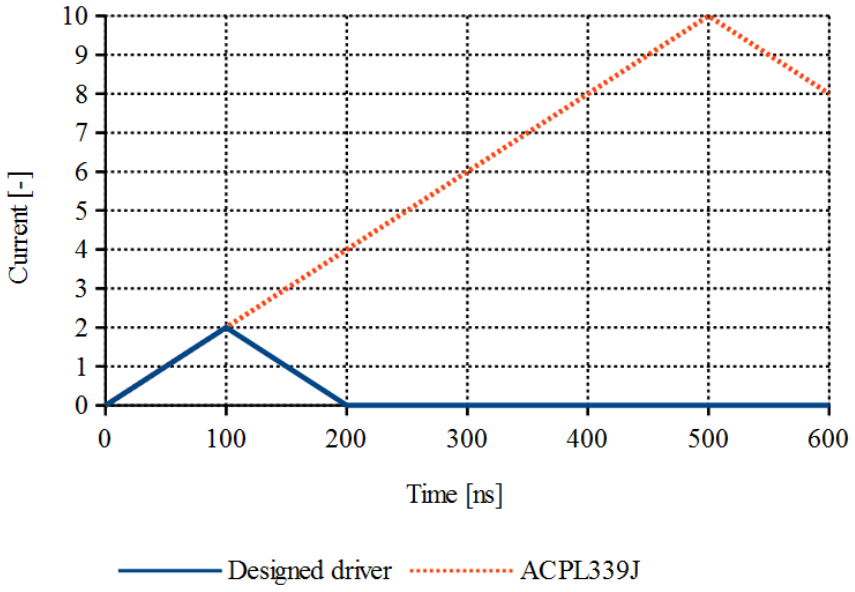

Fig. 32 Comparison of the current protection response times reckoned with relative current values assuming both drivers used in the same circuit shown in Figure 4. The ACPL339J graph is drawn on base of the data given in [40]

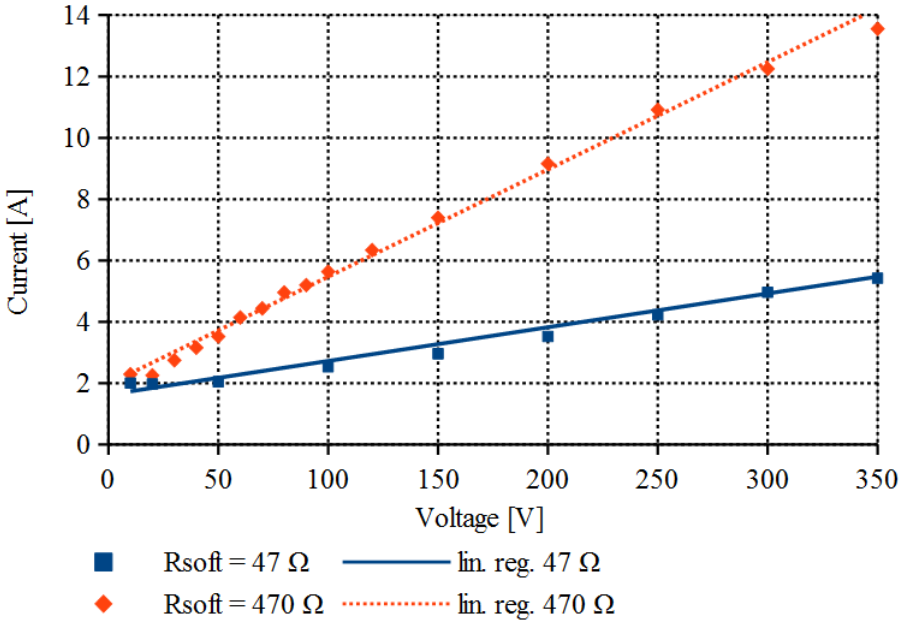

Fig. 33 Peak current depending on voltage and R_{soft}

Resistor R_{soft} needs to be set for the designed circuit not to prolong the on-time too much, but on the other hand to allow soft turn-off to prevent overvoltage.

The Fig. 34 shows how the over-current protection works with inductive load. In Fig. 35 it is shown the delay between over-current detection and the transistor turn-off. Fig. 36 shows the slow gate discharge that occurs when the over-current protection was tripped. The protection was set to 3 A.

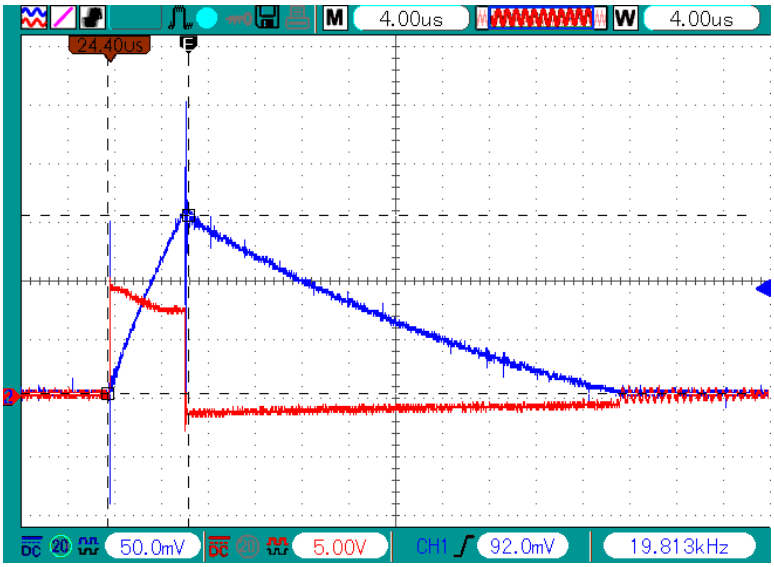

Fig. 34 Inductive load turn-off with the over-current protection set to 3 A, blue is current as 50mV/A and red is voltage across the load according to the Fig. 31

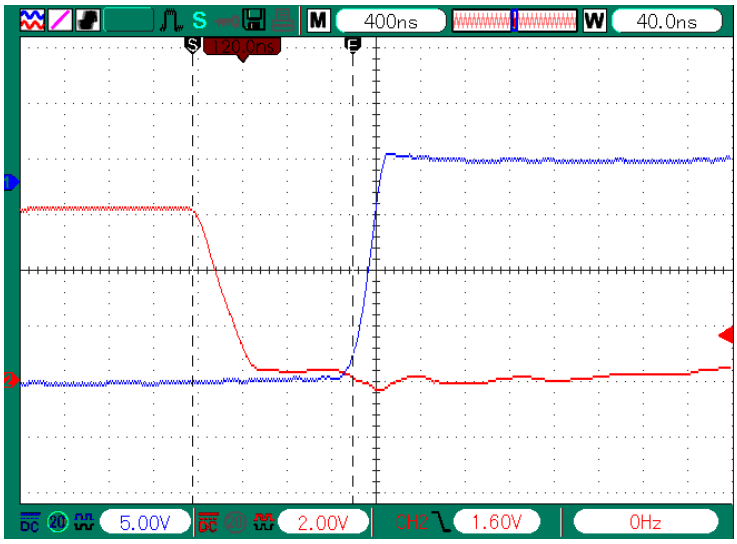

Fig. 35 Over current detection turn-off delay. Red line is the output of a comparator that detects the over current and the blue is voltage across the load (measured at different voltage than previous picture)

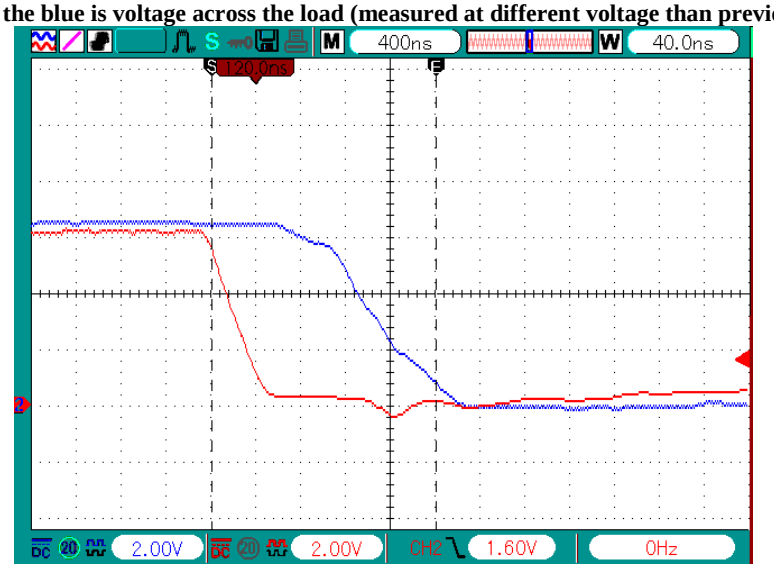

Fig. 36 Slow gate discharge after over-current detected. The blue is voltage at the gate and red comparator output to show when the over-current was detected

2.4 Discussion

One of the contributions to the driver's performance improvement is the development of the current limiting driver for GaN-based converters. The proposed driver for GaN transistor half-bridge has been designed and tested to meet the desired operation frequency range and to achieve properly turning off at the current limiting. The converter output short-circuit protection ensures the transistor operation within its entire output power range and exploits fully its capabilities.

In case of standard integrated drivers, the driver output stage limits the maximum switching frequency. The drivers' propagation delay has to be considered when using GaN transistors in power converters working at high frequencies. To increase the maximum operating frequency a faster driver output stage needs to be designed.

The proposed designed driver has 3 times faster response of desaturation protection compared to recently available fast drivers.

3 Cooling Possibilities of GaN Semiconductors

This chapter was partly published in Proceedings of the 2019 International Conference on Electrical Drives & Power Electronics, see [44].

According to [33], GaN technology brings lower on-state resistance R_{DSon} compared to other technologies. The dissipated power from the GaN device is lower compared to the others; however, the package of a typical GaN transistor is very small compared to its power rating [45]. The relatively small package brings new challenges in the device heat dissipation.

When designing high frequency converters, we want to keep current traces short to minimize parasitic inductances which results in compact design [46]. When placing the transistor as close as possible to the other components (typically DC-link capacitors or transformers), reasonable heat dissipation may become difficult. Given the small package size; without proper cooling systems, we can't usually reach the transistor manufacturer's recommended operating parameters.

Insulated metal substrate (IMS) board is frequently used in modern converters, however, it has some limitations. To ensure proper cooling, only one layer of copper is suitable for conductors. As a result, usually only the power stage is made using this technology.

To reach the benefits of operation at high frequency, the driver has to be fast, providing short rise/fall times and short delay times to ensure low pulse width distortion.

To prevent false turn-on, such as that caused by gate ringing [47] when discharging the gate at turning-off, the driver circuit must be placed close to the transistor to reduce parasitic inductance between driver and gate.

Compared to Si MOSFET, IGBT, and SiC MOSFET, the GaN gate needs significantly lower gate-to-source voltage, usually 5 V or 6 V maximum [34].

3.1 Description of Cooling Options

Three options of cooling GaN transistors are discussed and detailed figures are included. Also the comparison based on estimated thermal resistances of these variants is presented and compared with "five-side" cooling method from [48].

3.1.1 **Bottom Side Cooled GaN on IMS Board**

The bottom side cooled transistor [34] is placed on IMS PCB with aluminium core which is then mounted on a heatsink with an insulation layer according to Fig. 37.

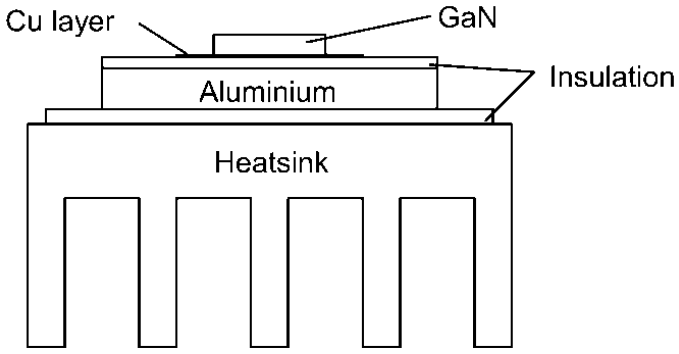

Fig. 37 Bottom side cooled transistor placed on IMS board

3.1.2 Top Side Cooled GaN

The top side cooled transistor [49] is in contact with the heatsink directly through an insulation material according to Fig. 38.

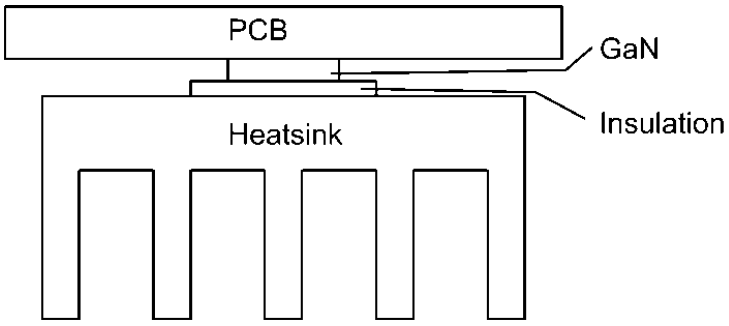

Fig. 38 Top side cooled transistor with heatsink

3.1.3 Bottom Side Cooled GaN on FR4 Board

The bottom side cooled transistor [34] is mounted on FR4 PCB according to Fig. 39. The heat is transferred through the board using vias placed under the transistor. On the bottom layer, the heat is spread into the copper layer. The heatsink is in contact with the PCB through an insulation material.

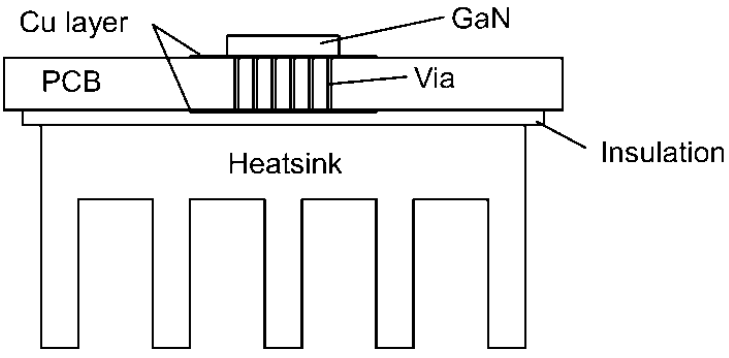

Fig. 39 Bottom side cooled transistor placed on FR4 board

3.1.4 Thermal Resistance Estimation

The estimated thermal resistance for each variant is compared in Tab. 5 with ”five-side“ cooling proposed in [48].

The temperature difference $\Delta\vartheta$ above ambient can be calculated from the dissipated power P_d and thermal resistance according to (1).

Junction to case thermal resistance R_{thjc} is obtained from transistor datasheets [34], [49], the same for top and bottom cooled versions. Case to heat-spreader resistance R_{thcs} and spreader to radiator resistance R_{thsr} are calculated according to (2) and (3) by using case and substrate area A_c, A_s, thickness l_c , l_s and relative conductivity λ of the insulation material.

For the top side cooled version, the heat-spreader is not used. Substrate to radiator thermal resistance R_{thsr} represents the thermally conductive material that must be used to isolate the heatsink from the transistor.

$$\Delta\vartheta = P_d \cdot \left(R_{thjc} + R_{thcs} + R_{thsr}\right) \quad (1)$$

$$R_{thcs} = \frac{l_{cs}}{A_c \cdot \lambda_{cs}} \quad (2)$$

$$R_{thsr} = \frac{l_{iso}}{A_s \cdot \lambda_{iso}} \quad (3)$$

Tab. 5 Estimated thermal resistances

Variant	R_{thjc} [K/W]	R_{thcs} [K/W]	R_{thsr} [K/W]	R_{thjr} [K/W]
Bottom on IMS	0.5	2.1	0.65	3.2
Top side cooled	0.5	-	8	8.5
Bottom on FR4	0.5	5.4	5	10.9
Five-side cooling [48]	0.56	-	10.3	10.9

According to Tab. 5, the calculated junction to radiator total resistance R_{thjr} is lower for the bottom side cooled transistor on IMS board compared to the top side cooled transistor. The R_{thsr} depends on the area of the insulation used for the heat transfer. The top side cooled transistor have no R_{thcs} but the area of the transistor itself is very small given the required power dissipation.

For the bottom cooled transistor on FR4, the R_{thcs} is caused by the thermal resistance of the vias. The heat can be better spread on the FR4 board but the thermal resistance of vias placed directly under the transistor package limits the possible thermal conductivity.

Transistor presented in [48] has higher R_{thjc}. When using the GS66508B [34] together with “five-side” cooling, the result (see Tab. 5) is expected to be better than the bottom side cooled variant on FR4 board.

3.2 Experimental Setup

The experimental DC/DC converter was designed to compare the three above-discussed cooling options. The board is equipped with transistors' footprints for all three variants to be directly comparable under similar conditions.

To equalize the switching losses, all variants have the same gate driving circuit consisting of a current protected driver measuring the saturation voltage such as in [50] and of a current buffer. In the case of the IMS board, the driver's output buffer stage is placed on the IMS board close to the GaN transistor to minimize the parasitic inductance in the gate path.

3.2.1 GaN on IMS Board

The primary idea was to adapt GaN into regular TO-247 package for compatibility with available Si and SiC transistors of the same power range.

The size of the TO-274 package limits the board size to 16 mm x 24 mm. This board must contain a hole for the screw or a place for the spring used to hold the transistor on the heatsink.

The other limitation is the fact that the board is made of conductive material, so the copper layer has to keep isolation distance from the edges of the board.

On regular TO-247 transistors, the back side is connected to the drain, while in this design, it increases drain to gate parasitic capacitance. The better option is to connect the IMS board metal to the source terminal.

The GaN transistor requires low parasitic inductance in the gate driving circuit to utilize the benefits of high frequency switching.

The proposed solution is to place a fast driver buffer on the IMS board close to the GaN transistor.

Such a driver must provide short propagation delays and short rise/fall times because its delays act in addition to the main driver circuit that supplies the gate when a regular TO-247 transistor is used.

To keep the board standalone, the driver power supply has to be sourced from the gate input. This is possible due to the low gate charge of GaN transistors and low power consumption of the driver. The presented solution is similar to the high-side driver bootstrap as can be seen in simple half-bridge converters where a capacitor is charged through a diode and supplies the driver during the off-time of the low-side transistor.

To adapt the gate-source voltage requirements of GaN to these of regular Si or SiC transistors, a voltage limitation circuit has to be added to prevent gate overvoltage.

The proposed schematic diagram is in Fig. 40. The board is connected through three terminals: gate, drain, and source as in case of regular transistors. The input voltage from the gate terminal that is usually supplied by a 15 V driver is limited by a Zener diode D2

to 5 V. This signal is used as the input of the fast driver MAX5048C. The driver supply voltage is stored in the capacitor C1.

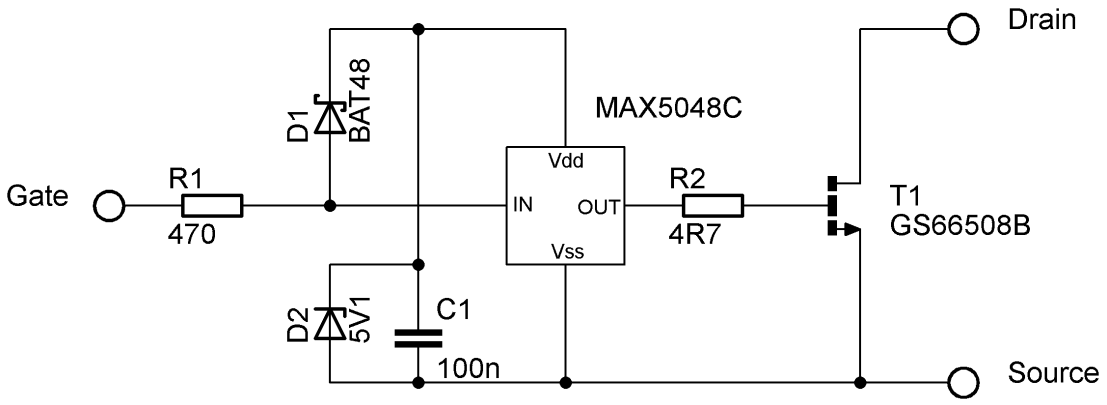

Fig. 40 Gate current buffer schematic diagram

When the transistor is turned on by the controller, the capacitor is charged through diode D1. A Schottky barrier diode was selected to minimize drop-out of the 5 V supply for the gate driver.

The benefits of the selected driver are its low power consumption and fast high current output. The driver is also equipped with under-voltage protection with built in safe pull-down resistor. This resistor is activated whenever the supply voltage is insufficient for safe operation and ensures the transistor proper turn-off.

The IMS board layout designed for GS66508B is shown in Fig. 41 and the finished board in Fig. 42. (Originally the Zener diode was placed right behind the R1 but its capacity was slowing the circuit so it was moved behind the D1 as on Fig. 40.)

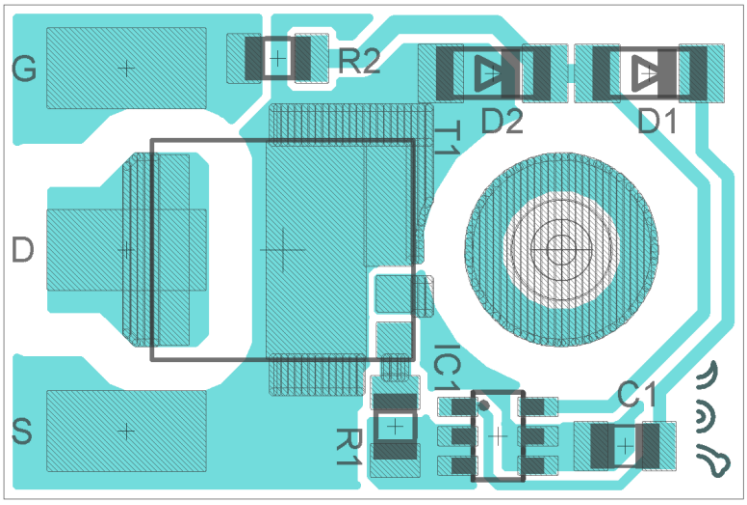

Fig. 41 IMS board layout

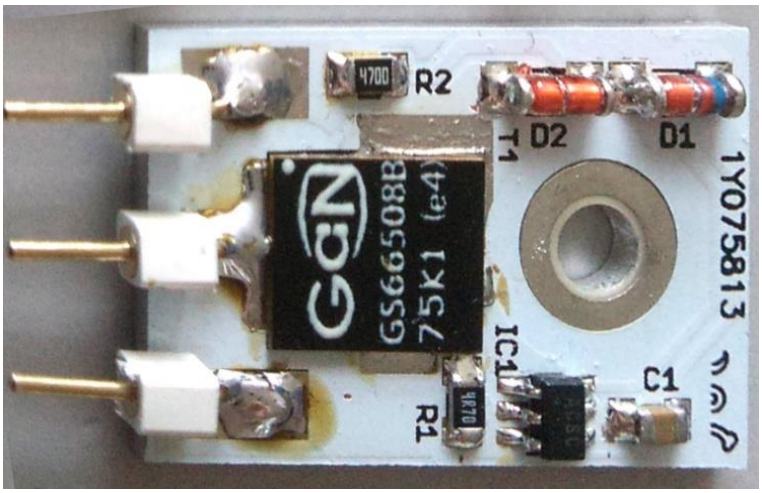

Fig. 42 Finished IMS board

3.3 Experimental Results

At measuring, the designed GaN driver is used in all three tested cooling configurations. The results obtained by measurement on realized experimental setup of all three cooling options are presented and compared.

3.3.1 Driver Verification

The finished boards were tested in a DC/DC converter topology and the measured results on the gate driver are presented in following figures.

Fig. 43 depicts the transistor gate to source voltage V_{GS} limited to 5 V independent of the board gate terminal input voltage V_{in} during the on-time.

The turn-on delay appears in Fig. 44 and turn-off delay in Fig. 45 measured as a time between V_{in} and V_{GS} transitions.

Measured turn-on delay is 15 ns and turn-off delay 35 ns.

The turn-on delay matches the datasheet parameter of MAX5048C. The turn-off delay is extended by 20 ns due to discharging of the parasitic capacitances in the circuit through the relatively high input resistance.

The input resistance may be reduced in order to shorten turn-off delay at the expense of increased dissipation during the on-state.

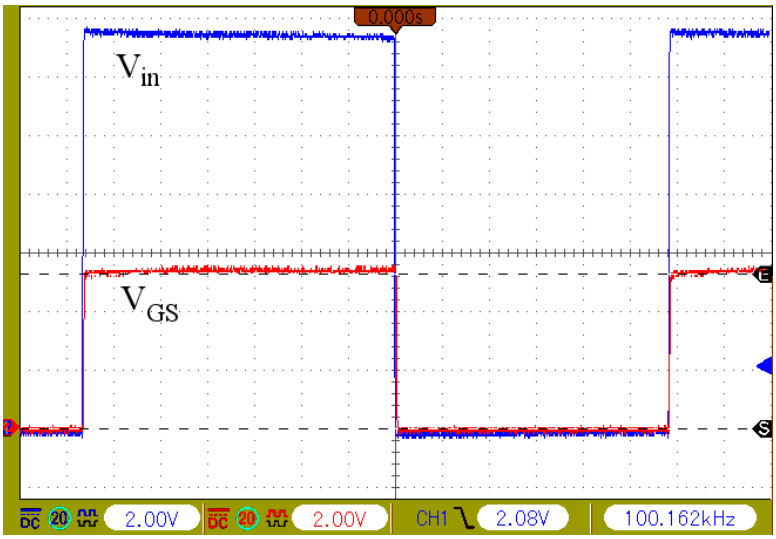

Fig. 43 Input voltage V_{in} on the current buffer gate terminal and V_{GS} measured on the GaN transistor 2 V/div, 1 µs/div

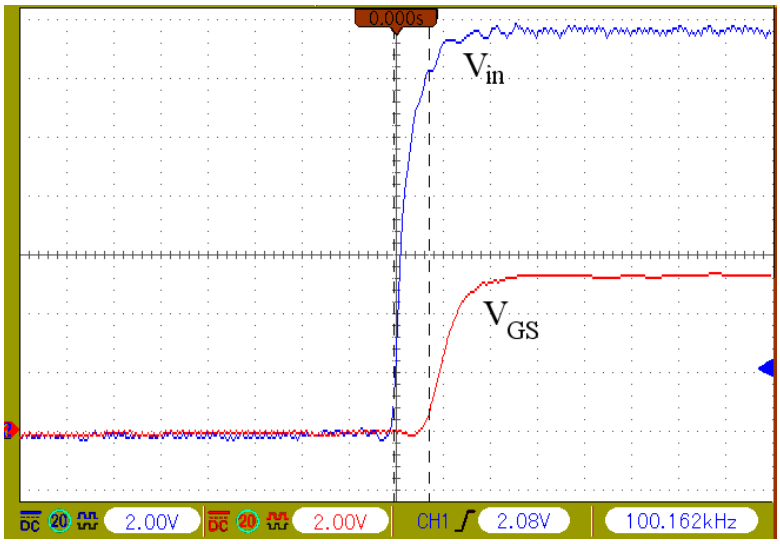

Fig. 44 Measured turn-on delay 15 ns

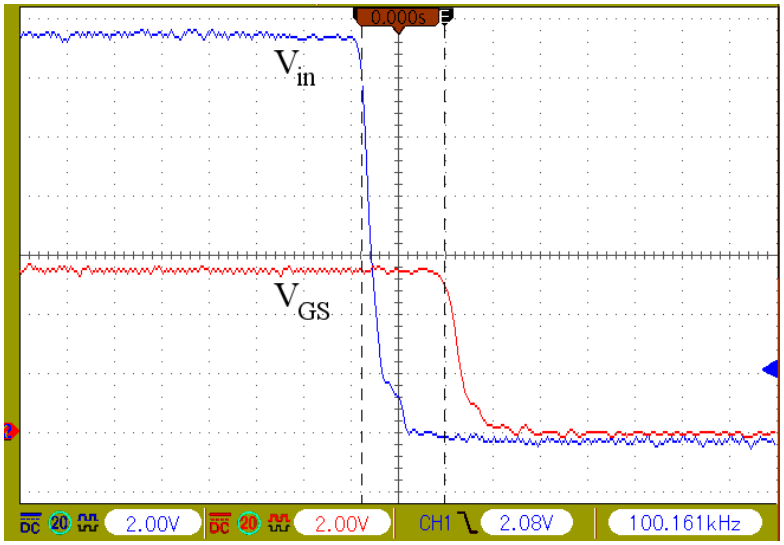

Fig. 45 Measured turn-off delay 35 ns

3.3.2 Cooling Options Comparison

The DC/DC converter designed for this purpose is a synchronous buck converter [36] with half-bridge using two GaN transistors and a working inductor on the output. It was designed based on the experience gained while working on [39].

The finished converters were connected in back-to-back configuration according to Fig. 46 to measure them at the equal transferred power in pairs.

Each converter is controlled by its own ARM Cortex M4 STM32F334 microcontroller. The controllers are equipped with high resolution timers [51] to provide precise control of dead-time. Such control is necessary for high efficiency when using GaN devices without substrate freewheeling diodes [52].

The precise dead-time control is necessary because we are using the reverse conduction region [45] of the GaN transistor instead of the freewheeling diode. It means that greater dead-time increases transistor's losses due to operating in reverse conduction region with high voltage drop.

The reason to forgo separate freewheeling diodes is that their reverse recovery losses can be removed. This is a way to increase converter efficiency and enable operation at high frequencies.

This converter topology, running at 400 kHz from 30 V input and 10 A on the output with 50 % duty cycle, achieved the total efficiency of 97 %.

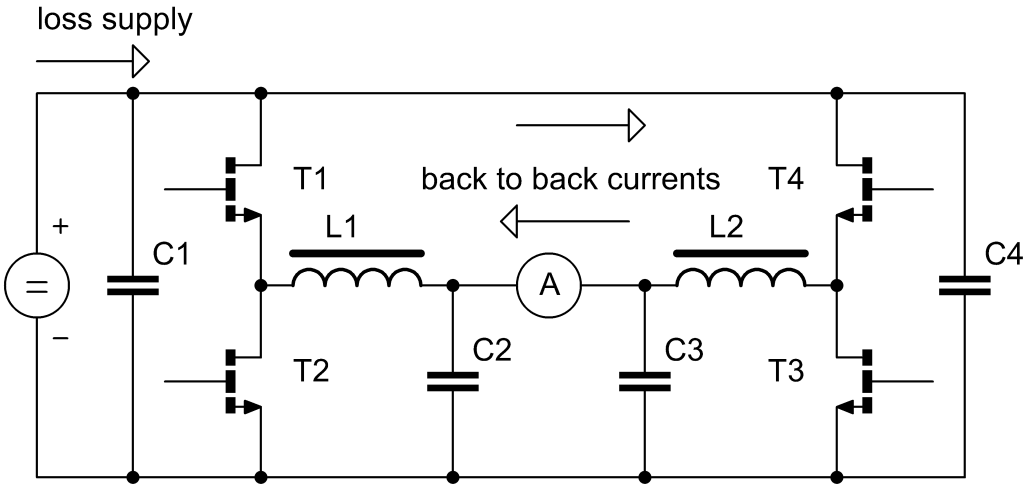

Fig. 46 Two converters in back-to-back configuration

All three realized converters (see Fig. 47) were equipped with relatively large heatsinks of the same size to provide enough thermal capacity to perform the measurement. For purposes of verification, both rise and fall temperature curves were measured to see if the temperature at the end of measurements will be equal for all variants.

The comparison of the rise and fall temperature curves of the three measured variants is shown in Fig. 48. At equal dissipated power, the bottom cooled transistor on IMS board reached half the temperature of the variant with the top side cooled transistor.

At the end of the measurement the temperature fall curve ends 2 K above the initial value. This means, the heatsink has enough capacity to provide reasonable data for a comparison of the junction to radiator resistances.

The bottom side cooled variant on IMS board is able to keep the junction temperature lower than the other variants. It enables the converter to run at higher power or with higher efficiency than the other variants at the same power. The latter being a result of the GaN transistor's R_{DSon} temperature dependence. This dependence affects the converter efficiency with increased temperature as investigated in [54].

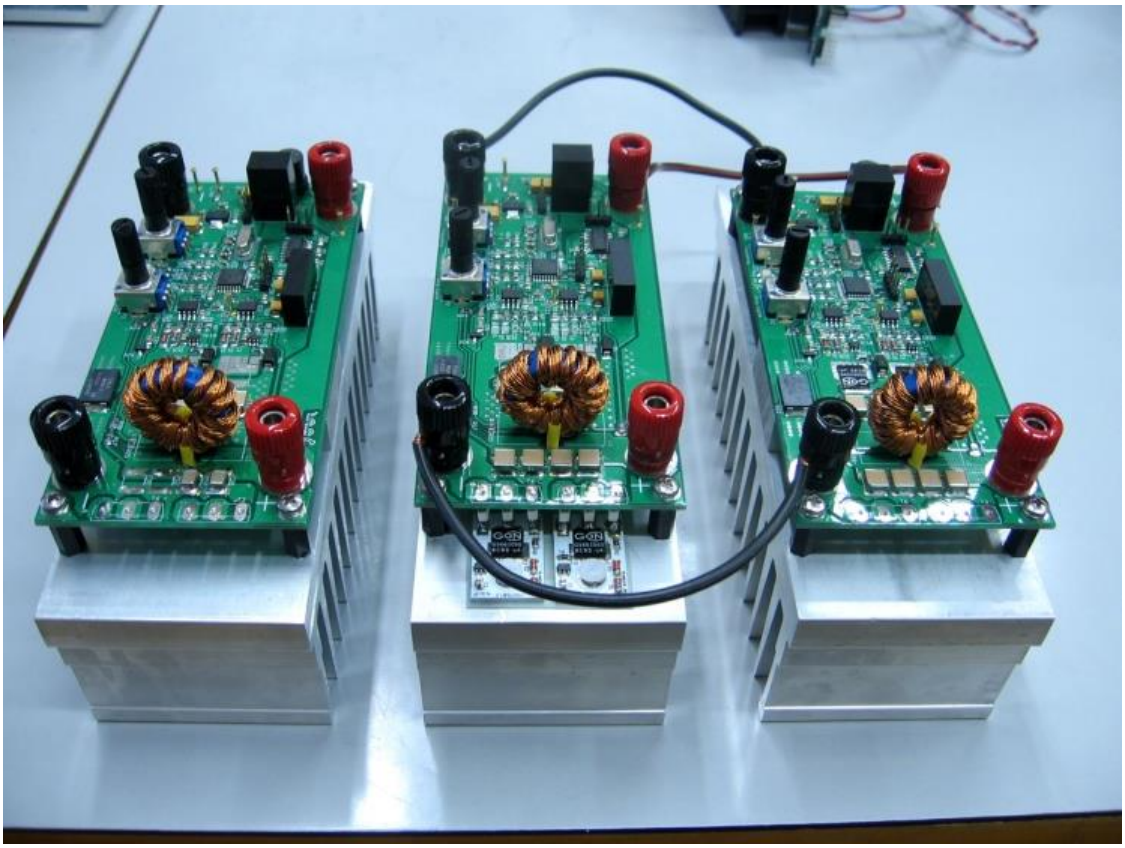

Fig. 47 Finished experimental converters: top side cooled variant (on the left), bottom side cooled on IMS board (in the middle), and bottom on FR4 board (on the right)

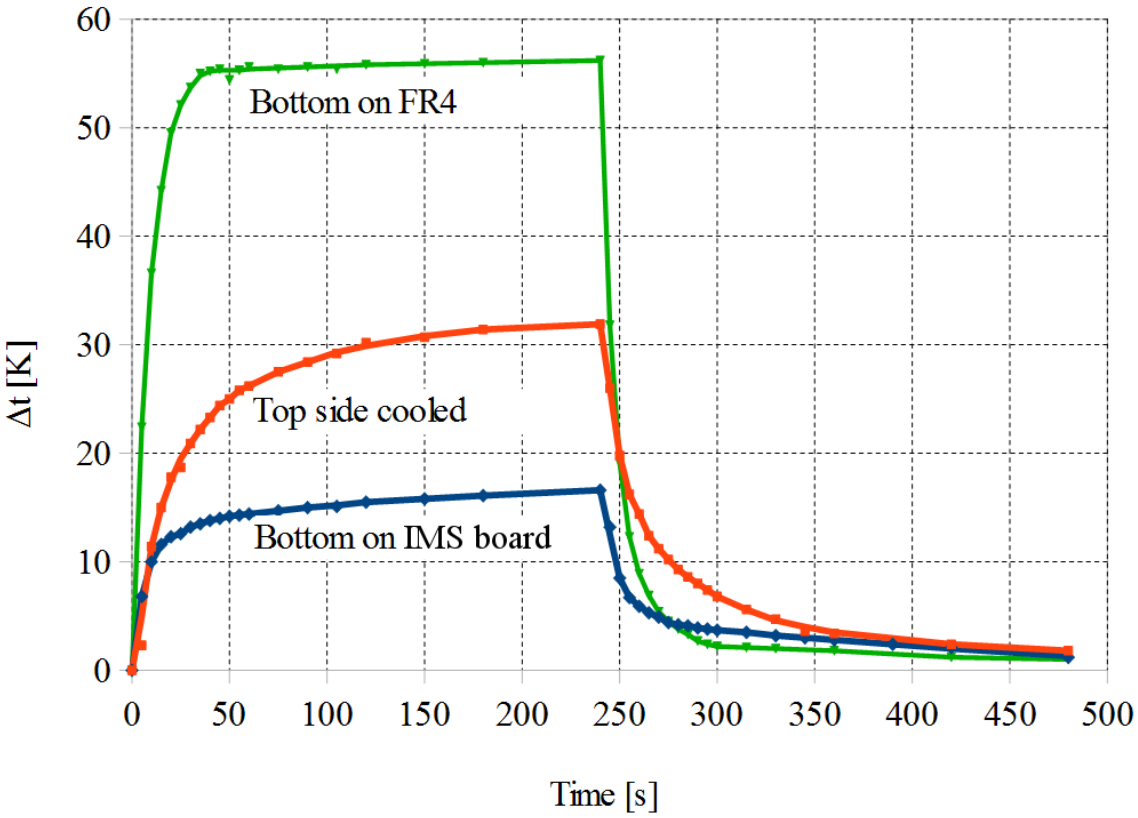

Fig. 48 Cooling options comparison

3.4 Discussion

Three methods of cooling the printed circuit board mounted GaN transistors were tested and compared together. Three converters were made and tested at the same power. The results are presented as transistors' steady state temperatures at given power level for each cooling method.

The important results in that the bottom side cooled transistor on IMS board reached only half the temperature compared to the top side cooled and four times lower temperature compared to the bottom side cooled transistor on FR4 board.

The presented solution for bottom side cooled GaN transistors was successfully tested in a DC/DC converter. The board design fits the dimension of regular TO-247 package used for Si and SiC MOSFETs and the circuitry enables adaptation of GaN transistors to be used directly in place of existing transistors with changes neither in the board design nor in driving circuits.

4 GaN Transistor Switch-On Loss Reduction

This chapter was partly published in journal Electronics, see [53].

GaN devices bring a few problems and challenges to the converter design and control stage. One of them is the so-called current collapse phenomenon that increases the conduction losses of power converters [45], [55].

By the current collapse, we mean resistance variations of the conductivity channel shortly after the transistor has been turned on [56]. This variation is caused by trapped electrical charge at the gate electrode of the GaN transistor structure in the off-state [57]. The amount of the charge is then dependent mainly on the DC-link voltage as reported in [58] for p-doped GaN. In hard-switched converters, this phenomenon increases the total losses approximately twice, meaning that the heatsink should be dimensioned differently than according to the datasheet parameters. This disadvantage often leads to the deployment of GaN transistors in small and low-power applications rather than electric drives (which are dominated by hard-switched converters) [59], [60].

Various papers try to model the current collapse in GaN devices to better comprehend its behaviour with respect to the operating conditions such as the transistor blocking voltage [61], [62]. The phenomenon is also being extensively measured on various structures [63]. There are also current-collapse-free GaN transistors under development [64], [65]. However, presently available GaN devices still exhibit the deteriorated behaviour caused by the increased on-state resistance.

Several approaches to reducing the losses caused by the current collapse phenomenon have been proposed in the literature. Most solutions are based on hardware (HW) modification, with the most significant being the utilization of soft-switching [66]. However, this technique complicates the converter circuit and usually doubles the number of transistors and inductors [67].

Generally, when speaking about specific problems connected with power electronic converters, software-based solutions are always preferred over hardware ones since hardware solutions complicate the resulting circuitry and increase the cost and volume of the converter. Therefore, a simple approach that mitigates the current-collapse losses of hard-switched three-phase two-level voltage-source GaN inverters (VSI) is presented. The solution is based on the author's static measurements [68] and utilizes the classical 7-segment space-vector pulse-width modulation (SVPWM) modified to omit short gate pulses when the reference vector approaches the voltage limit. The presented control algorithm operates with optimum modulation based on an offline measured look-up table (LUT) over the whole power range of the drive. The proposed method is suitable mainly for control strategies that do not need the knowledge of the stator voltage vector since it brings voltage distortion at high modulation index values. The presented approach is validated within a field-oriented control (FOC) of a 0.5 kW permanent magnet synchronous motor (PMSM) drive fed by GaN VSI.

4.1 Theoretical Analysis

The three-phase VSI in Fig. 49 is a hard-switched type of converter. It means that each time one transistor in one leg is turned on and the other is turned off, there is a blocking voltage equal to the DC-link voltage present across the non-conducting transistor. Due to this type of operation (i.e., switching during "high" blocking voltage), the GaN transistor suffers from the current-collapse phenomenon, which causes higher on-state resistance right after each turn-on process [62]. The resistance increase depends on the blocking voltage magnitude, current polarity, and gate pulse width. The behaviour of dynamic on-state resistance R_{DSon} is illustrated in Fig. 50.

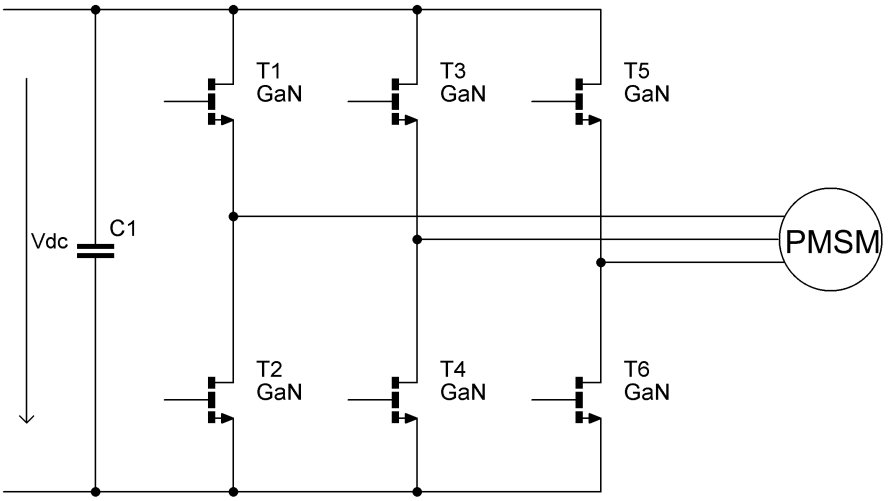

Fig. 49 Three-phase two-level GaN voltage-source inverter

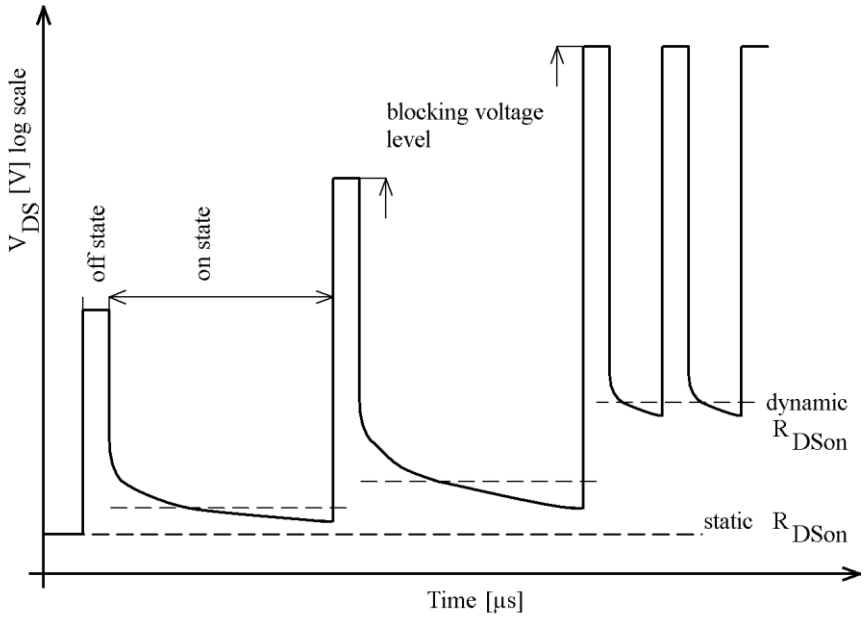

Fig. 50 Current-collapse effect on the GaN on-state resistance

In Fig. 50, the transistor is turned on at the beginning with the static R_{DSon} value. After the transistor is turned off and a blocking voltage of a certain level for a certain amount of time is applied across the transistor, the following turn-on process increases the dynamic R_{DSon} because of the trapped charge around the gate that leads to the channel resistance increase.

The resistance remains relatively high until the parasitic charge is removed. The dynamic R_{DSon} is then dependent on the blocking voltage level to which the transistor structure is exposed. The situation is illustrated within the second pulse in Fig. 50. When the turn-on duration is short, there is not enough time for the trapped charge to be removed, and dynamic R_{DSon} gets significantly higher as shown by the last two pulses in Fig. 50. The most significant part of the additional resistance is the channel's resistance, which is determined by the volt-ampere characteristic of the transistor.

Concerning the channel current i_{ch}, it is usually expressed in the literature as [59]

$$i_{\mathrm{ch}} = g_{\mathrm{m}}(V_{\mathrm{GS}} - V_{\mathrm{GS(th)}}), \tag{4}$$

where g_{m} is the device transconductance, V_{GS} applied gate voltage from the driver, and $V_{\mathrm{GS(th)}}$ the threshold voltage. During the current-collapse, both g_{m} and V_{th} are affected when the structure is exposed to a higher blocking voltage before the turn-on process. The transconductance is decreased and the gate threshold biased to a higher value. In consequence, the transistor acts as it would receive a gate pulse of an insufficient voltage level (i.e., as it would work in a linear mode).

The contribution of the R_{DSon} resistance to the conduction losses can then be analytically expressed as [59]

$$P_{\mathrm{cond}} = R_{\mathrm{DSon}} i_{\mathrm{DS}}^2, \tag{5}$$

$$P_{\mathrm{cond}} = \frac{1}{T}\sum_{i=0}^{N} R_{\mathrm{DSon}(i)} i_{\mathrm{DS}(i)}^2 t_{\mathrm{on}(i)}, \tag{6}$$

where T is the switching period, N is the number of pulses per switching period, $R_{\mathrm{DSon}(i)}$ is the on-state resistance during the pulse, $i_{\mathrm{DS}(i)}$ is the current flowing through the transistor, and $t_{\mathrm{on}(i)}$ is the turn-on time for which the power losses are calculated. The problems, their causes, and the possible solutions connected with the current-collapse phenomenon are described briefly in Fig. 51.

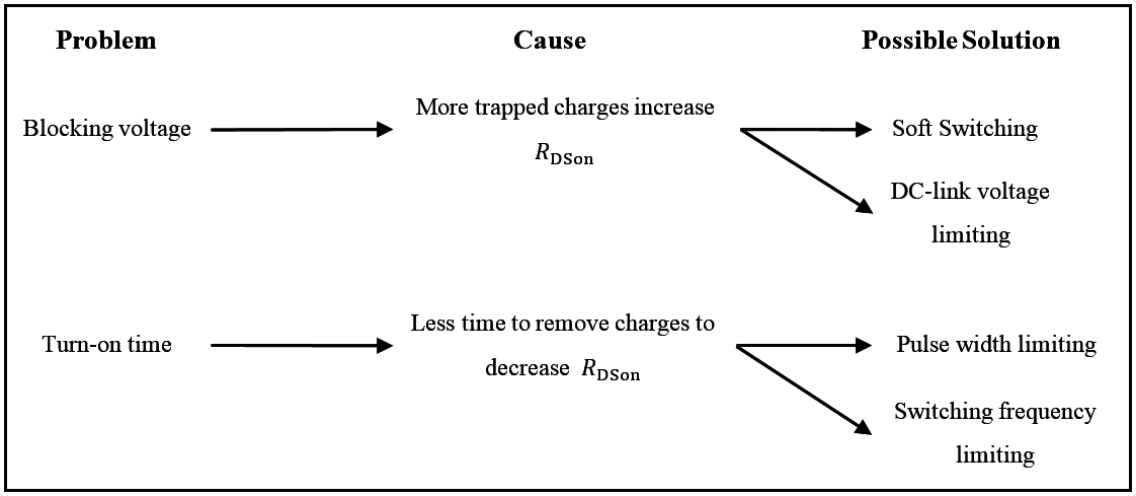

Fig. 51 Problems connected with current collapse, their causes, and possible solutions

Soft switching is a very effective method in decreasing the conduction losses; however, it requires additional hardware to be added to the converter, approximately doubling the resulting number of transistors. The blocking voltage regulation can also mitigate the effect of current collapse. However, it requires the possibility to change the VSI DC-link voltage value, which may result in the presence of an additional converter. This technique is sometimes used to decrease motor losses when the drive works with variable load and under variable speed conditions [69].

Decreasing the switching frequency is often used in medium and high-power silicon-based converters to minimize the switching losses. However, in the case of GaN converters, it is generally desirable to keep the switching frequency constant and as high as possible to fully utilize the potential of the GaN devices (i.e., benefits such as easy filtering and smoothing of the motor current waveform by the motor leakage inductance [70]).

Following the above analysis, the motivation is to avoid the converter topology modification and the reduction of the switching frequency. Therefore, the solution that will be described in more detail in the following sections is purely software-based and utilizes the modification of the SVPWM pattern.

4.1.1 Space-Vector Modulation with Minimum Pulse Width Limitation

SVPWM is a popular modulation strategy that is extensively used in electric drives. In a linear mode, it maximizes the DC-link voltage utilization, i.e., increases the modulation index compared to other modulation types while keeping undistorted sinusoidal waveforms of the motor line-to-line voltages [71].

Considering the three-phase reference line-to-neutral motor voltages and the resulting duty cycles for each VSI leg, mathematically, the modulation can be written as [72]

$$v_\mathrm{A} > v_\mathrm{B} > v_\mathrm{C} \quad \text{or} \quad v_\mathrm{C} > v_\mathrm{B} > v_\mathrm{A} \begin{cases} d_\mathrm{A} = \frac{(v_\mathrm{A} - v_\mathrm{C})}{2v_\mathrm{DC}} \\ d_\mathrm{B} = \frac{(2v_\mathrm{B} - v_\mathrm{A} - v_\mathrm{C})}{2v_\mathrm{DC}} \\ d_\mathrm{C} = \frac{(v_\mathrm{C} - v_\mathrm{A})}{2v_\mathrm{DC}} \end{cases}, \tag{7}$$

$$v_\mathrm{B} > v_\mathrm{A} > v_\mathrm{C} \quad \text{or} \quad v_\mathrm{C} > v_\mathrm{A} > v_\mathrm{B} \begin{cases} d_\mathrm{A} = \frac{(2v_\mathrm{A} - v_\mathrm{B} - v_\mathrm{C})}{2v_\mathrm{DC}} \\ d_\mathrm{B} = \frac{(v_\mathrm{B} - v_\mathrm{C})}{2v_\mathrm{DC}} \\ d_\mathrm{C} = \frac{(\mathrm{v_C} - v_\mathrm{B})}{2v_\mathrm{DC}} \end{cases}, \tag{8}$$

$$v_\mathrm{A} > v_\mathrm{C} > v_\mathrm{B} \quad \text{or} \quad v_\mathrm{B} > v_\mathrm{C} > v_\mathrm{A} \begin{cases} d_\mathrm{A} = \frac{(v_\mathrm{A} - v_\mathrm{B})}{2v_\mathrm{DC}} \\ d_\mathrm{B} = \frac{(v_\mathrm{B} - v_\mathrm{A})}{2v_\mathrm{DC}} \\ d_\mathrm{C} = \frac{(2v_\mathrm{C} - v_\mathrm{A} - v_\mathrm{B})}{2v_\mathrm{DC}} \end{cases}, \tag{9}$$

where d_A , d_B, d_C are the modulator output duty cycles (i.e., the values that are compared with the triangular carrier signal in the microprocessor – the minimum duty cycle corresponds to the bottom and the maximum duty cycle corresponds to the top of the PWM up-down counter), v_A, v_B, v_C are the three-phase voltages demanded by the superior control system, and v_DC is the DC-link voltage.

To reduce the current-collapse conduction losses, the SVPWM is modified to exclude short pulses of a given time duration. Fig. 52 (a) shows the duty cycle d_A , d_B, d_C for each inverter leg including the sinusoidal output $d_\mathrm{A} - d_\mathrm{B}$ which represents the relative output line-to-line voltage between the phases A and B. Fig. 52 (a) shows the duty cycle waveforms in a linear mode and Fig. 52 (b) with the 5 % percent pulse width limitation.

The duty cycle is equally limited in all the output phases. Depending on the limiting value d_limit, the modulation is adjusted as

$$d'_x = \begin{cases} d_x & \text{... if} \quad d_x > d_\mathrm{limit} \\ 0 & \text{... if} \quad d_x < d_\mathrm{limit} \\ 1 & \text{... if} \quad (1 - d_x) < d_\mathrm{limit} \end{cases} \qquad x = \mathrm{A, B, C.} \tag{10}$$

Unfortunately, the technique of short pulses reduction results in the deformation of the motor voltage. The voltage vector deformation is shown in Fig. 53 (a) for the case of a stationary $\alpha\beta$ reference frame and in Fig. 53 (b) for the case of a synchronous dq reference frame. However, if only the basic sensored FOC is considered, the current controllers compensate for this distortion by adjusting the reference d and q-axis voltage components.

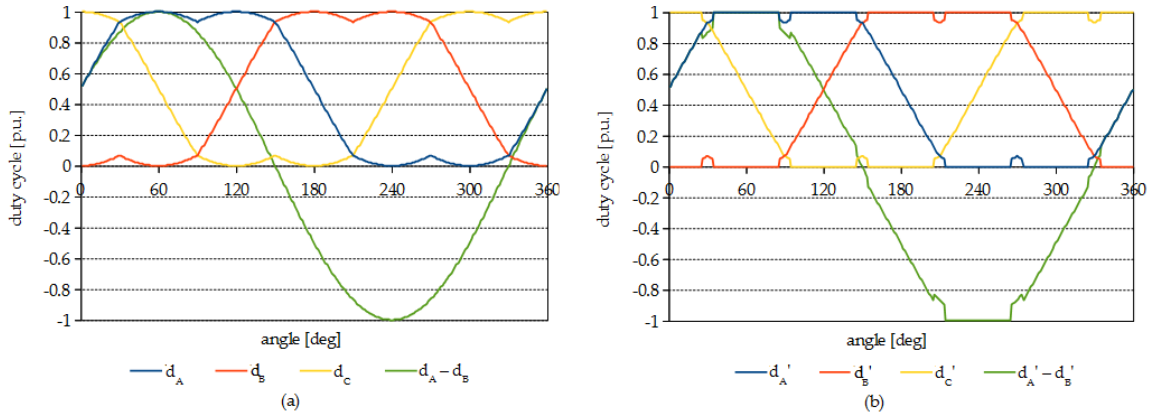

Fig. 52 SVPWM in (a) linear mode, (b) deformed SVPWM with 5 % pulse width limitation

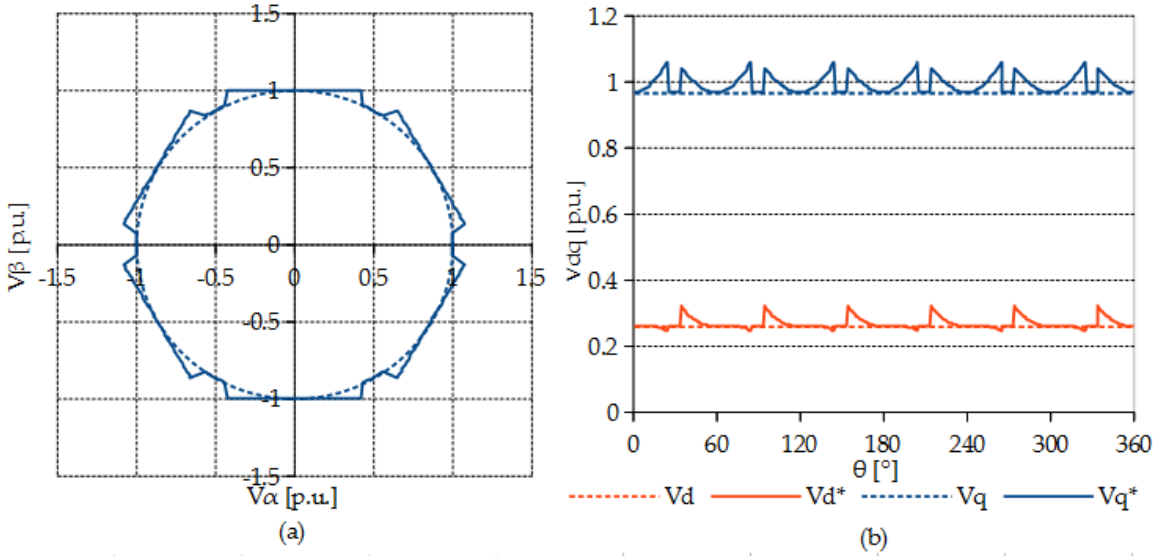

Fig. 53 Deformation of the voltage vector caused by the pulse width limiting set to 5 % of the duty cycle at a load angle of 15° (PMSM from the experimental part is considered)

4.1.2 Drive Losses Analysis

If the losses of the DC-link voltage source are neglected, the total drive losses can be divided into converter and motor losses. Limiting the minimum pulse width decreases the losses caused by the current collapse and increases the motor losses. The increase in motor losses is caused mainly by the additional iron losses since the voltage distortion introduces the current distortion, leading to distorted flux density distribution in the machine core [69]. Therefore, the aim is to find an optimum minimum pulse width that mitigates the negative influence of the current collapse and, at the same time, does not significantly increase the machine losses. The situation is depicted in Fig. 54.

4.1.3 PMSM Control Strategy

The block diagram of the PMSM control scheme is depicted in Fig. 55. It is based on the traditional FOC, where the machine torque is controlled by the q-axis and the machine flux by the d-axis current component. The transformation angle between the stationary $\alpha\beta$ and the synchronous dq system attached to the rotor permanent magnet axis is

measured using an incremental encoder. The control algorithm also implements a speed controller superior to the q-axis current controller to achieve required mechanical operating points (a permanent magnet generator loads PMSM with resistance connected to the stator winding). The speed controller is also used to calculate the d-axis current reference in the field-weakening region according to the strategy presented in [73].

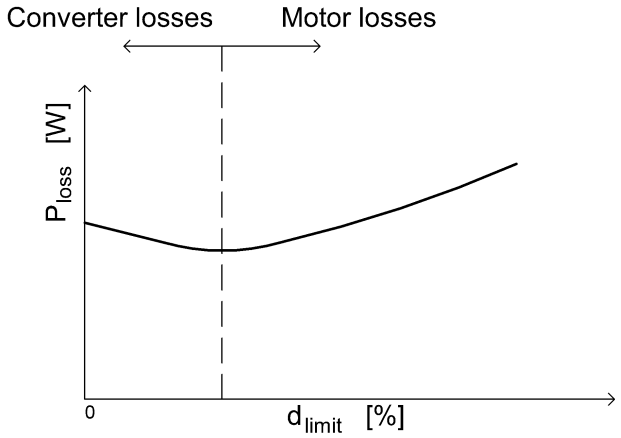

Fig. 54 Electric drive loss distribution based on the duty cycle pulse width limit value

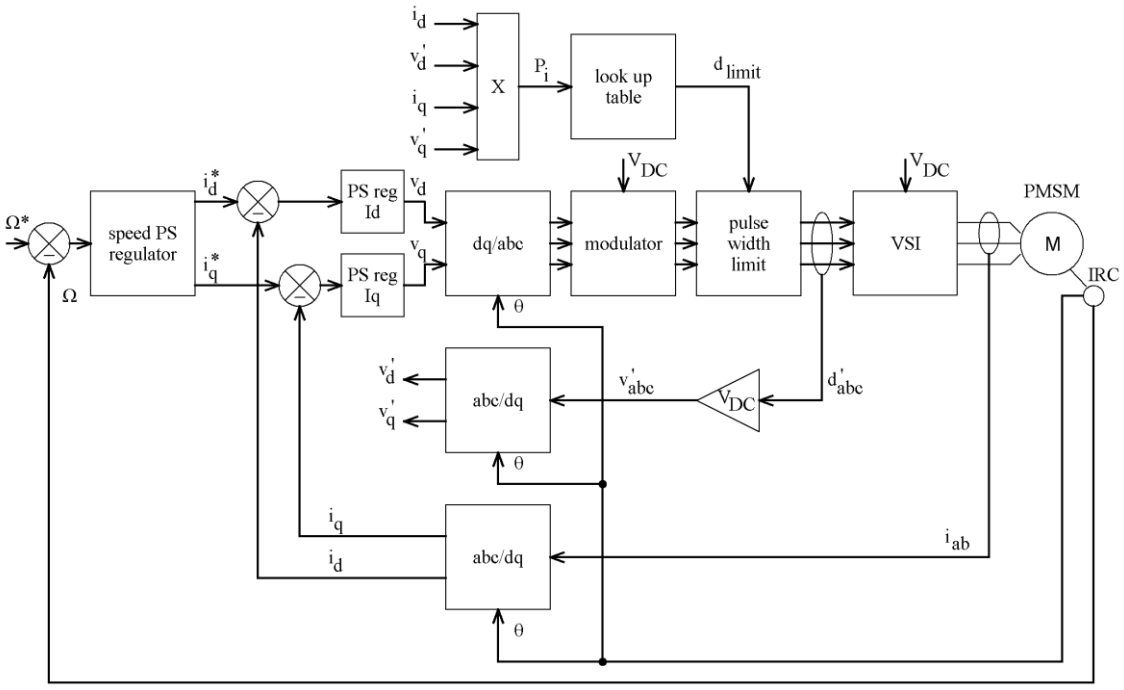

Fig. 55 PMSM control scheme with added LUT-based pulse width limiting block

The reference voltage vector demanded by the current controllers is transformed to the three-phase system and fed to the modulator. The modulator output then enters the pulse limiting block. The limiting value is derived from a LUT based on motor active power calculated as

$$P = \frac{3}{2}\left(i_d v_d + i_q v_q\right), \tag{11}$$

where i_d and i_q are the d- and q-axis stator current vector components, respectively, and u_d and u_q are the d- and q-axis stator voltage vector components, respectively. The LUT is experimentally measured with respect to the machine input power since increased mechanical power on the shaft means increased motor speed and, therefore, higher supply voltage (i.e., higher modulation index) with shorter gate pulses. Thus, in Fig. 55, the voltage components reconstructed from the adjusted duty cycles are used for the motor input power calculation since, due to the voltage distortion introduced by the proposed method, the outputs from the current controllers differ from the actual voltage applied to the motor terminals.

4.2 Experimental Results

The experimental setup is pictured in Fig. 56. The workplace consists of a custom GaN VSI, two identical mechanically coupled PMSMs, a regulated DC supply, and a resistive bank used for the PMSM generator loading.

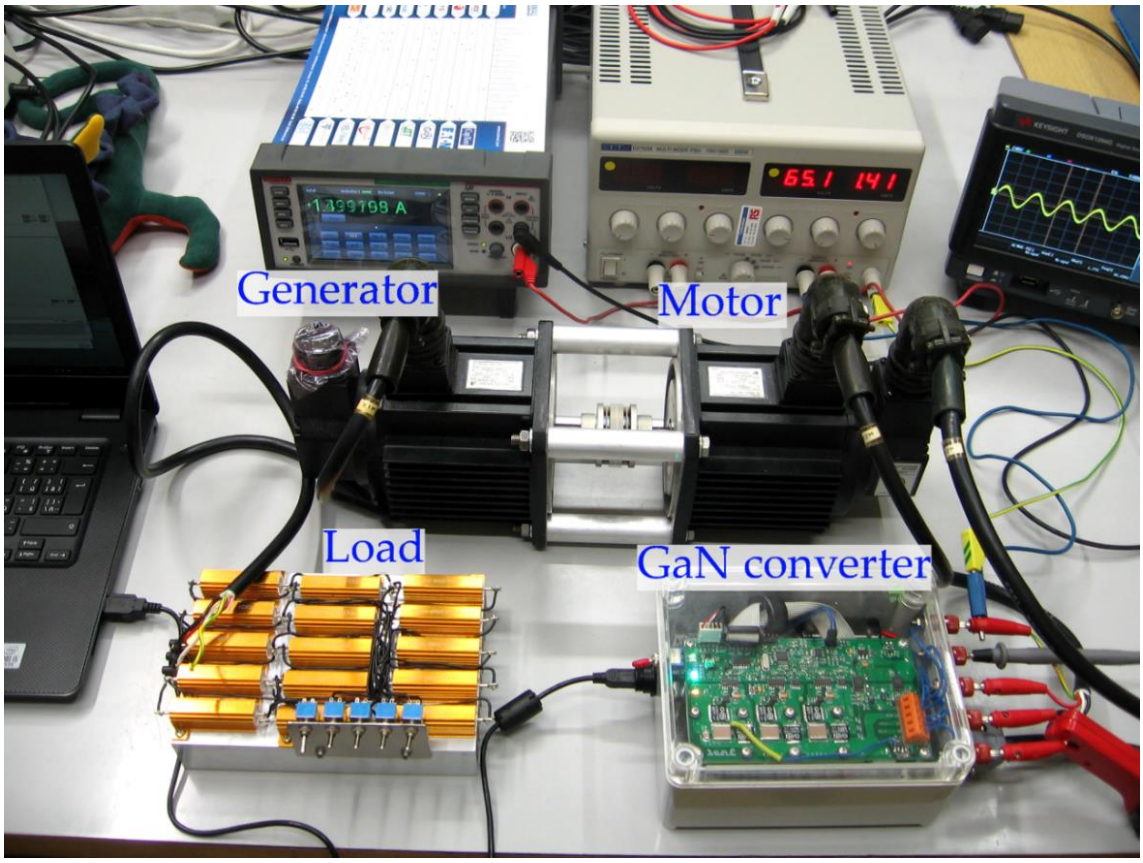

Fig. 56 Experimental setup

4.2.1 Experimental Setup

Fig. 57 shows a simplified block diagram of the experimental setup. The VSI is based on six GS66516B GaN transistors with Si8275 isolated half-bridge drivers and operates at a switching frequency of 100 kHz. The machine phase currents are measured by two TMSC1100 isolated hall-effect current transducers with low DC offset and an internal compensation circuit. The utilized ARM Cortex M4 microcontroller STM32F334 is

equipped with a high-resolution timer peripheral – a 16-bit timer with up to 217 ps resolution available for the duty cycle adjustment.

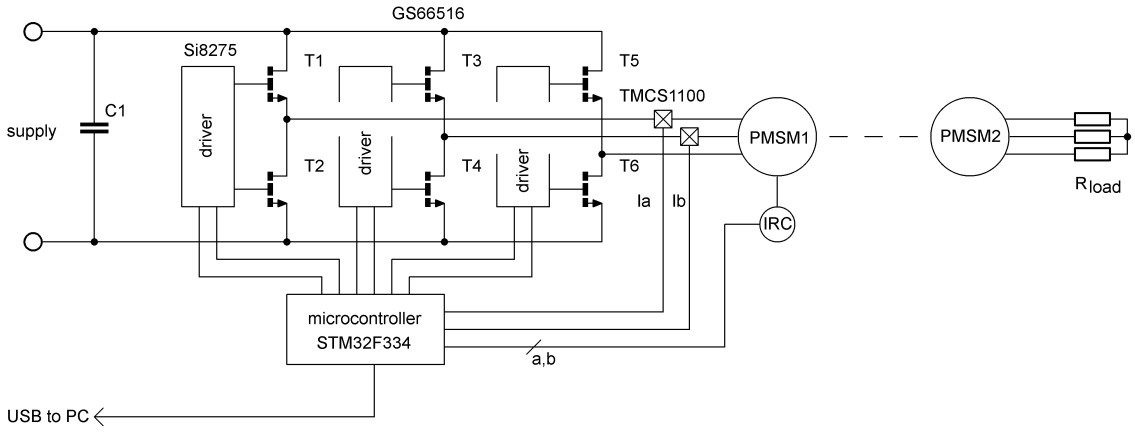

Fig. 57 Simplified schematic diagram of the experimental setup

Both the motor control algorithm and the data sampling run at 25 kHz. The GaN VSI supplies a 500 W four-pole PMSM with an incremental encoder for the rotor position measurement. The motor is then coupled to a second identical machine loaded by variable resistors. The nameplate data and model parameters of both machines are listed in Tab. 6

Tab. 6 Motor and generator parameters

Motor/Generator	
Type	USAREM-05CFJ11
RPM	3000
Power [W]	500
Max voltage [V]	200
Max current [A]	3.6
Stator resistance [Ω]	1.63
d-axis inductance [mH]	10.3
q-axis inductance [mH]	10.9

4.2.2 **Pulse Width Limiting**

Fig. 58 shows the recorded waveforms of the reference duty cycles and resulting machine phase currents for multiple pulse width limit values. The nominal duty cycle of 100 % is considered as the theoretical maximum in a linear modulation region. The minimum pulse width limiting process leads to the distortion of the reference duty cycle, which then contributes to the voltage vector trajectory distortion, as shown earlier in Fig. 53. For high values of pulse limitation, the duty cycle practically approaches a trapezoidal waveform. However, since the switching frequency is very high, the voltage distortion contributes to the current distortion only slightly.

4.2.3 Current-Collapse Loss Minimization

Because the DC-link voltage is kept at a constant value of 100 V by the regulated DC supply, the current drawn from the DC source directly contributes to the power consumption. Therefore, the DC-link input current for multiple drive operating points and minimum pulse width limit values to get the energy saved by the proposed method were measured. Since both motor and generator PMSMs are manufactured as servo drives, 100 V supply voltage was chosen with respect to the mechanical limits of the system so the PMSM drive could work in the base-speed region as well as in the field-weakening region within its nominal RPM.

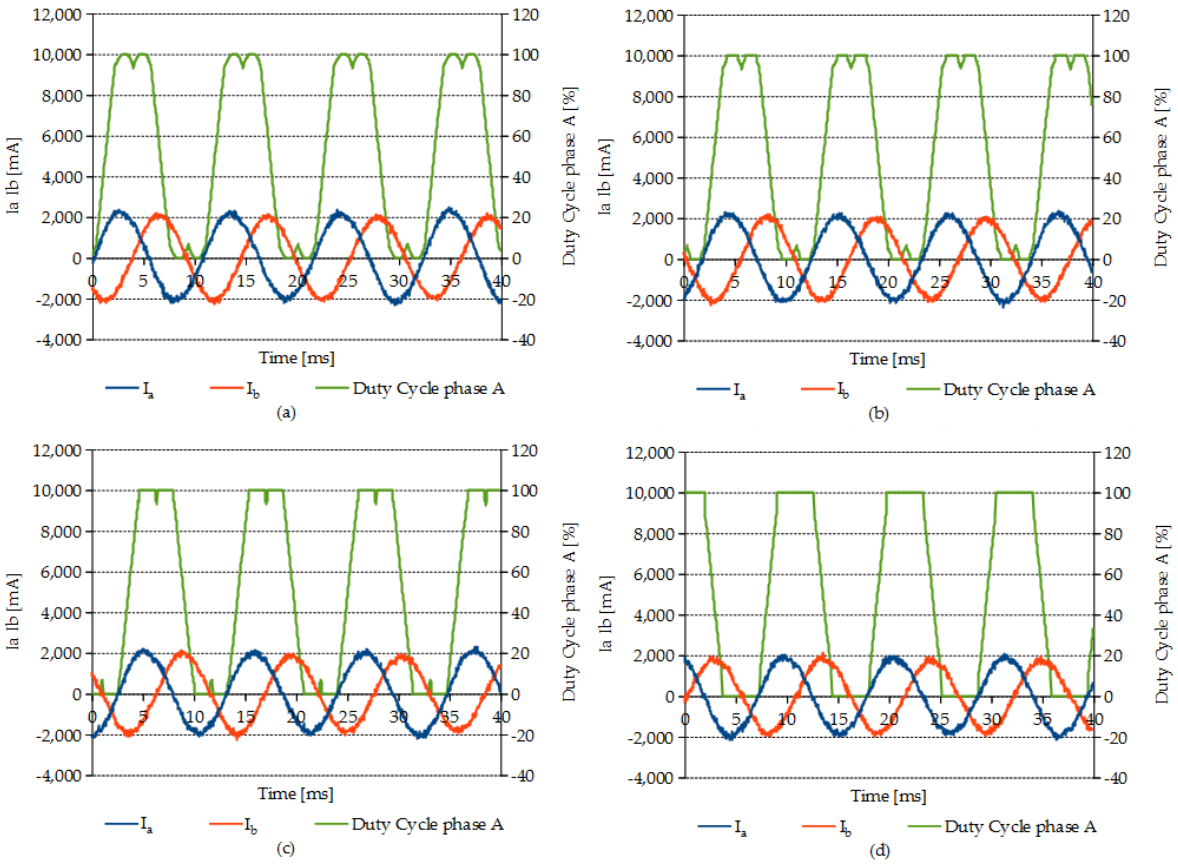

Fig. 58 Modulation with: (a) no pulse width limited, (b) with the limiting value 5 %, and (c) with the limiting value 10 % of the nominal duty cycle. Reference speed 2000 RPM, 100 V DC-link voltage, load resistance R_{load} = 100 Ω

The recorded data are depicted in Fig. 59. Fig. 59 (a) and Fig. 59 (b) are measured for a motoring operation in the base-speed region. Fig. 59 (c) then corresponds to the field-weakening region. As expected, the DC-link current increases with increasing the motor speed and decreasing the load resistance.

To give a better insight into the shape of the measured waveforms and the minima's position, Fig. 60 is converted into a per-unit system. The base value is different for each reference speed and corresponds to the DC-link current drawn without pulse width limitation. The results are then shown in Fig. 60.

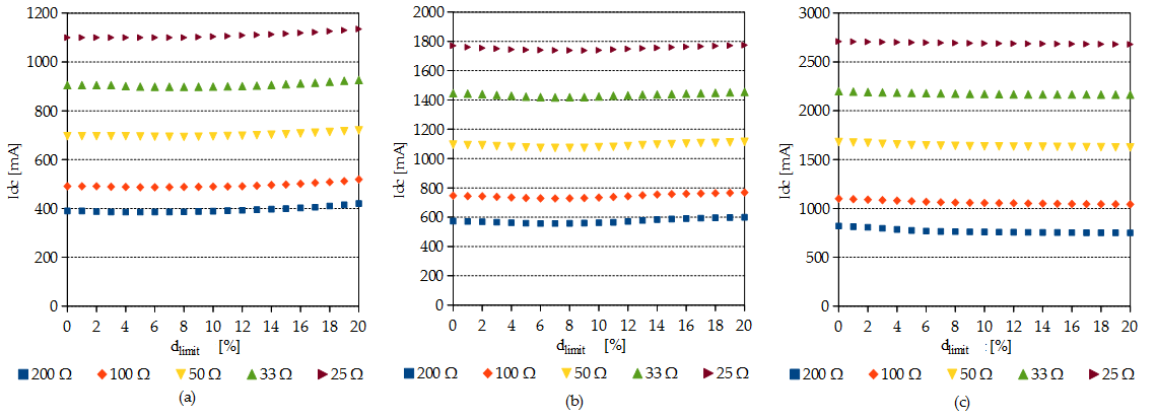

Fig. 59. Input DC-link current measured for different loads at (a) 1500 RPM, (b) 2000 RPM, and (c) 2500 RPM

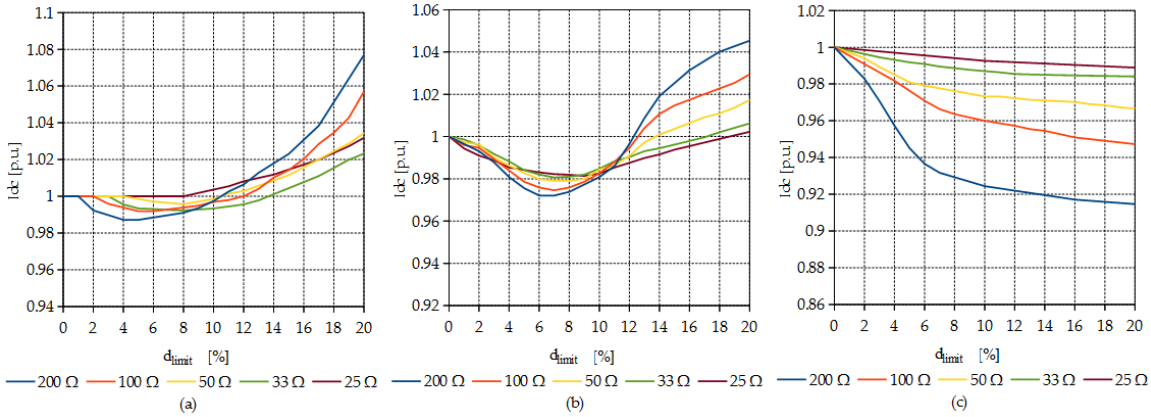

Fig. 60 Relative input DC-link current measured for different loads at (a) 1500 RPM, (b) 2000 RPM, and (c) 2500 RPM

In Fig. 60 (a), the motor load is low, resulting in a significant increase of the drive losses when the pulse width limit greater than 10 % is applied. Because the output power is also low, the decrease in converter losses is lower than the increase in motor losses due to the current distortion. Fig. 60 (b) shows that a more pronounced local minimum exists in the DC-link current for a certain pulse width limit at higher speeds since the voltage margin of the inverter decreases (more voltage is needed to counter the back-electromotive force) and, therefore, the reference voltage vector gets closer to the hexagon boundary. In Fig. 60 (c), the machine is operated in a field-weakening. In this case, the local minima do not exist in the DC-link current waveforms. The cause of this behaviour is that the modulation index, which is increased due to the pulse width limiting, lowers the d-axis current, which results in a decrease of motor phase RMS current value. The reduction of stator ohmic losses in the field-weakening region is more significant than the increase core losses; therefore, the curves have a continuously decreasing tendency.

Overall, it can be stated that the proposed method is most effective when the reference speed approaches the boundary between the base-speed and field-weakening region and the load is low. The relative decrease in the consumed power is 2 to 3 % in such a case. For lower speed, the maximum power savings are around 1 % in the case of

a low-load operation and are almost negligible for a high-load operation. Finally, it can be stated that the method lacks effectivity in the field-weakening region since here the local minima practically do not exist. The curves have a continuously descending tendency, but the decrease in current consumption, as explained above, is not caused by the mitigation of the current-collapse phenomenon.

As a final stage of the experiments, a LUT was determined for a variable inverter output power. During this measurement, the motor was running at 2000 RPM, and the load was varied in steps from 10 % to 100 % of the nominal torque. Again, the GaN VSI was supplied by 100 V DC.

The results are depicted in Fig. 61, which shows the measured values fitted by a polynomial function. The general form of the utilized function is given by

$$y = ax^3 - b\,x^2 + cx, \tag{12}$$

where a, b, and c are parameters to be determined. The fitting process was done using *Wolfram Mathematica*, and the found values are $a = 8.102$, $b = 24.74$, and $c = 28.79$.

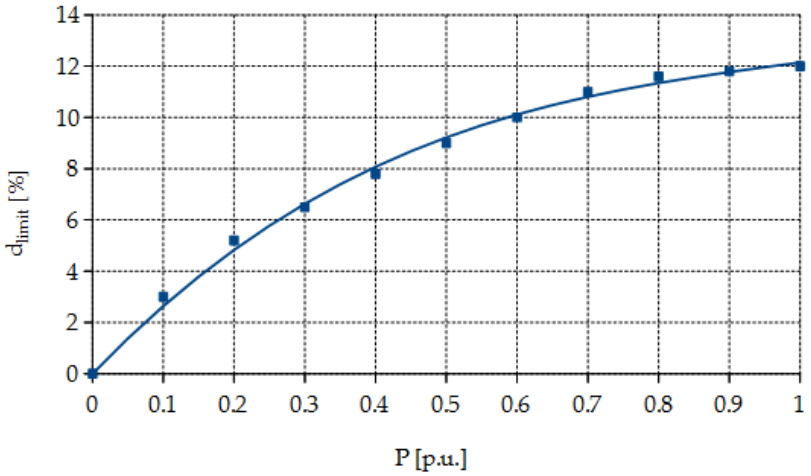

Fig. 61 Third-order polynomial function fitted to the measured data (limiting duty-cycle as a function of the inverter output power)

Therefore, the final resulting function implemented in the control algorithm for the current-collapse loss mitigation is given by the formula

$$d_{\text{limit}} = 28.79\,P - 24.74\,P^2 + 8.102\,P^3, \tag{13}$$

where P is the per-unit inverter output power calculated from (11) with the base value equal to the motor input power when the speed is set to 2000 RPM, and the machine is loaded by its nominal torque. The new value of d_{limit} is updated every 100 ms since the calculated power needs to be averaged. Furthermore, it was found out that a lower update period could affect the stability of the current control loops.

A direct comparison of the measured input DC-link current for operating points corresponding to minima in Fig. 60 for 1500 RPM and 2000 RPM is presented in Tab. 7

The data compares the DC-link current consumption for the case of non-limited and limited duty-cycle. The drive losses are decreased on average by 2 % at 2000 RPM, which can be seen as a "nominal speed" for the utilized DC-link voltage value. At 1500 RPM, the loss decrease is not so significant because the converter operates with low q-axis voltage, not sufficient for pulse width limiting.

Tab. 7 DC-link current measurement for various operating points

Speed	Load	DC-link current [A]		Loss decreased
RPM	Ω	$d_{\text{limit}} = 0$	LUT	%
1500	200	0.4020	0.3990	0.75
	100	0.5051	0.5030	0.42
	50	0.7162	0.7120	0.59
	33	0.9225	0.9170	0.60
2000	200	0.5730	0.5570	2.87
	100	0.7470	0.7280	2.61
	50	1.095	1.072	2.15
	33	1.446	1.418	1.97
	25	1.771	1.738	1.90

To visualize the proposed method's merits directly, infrared camera pictures of the inverter were taken. The reference machine speed was set to 2000 RPM, and the load resistance for the PMSM generator was selected as 25 Ω. As a prerequisite for the measurement, the drive was running some time with the LUT turned on until the temperature stabilized. Then, the LUT was turned off, and once the temperature stabilized again, Fig. 62 was taken. After that, LUT was turned on again, and after reaching a thermal steady-state, Fig. 63 was taken. It can be seen that the steady-state temperature of the hottest point on the inverter dropped by 6 °C when the proposed method of the current collapse loss minimization was applied. Fig. 64 then shows the converter board in detail. The GaN transistors are cooled using vias through the board with the heatsink mounted on the bottom side.

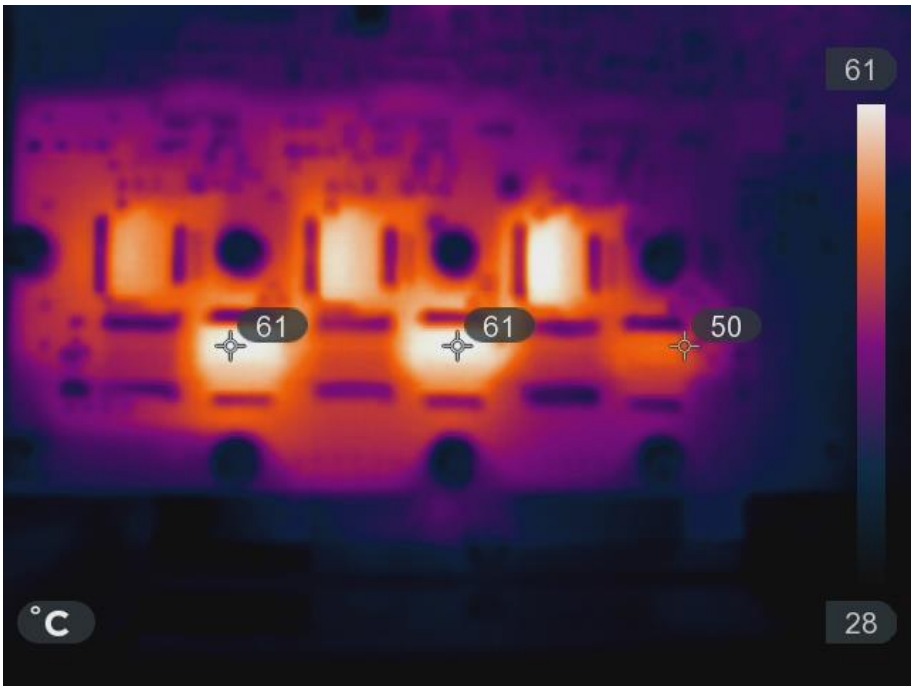

Fig. 62 Infrared camera measurement at 2000 RPM and R_{load} = 25 Ω without pulse width limitation

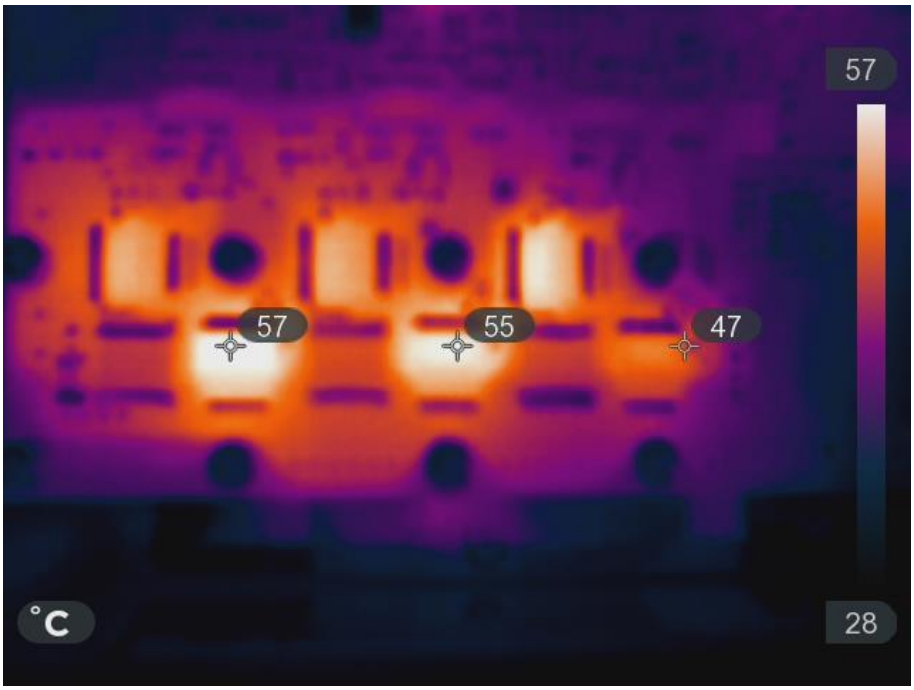

Fig. 63 Infrared camera measurement at 2000 RPM and R_{load} = 25 Ω with LUT-based pulse width limitation

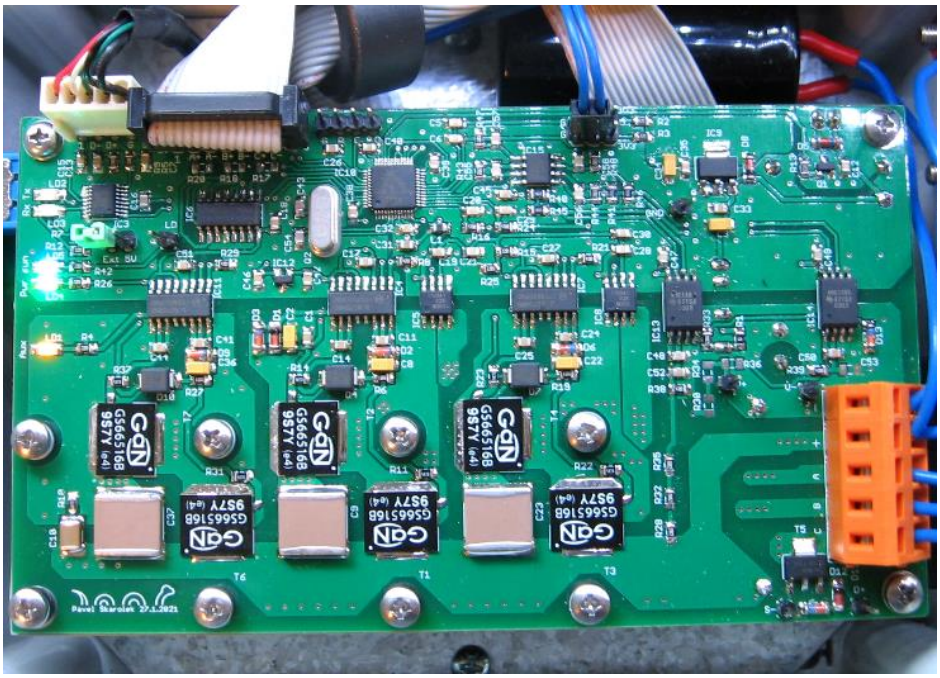

Fig. 64 Detail of the inverter board

4.3 Discussion

The GaN-based converter losses caused by the current collapse phenomenon and their mitigation, respectively, were investigated. It was explained that the additional losses are caused by increased dynamic on-state resistance depending on the pulse width of the utilized modulation strategy. Following this, the SVPWM of a three-phase VSI-fed PMSM in the basic FOC loop was adjusted by limiting the minimum pulse width for the GaN gate drivers. It was found out that the modulated voltage distorted by the limited pulse width decreases the current-collapse losses. At the same time, it causes additional machine losses introduced by the current distortion. Since both the converter and motor losses depend on the duty cycle limit value, optimal minimum pulse width corresponding to minimum consumed power for a given steady-state operating point can be determined. Also, it was experimentally observed that the optimum duty cycle limit value depends on the converter input power. Therefore, a LUT was implemented within the motor control algorithm to set the duty cycle limit value with respect to the actual motor input power calculated from the motor currents and voltages.

The amount of saved power was indirectly assessed by measuring the DC-link current on the input to the VSI-fed PMSM at a given speed and variable load. The consumed DC-link current of a SVPWM without duty cycle being limited was compared to the measured input current values corresponding to various duty cycle limit values. It was found that the loss reduction depends on the motor operating point. At low speed, the loss reduction is small due to the low q-axis voltage. So the pulse width limiting technique is here inefficient. At high speeds, when the motor operates in the field-weakening region, no local minimum corresponding to optimal duty cycle limit value exists. Therefore, in the field-weakening region, the method is not effective.

A significant loss reduction was observed for a given DC-link voltage where the converter operates at a higher q-axis voltage. Here the reference voltage vector within the SVPWM approaches the voltage hexagon boundaries. Since this operating point is typical for PMSM deployed in non-traction applications, such as pumps or servo drives, it can be expected that the proposed method could significantly decrease the power consumption for some specific types of drives used in industry or household applications. Furthermore, another advantage of the presented method is the purely software-based implementation.

5 GaN Transistor Switch-Off Loss Reduction

This chapter was partly published in journal Electronics, see [74].

With the absence of a freewheeling diode in the GaN transistor, the reverse conduction region is used to conduct the current [75]. However, a significant voltage drop in the reverse conduction mode exists, consisting of a gate threshold and turn-off voltage, which means the load current should be immediately transferred to the complementary switch in the half-bridge to avoid additional losses. In other words, the delay between when one transistor is turned off and the other is turned on, which is called the dead-time, needs to be set precisely [76]. However, the optimum dead-time for GaN transistors changes with the converter output power and input DC-link voltage [77]. An in-depth investigation in [78] shows the need to modify both the rising and falling edges of the microcontroller (MCU) control signal with the variable dead-time.

There are multiple approaches to proper dead-time selection. One option is to manually create a look-up table for a specific converter so the controller can set the dead-time accordingly [79]. The half-bridge configuration can also be equipped with a special sampling circuit to measure the actual time delay between the upper and lower transistors' switching instants [80], [81]. The model-based methods presented in [82] and [83] calculate the optimum dead-time depending on the converter's operating point reconstructed from the measured values. Furthermore, maximum efficiency point tracking algorithms can be used within various types of converters for dead-time optimization in the case of a variable switching frequency [84]. GaN drivers with built-in dead-time minimization circuits are being developed too; however, their operation is limited to the type of converter they are specifically designed for, such as highly efficient miniature DC/DC converters [85].

In this part, an online method of dead-time loss minimization for a vector-controlled PMSM supplied by a three-phase VSI controlled by a space-vector modulation (SVM) is proposed. The method is intended to improve and extend the authors' work presented in [86], where a similar approach was discussed for a half-bridge DC/DC converter topology. The method's principle is based on an online analysis of the current controllers' output at multiple operating points. Its main advantage is that no prior converter data and additional hardware are needed. The method, along with the motor control algorithm, was programmed into an MCU and verified experimentally.

5.1 Theoretical Analysis

Since the three-phase two-level VSI consists of three half-bridges connected in parallel, the dead-time theoretical analysis was conducted on a single half-bridge. The typical GaN-based half-bridge configuration is shown in Fig. 65. The actual transistors' switching depends not only on the dead-time issued by the MCU but also on the propagation delay introduced by the driver, the delay caused by a digital isolator (when used for the high-side switch), and the delay given by the transistors' intrinsic properties. Compared to silicon devices, in the case of fast-switching GaN transistors, the driver's

delay is comparable to the transistor's delay [85]. Furthermore, the driver's delay varies with the temperature and supply voltage, and the transistors' delay, with the DC-link voltage and the load current. In the following text, the actual time duration when both transistors in the half-bridge are in the "off" state will be referred to as the "output dead-time". Similarly, the converter's output voltage actual transition will be referred to as the "output duty cycle".

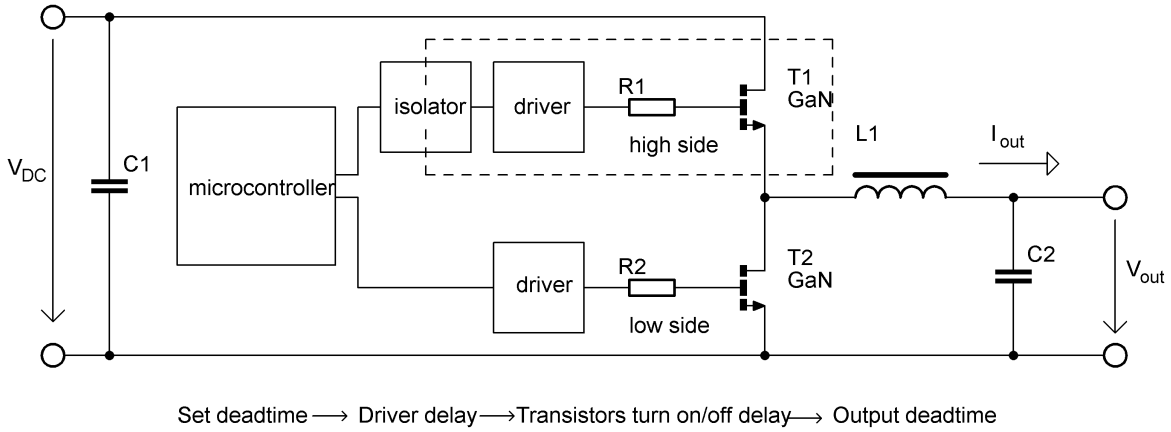

Fig. 65 A typical GaN-based half-bridge configuration

5.1.1 Dead-Time Generation

Ideally, the output dead-time should be equal to zero to minimize the additional losses [80]. When a fixed dead-time is used, it should be long enough with respect to the driver and transistor switching parameters to prevent a shoot-through (i.e., when both transistors are on simultaneously) [87]. The dead-time in the half-bridge configuration is adjusted by delaying the MCU's control signal's rising and falling edges. The set dead-time can be both positive and negative. The negative dead-time is needed in case the turn-on delays are longer than the turn-off delays. This is explained in Fig. 66, which shows the reference signal (Ref); the corresponding controllers' outputs for the high (H) and low (L) transistors, respectively; and the resulting output voltage (V) and current (I) waveforms. The figure shows a situation when the driver and transistor turn-on delay is longer than the turn-off delay. In practice, this situation is common when separate high-side drivers or digital isolators are used during the circuit design [78].

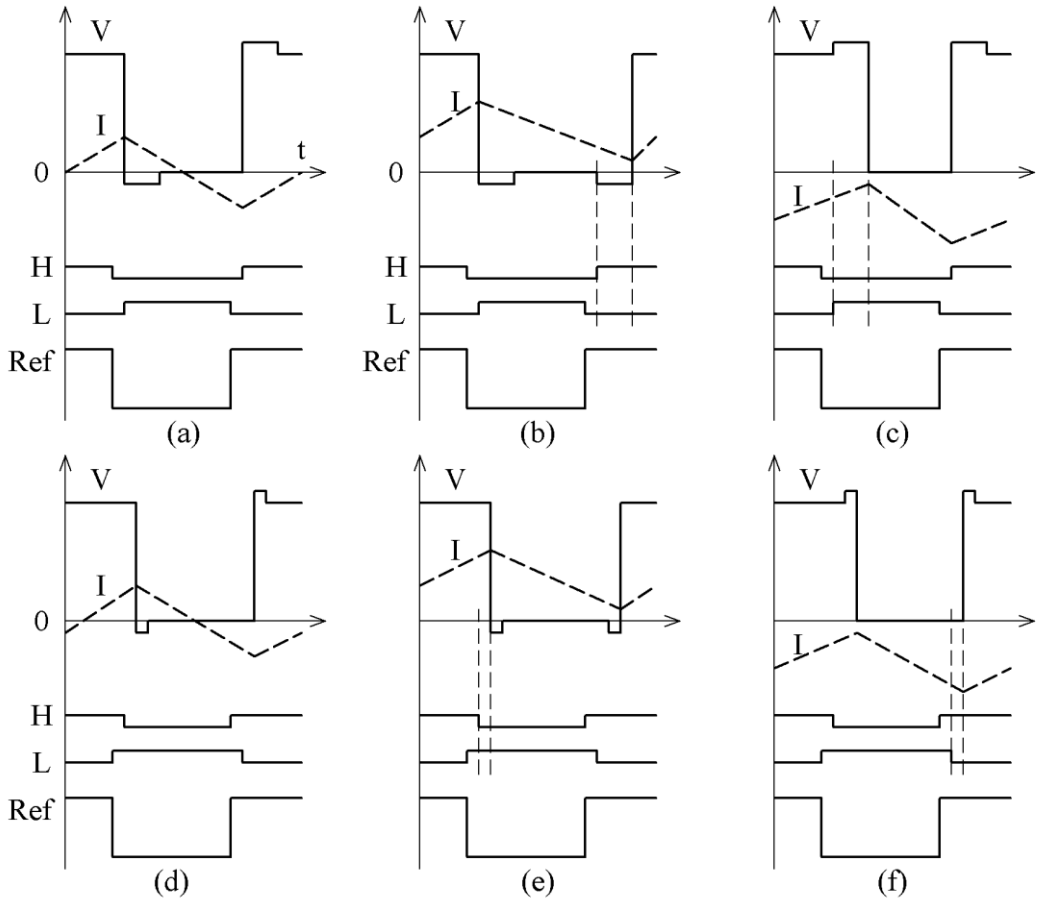

Fig. 66 Output duty cycle for (a) discontinuous conduction mode (DCM) positive dead-time, (b) continuous conduction mode (CCM) current source positive dead-time, (c) CCM current sink positive dead-time, (d) DCM negative dead-time, (e) CCM current source negative dead-time, and (f) CCM current sink negative dead-time

In the so-called discontinuous conduction mode (DCM), the output current polarity changes within a single switching period, causing a voltage commutation that always appears after the previously conducting transistor is turned off [88]. During the DCM, the output duty cycle is not influenced by the dead-time, as seen in Fig. 66a,d. The shorter output dead-time in Fig. 66d was achieved by utilizing the negative dead-time, which is created by delaying the control signals' falling edges for both the upper and lower transistors.

In the case of continuous conduction mode (CCM) and the current source operation (Fig. 66b), the output signal's rising edge was delayed by the dead-time plus the difference in the turn-on/off times of the driver's circuitry. The output duty cycle does not correspond to the reference duty-cycle, which means voltage distortion is introduced. When the half-bridge operates as a current sink (Fig. 66c), the falling edge is delayed instead, and the duty cycle is increased.

During CCM and current source operation (Fig. 66e), the negative dead-time changes the output duty cycle at the falling edge of the output signal, similar to the situation shown in Fig. 66c. For the current sink operation (Fig. 66f), the rising edge was adjusted.

Depending on the half-bridge output current in CCM, the output duty cycle D can be obtained from Tab. 8.

Tab. 8 Output duty cycle in CCM

Current Direction	Dead-Time Polarity	Output Duty Cycle
Source	Positive	$D = D_{\mathrm{MCU}} - \frac{t_{\mathrm{d(rise)}}}{T}$
Source	Negative	$D = D_{\mathrm{MCU}} - \frac{t_{\mathrm{d(fall)}}}{T}$
Sink	Positive	$D = D_{\mathrm{MCU}} + \frac{t_{\mathrm{d(fall)}}}{T}$
Sink	Negative	$D = D_{\mathrm{MCU}} + \frac{t_{\mathrm{d(rise)}}}{T}$

In Tab. 8, D_{MCU} is the reference duty cycle, $t_{\mathrm{d(rise)}}$ is the switching delay following the reference signal's rising edge, $t_{\mathrm{d(fall)}}$ is the switching delay following the reference signal's falling edge, and T is the switching period.

5.1.2 Reverse Conduction Loss

The cause of the reverse conduction losses is shown in Fig. 67. Here, the half-bridge output voltage (which operates as a current source) is distorted by negative peaks that correspond to the low transistor being in the self-commutated reverse conduction region [75]. The peaks disappear when the transistor is turned on and starts to operate with a smaller voltage drop (comparable to the forward conduction mode). The dead-time is at its optimum when the duration of the negative peaks is minimized.

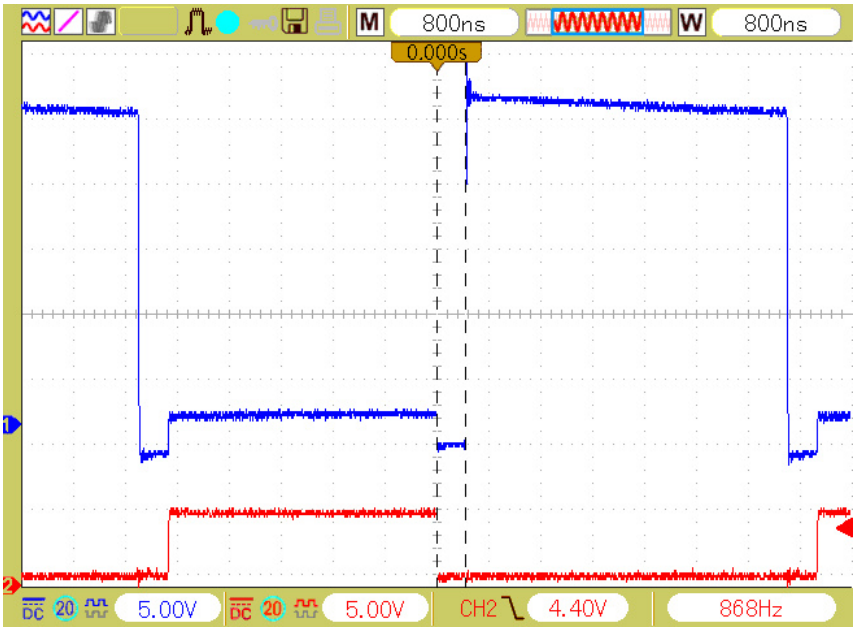

Fig. 67 Half-bridge output voltage (blue) and low-side transistor gate signal (red)

The output voltage V_{out} of the converter can be expressed as [86]

$$V_{\mathrm{out}} = D \cdot V_{\mathrm{DC}} - \Delta V_{\mathrm{SD}}, \tag{14}$$

$$\Delta V_{\mathrm{SD}} = \frac{2t_{\mathrm{dt}}}{T} V_{\mathrm{SD(off)}} \cdot \mathrm{sgn}(I_{\mathrm{out}}), \tag{15}$$

where D is the output duty cycle, V_{DC} is the DC-link voltage, ΔV_{SD} is the additional voltage drop caused by the non-zero output dead-time, t_{dt} is the output dead-time, $V_{\mathrm{SD(off)}}$ is the voltage drop across the source and drain, and I_{out} is the converter's output current.

The additional voltage drop ΔV_{SD} depends on the polarity of the output current and source-drain voltage $V_{\mathrm{SD(off)}}$, which appears across the transistor that operates in reverse conduction self-commutated mode. The source-drain voltage $V_{\mathrm{SD(off)}}$ consists of the gate threshold voltage $V_{\mathrm{GS(th)}}$ and negative gate voltage $V_{\mathrm{GS(off)}}$ that the driver applies during the off state [77], i.e.,

$$V_{\mathrm{SD(off)}} = V_{\mathrm{GS(th)}} - V_{\mathrm{GS(off)}}. \tag{16}$$

From (16), it can be seen that the dead-time losses are even more significant in the case of robust converters that apply a negative gate voltage in the off-state to prevent a false turn-on.

As explained in the previous section, the converter output voltage changes with the dead-time depending on the operation mode (Fig. 68). During the CCM, the maximum output voltage exists, which corresponds to no self-commutation. When the dead-time is decreased beyond some threshold value (the vertical dashed line in Fig. 68b), the current flowing through the recently turned-on transistor starts to rise before the current of the other transistor drops to zero. This shoot-through operation means the output is connected to the virtual DC-link neutral point for a short time. The current is then limited only by the parasitic inductance.

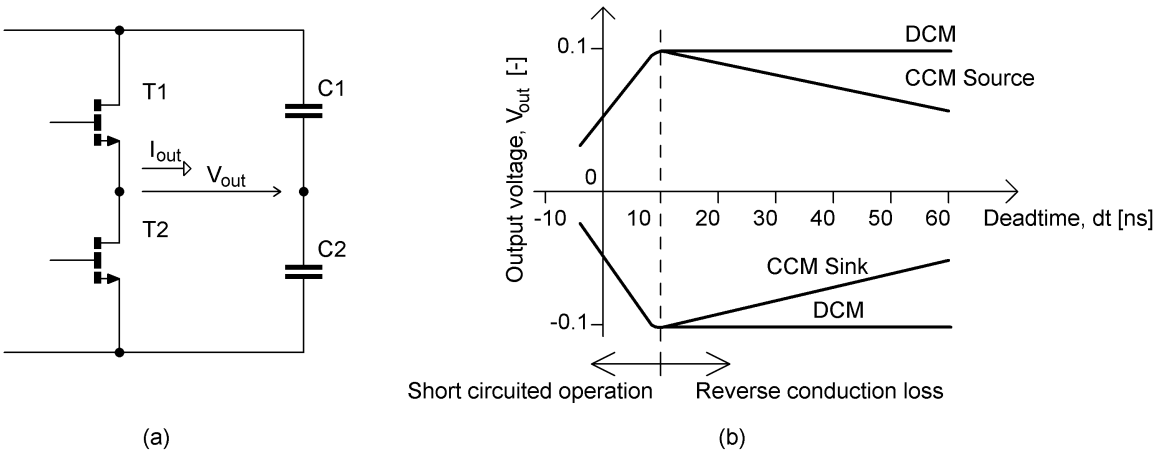

Fig. 68 Output voltage dependence on dead-time: (a) virtual DC-link neutral point, (b) dependence of output voltage on dead-time and modes of operation

5.1.3 **Drive Controller**

The block diagram of the proposed control scheme with a dead-time loss minimization algorithm is presented in Fig. 69. In contrast to the standard control schemes, the tracking algorithm block, and the corresponding dead-time compensation block, are added. Fig. 69 also shows a speed PS regulator with the possibility of field-weakening operation. Such a controller has been described, for instance, in [89]. The

reason behind the PS speed controller deployment is a more convenient measurement and presentation of the experimental results.

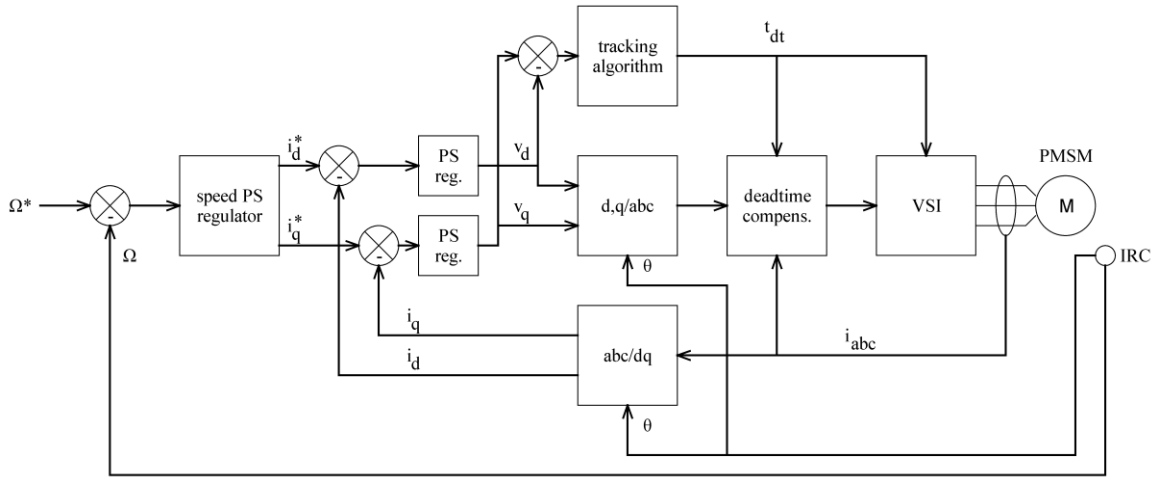

Fig. 69 Proposed control scheme

In a steady state, the ΔV_{SD} given by (15) produces output voltage distortion that can be expressed as [90]

$$\Delta v_\alpha = K\frac{2t_{\mathrm{dt}}}{T}V_{\mathrm{SD(off)}}\left[\mathrm{sgn}(i_a) - \frac{1}{2}\mathrm{sgn}(i_b) - \frac{1}{2}\mathrm{sgn}(i_c)\right], \tag{17}$$

$$\Delta v_\beta = K\frac{\sqrt{3}}{2}\frac{2t_{\mathrm{dt}}}{T}V_{\mathrm{SD(off)}}[\mathrm{sgn}(i_b) - \mathrm{sgn}(i_c)]. \tag{18}$$

where K is Clarke's transformation coefficient. The distorting voltage components expressed in the $\alpha\beta$ stationary reference frame can be transformed into the rotor-fixed dq reference frame as

$$\Delta v_d = \Delta v_\alpha \cos(\theta) + \Delta v_\beta \sin(\theta), \tag{19}$$

$$\Delta v_q = \Delta v_\beta \cos(\theta) - \Delta v_\alpha \sin(\theta). \tag{20}$$

where θ is the angle between the stationary and rotor-fixed coordinate systems. Fig. 70a shows the trajectory of the reference voltage vector (dashed) and the distorted voltage vector (solid) per electrical revolution in the stationary $\alpha\beta$ coordinate system (voltage in per unit). Fig. 70b then shows the vectors transformed into the dq reference frame. From Fig. 70, it can be seen that to compensate for the voltage distortion, the d-axis current controller has to increase the $-v_d^*$ demand, and the q-axis controller has to decrease the v_q^* demand.

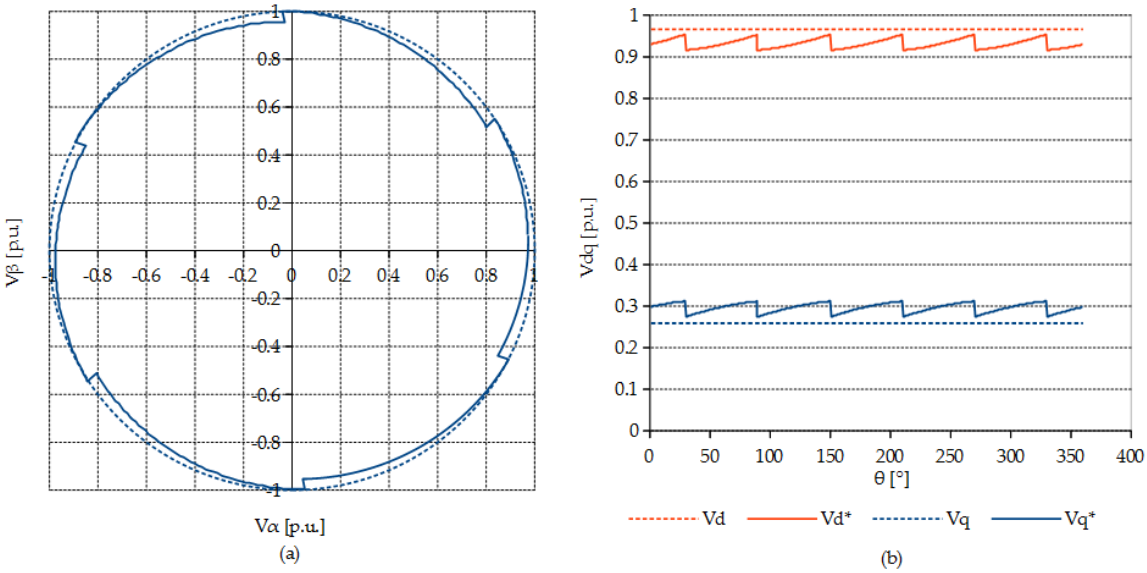

Fig. 70 The inverter reference (dashed) and distorted (solid) output voltage in (a) the stationary *αβ* reference frame and (b) in the rotor-fixed *dq* reference frame; t_{dt} = 5 % of T; ΔV_{SD} = 5 % of V_{DC}; power factor, 0.5; load angle, 15°

5.1.4 Tracking Algorithm

The tracking algorithm [84] is a simple perturb-and-observe tracker searching for the minimum output of the dq-axis current controllers by adjusting the dead-time for the VSI. Mathematically, the output of the tracker can be described as

$$t_{\mathrm{dt}}(k) = t_{\mathrm{dt}}(k-1) + \Delta t_{\mathrm{dt}}, \tag{21}$$

$$\left(v_{q(\mathrm{av})} - v_{d(\mathrm{av})}\right)_k > \left(v_{q(\mathrm{av})} - v_{d(\mathrm{av})}\right)_{k-1} \Rightarrow \Delta t_{dt} = -\Delta t_{dt}, \tag{22}$$

where Δt_{dt} is the dead-time increment, $v_{d(\mathrm{av})}$ and $v_{q(\mathrm{av})}$ are the dq voltage components averaged within the tracker update period, and the symbol k denotes the discrete step. The duty cycle for each phase is then compensated according to Tab. 8, i.e.,

$$D_x = D_{\mathrm{MCU}x} + \frac{t_{\mathrm{dt}}}{T} \cdot \mathrm{sgn}(i_x), x = a, b, c. \tag{23}$$

The optimum dead-time is continually tracked to ensure the reverse conduction losses are minimized, even during the drive parameter variation (i.e., power, DC-link voltage, and temperature variations).

5.2 Experimental Results

A GaN-based three-phase VSI prototype was built to implement the motor control algorithm along with the proposed dead-time loss minimization method. A picture of the experimental workspace is shown in Fig. 71.

The following experiment was designed to test the method. A PMSM drive was operated under various load and speed conditions, including the field-weakening region. At first, the tracking algorithm input variable had to be determined. Based on the theoretical analysis performed in Section 2, the resulting quantity selected as the tracker's observed value was the difference between the q- and d-axis voltage components, i.e.,

$v_q - v_d$. With the observed variable determined, the tracking algorithm had to be tuned; i.e., the dead-time increment and update period values were set. The tracking algorithm was then tested at multiple operating points. Furthermore, the power consumed by the converter for multiple fixed dead-time values was measured, and the results were compared to the proposed tracker-based optimization method.

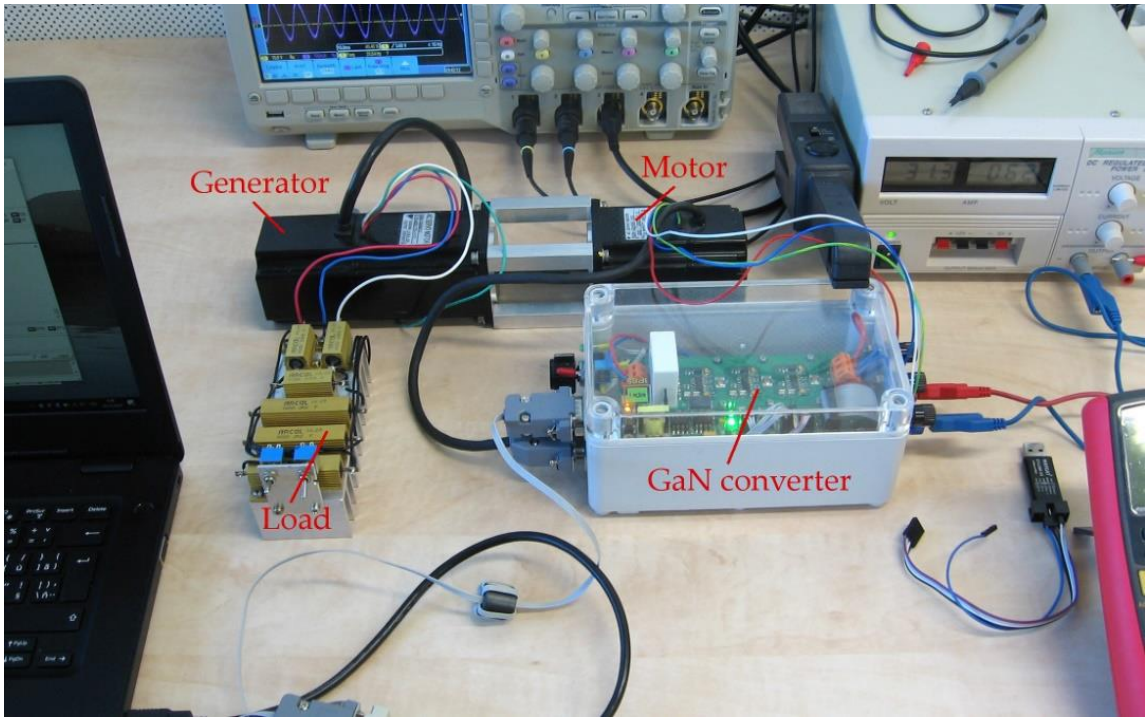

Fig. 71 Experimental workspace

5.2.1 Experimental Setup

The VSI was equipped with six GS66508T GaN transistors driven by Si8275 isolated half-bridge gate drivers. The converter was controlled by an ARM Cortex M4 MCU STM32F334 equipped with a high-resolution timer peripheral that allows setting the dead-time with a resolution of 1 ns. The SVM frequency was set to 100 kHz. The converter supplied a 200 W 4-pole PMSM with an incremental encoder used for speed and position feedback. A simplified schematic diagram of the experimental setup is shown in Fig. 72.

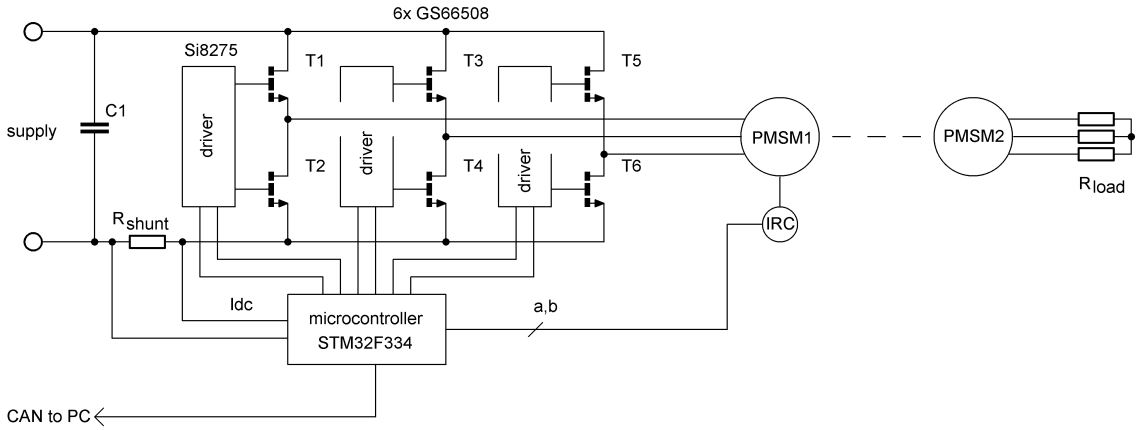

Fig. 72 Simplified schematic diagram of the experimental setup

A single shunt current measuring method with phase current reconstruction optimized for a high switching frequency [91] was used for the current measurement. The VSI output voltage is hardware-demanding to measure directly due to its pulsating nature and high-frequency components. Therefore, the reference voltage vector, i.e., the current controllers' output, was used within the algorithm instead. The controlled motor was then coupled with a similar PMSM machine loaded by resistors R_{load} to create a mechanical load. The nameplate data and model parameters of both machines are shown in Tab. 9. The data acquired by the MCU were transferred directly to the laptop via a CAN bus, which was also used to set the controllers' reference values.

Tab. 9 Motor and generator parameters

	Motor	**Generator**
Type	SGM-02A5F	SGM-04AW12
RPM	3000	3000
Power (W)	200	400
Max voltage (V)	200	200
Max current (A)	2.0	4.0
Stator resistance (Ω)	1.35	1.26
d-axis inductance (mH)	7.05	7.75
q-axis inductance (mH)	7.25	8.05

5.2.2 Current Controllers' Output Change with Dead-Time

First, the behaviour of the current controllers' output with respect to the set dead-time was examined. During the experiment, the motor was running in a steady state at a constant speed, with the dead-time being changed by 1 ns steps per 200 ms to let the current controllers stabilize. The reference speed was then modified and the data measured again. The dependence of the relative output values of the d- and q-axis current controllers on the set dead-time for different reference speed values and different load resistors R_{load} are plotted in Fig. 73.

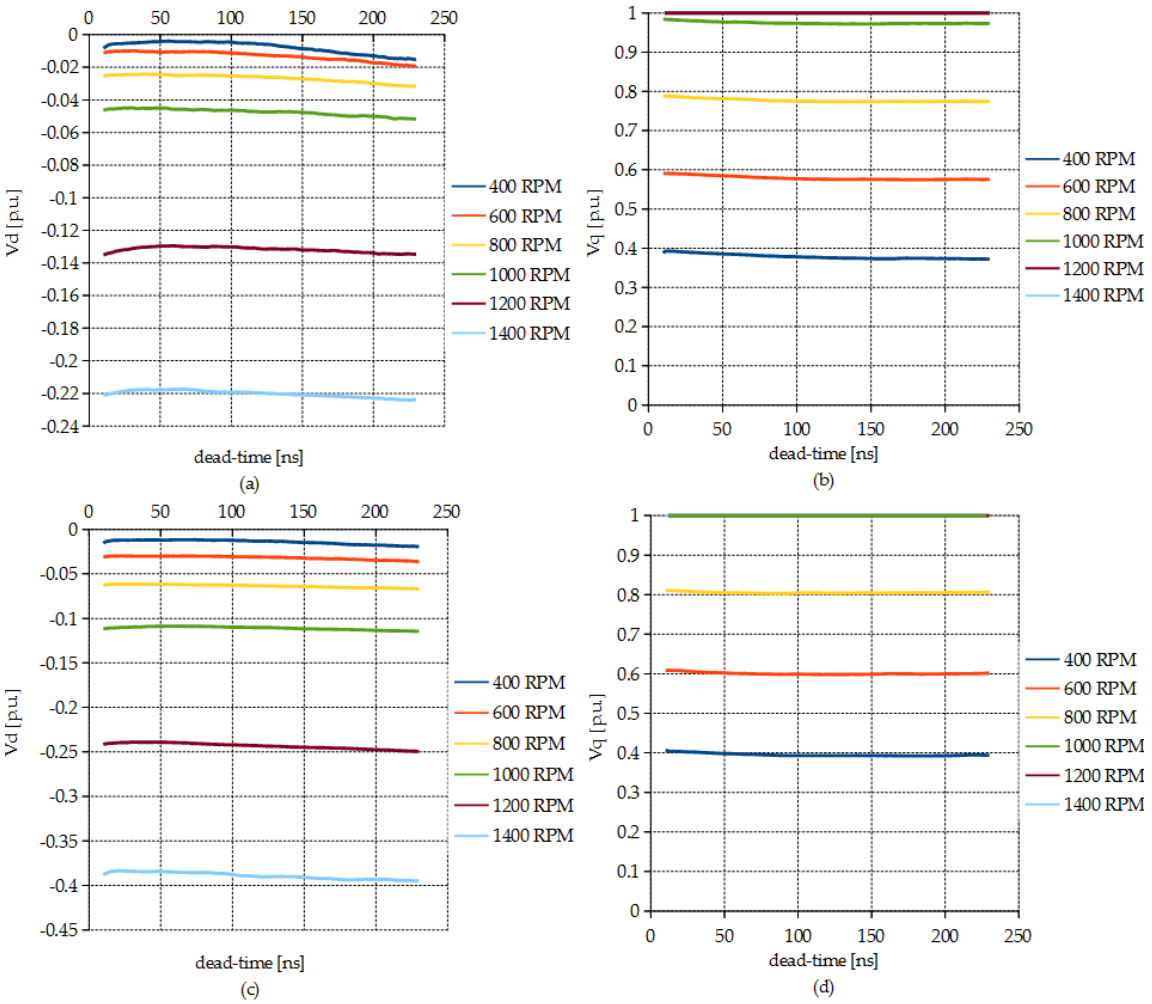

Fig. 73 Dependence of current controllers' outputs on the set dead-time for different speed references; mechanical load created by PMSM with a variable resistance R_{load} in the armature: (a) *d*-axis current controller, R_{load} = 187 Ω; (b) *q*-axis current controller, R_{load} = 187 Ω; (c) *d*-axis current controller, R_{load} = 73 Ω; and (d) *q*-axis current controller, R_{load} = 73 Ω

Fig. 73a shows that v_d decreased with increasing speed. Contrary to that, v_q (Fig. 73b) increased with the speed almost linearly until the field-weakening region was reached (above 1000 RPM). In Fig. 73c, the higher negative values of v_d with respect to the speed were caused by the increased load angle, while the small increase in v_q in Fig. 73d compensated the stator resistance. To make the shapes of all the curves more clearly visible, they are replotted in Fig. 74 with their aligned peaks.

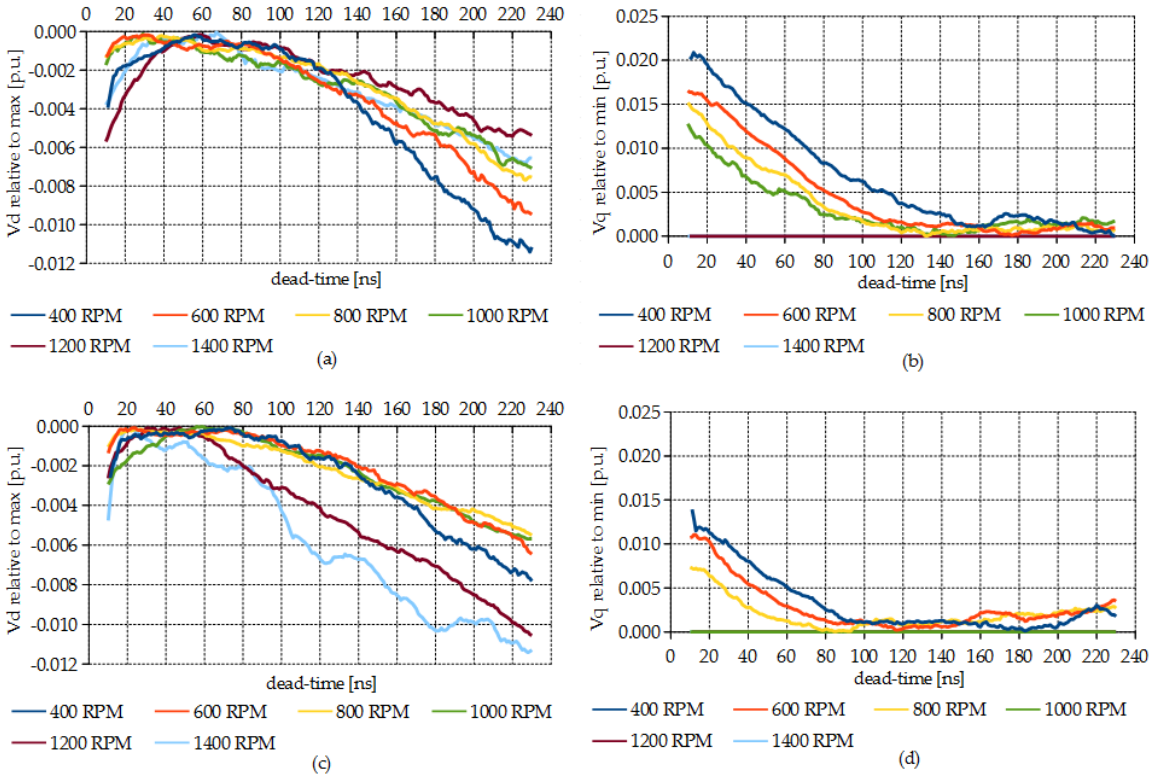

Fig. 74 More detailed depiction of curves from Fig. 73: (a) *d*-axis current controller, R_{load} = 187 Ω; (b) *q*-axis current controller, R_{load} = 187 Ω; (c) *d*-axis current controller, R_{load} = 73 Ω; and (d) *q*-axis current controller, R_{load} = 73 Ω

In Fig. 74, the v_d curves exhibit a visible maximum, while the v_q curves mostly keep decreasing across the whole tested range. This behaviour was caused by the distorting voltage vector decreasing v_d and increasing v_q components, as shown in Fig. 70. During this time, the reverse conduction losses were increased with the set dead-time. It follows that the optimum dead-time value can be found at the minimum of $v_q - v_d$. This quantity is also used as the observed value within the tracking algorithm.

5.2.3 Tracking Algorithm

Fig. 75 shows the trace of the tracker's dead-time from the starting point of 200 ns. The dead-time increment Δt_{dt} was set to 5 ns, and the tracker update period, to 200 ms. In Fig. 75a, the motor was running at 800 RPM where both the v_d and v_q voltage components were changing. In Fig. 75b, the motor was running in the field-weakening region where only the change in v_d was observed by the tracker. For an increased load and the same speed references, Fig. 75c,d show lower values found by the tracker.

Due to the speed-dependent load, a higher speed means a higher output VSI current. The same goes for an increased load. The VSI current and the current-dependent change in the GaN's switching behaviour caused additional losses and output dead-time variation. Therefore, the optimum dead-time found was lower for both increased loads and speeds.

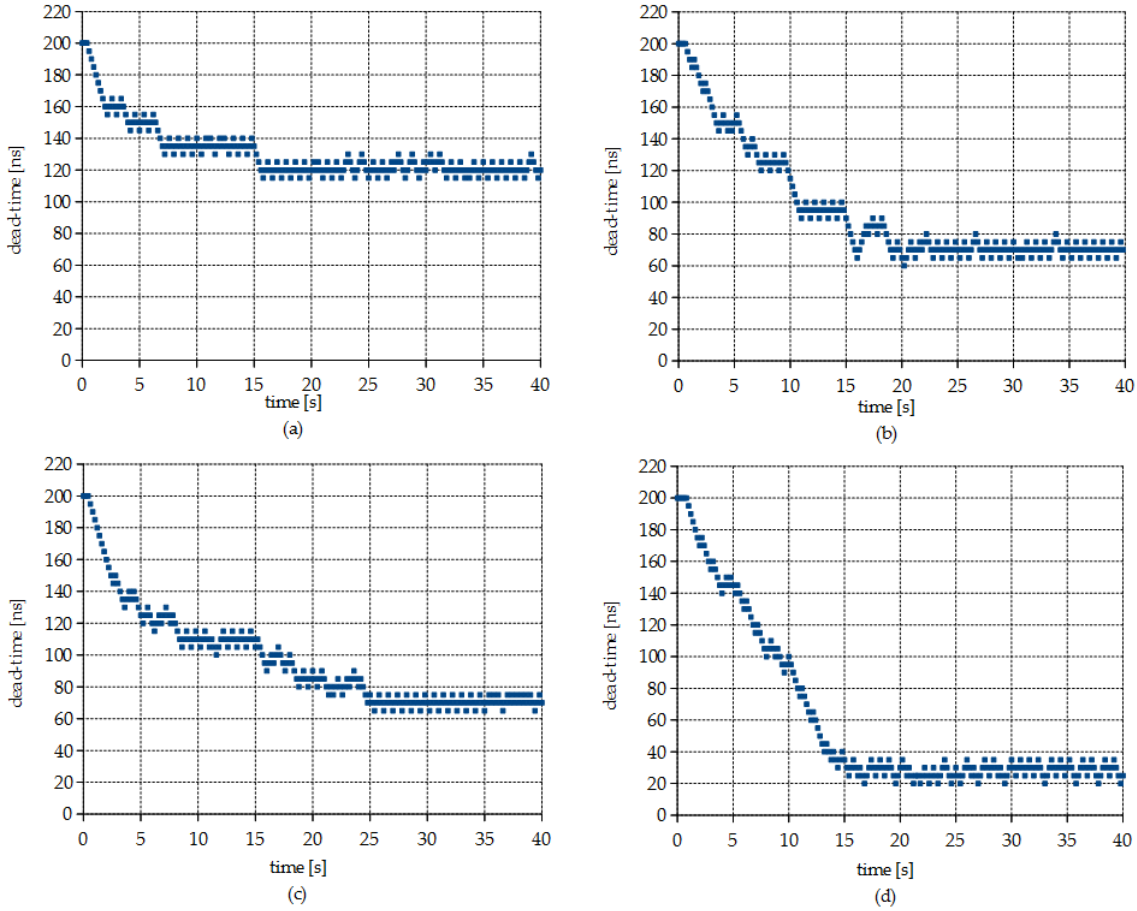

Fig. 75 Tracking algorithm searching for an optimum dead-time for (a) 800 RPM, R_{load} = 187 Ω; (b) 1200 RPM, R_{load} = 187 Ω; (c) 800 RPM, R_{load} = 73 Ω; and (d) 1200 RPM, R_{load} = 73 Ω

5.2.4 Dead-Time Loss Minimization

To quantify the amount of energy savings achieved with the proposed method, the input inverter power was measured for multiple cases. Within the first group of tests, the converter was operated with selected values of fixed dead-time. Within the second group of tests, the converter was operated with a dead-time found by the tracking algorithm. Tab. 10 shows the measured DC-link currents for the fixed and tracked optimum dead-times with the calculated relative loss differences.

Tab. 10 Relative comparison of VSI losses for selected values of fixed dead-time compared to optimized dead-time for various speed references and R_{load} = 73 Ω

RPM	Input DC-Link Current for Various Dead-Time Values (A)					Relative Power Saved with the Tracking Algorithm (%)			
	200 ns	100 ns	50 ns	10 ns	Tracker on	200 ns	100 ns	50 ns	10 ns
400	0.1416	0.1409	0.1419	0.1478	0.1409	−0.50	−0.01	−0.71	−4.90
600	0.2376	0.2364	0.2373	0.2440	0.2362	−0.59	−0.08	−0.47	−3.30
800	0.3658	0.3641	0.3643	0.3750	0.3636	−0.61	−0.14	−0.19	−3.14
1000	0.5338	0.5310	0.5301	0.5400	0.5293	−0.85	−0.32	−0.15	−2.02
1200	0.7641	0.7600	0.7574	0.7700	0.7573	−0.90	−0.36	−0.01	−1.68
1250	0.8703	0.8656	0.8642	0.8755	0.8621	−0.95	−0.41	−0.24	−1.55
1300	0.9832	0.9748	0.9709	0.9830	0.9682	−1.55	−0.68	−0.28	−1.53
1350	1.0750	1.067	1.0620	1.0780	1.0580	−1.61	−0.85	−0.38	−1.89
1400	1.1385	1.1309	1.1258	1.136	1.118	−1.83	−1.15	−0.70	−1.61

In Tab. 10, it can be seen that for 400 RPM, the optimum dead-time lies close to 100 ns because here, the relative loss difference between the fixed and tracked dead-time is minimal. A similar situation exists for 1200 RPM and 50 ns. Contrary to that, the fixed 10 ns and 200 ns values were clearly too small and large, respectively, for the whole measured range.

In the field-weakening region (above 1000 RPM), the power loss decrease is more significant because the field-weakening d-axis current component causes additional losses when the dead-time is fixed. This is important mainly when the GaN converter is used as a direct replacement for a silicon-based converter. At high switching frequencies, the GaN reverse conduction mode causes higher power losses compared to low-frequency silicon-based converters. Therefore, it follows that the dead-time optimization is also important from the point of view of the GaN-based converters becoming a convenient high-power density and high-efficiency alternative to silicon-based converters.

5.2.5 Comparison with Other Methods Mentioned in the Literature

To assess the overall quality of the proposed method within the context of other methods presented in the literature, a qualitative comparison was made. The features of the individual approaches in selected categories are highlighted in Tab. 11. The method presented here stands out against other approaches mainly because it eliminates their disadvantages while achieving effective loss minimization at the same time.

Tab. 11 Dead-time optimization method comparison

	Additional Measurements	Simulation Requirements	HW	SW	Loss Minimization
Fixed Dead-time [87]	single measurement	-	-	-	low
Look-Up Table [52]	dead-time map required	-	memory space	searching in the dead-time map	medium
Model-Based [82]	-	converter model preparation	-	converter model online calculation	high
Dead-Time Sensor [80]	-	-	reverse drop sampling circuit	reverse drop data acquisition	high
The Proposed Method	-	-	-	tracking algorithm	high

5.3 Discussion

A novel method of a GaN-based PMSM drive dead-time loss minimization strategy is presented. The proposed control scheme consists of a classic vector control structure with added tracking algorithm to find the optimum dead-time value. The main idea is based on the theoretical and mathematical analysis of the GaN's reverse conduction phenomena and their influence on the inverter output voltage. It follows from there that

reverse conduction losses occur together with the output voltage distortion. Therefore, the tracking algorithm (a simple perturb-and-observe) utilizes the current controllers' output signals for the optimum dead-time selection. The contribution of the presented method is that neither additional hardware nor prior inverter data are necessary for its function. The method is a viable option for either offline or online optimum dead-time identification.

The experimental results confirm the validity of the presented approach at drive's multiple operating points. It has been found out that a load increase leads to a lower optimum dead-time value being found by the tracking algorithm. This is caused by the current-dependent switching behaviour of GaN devices. Furthermore, converter power losses were measured at several operating points for multiple fixed dead-time values and compared to the losses measured in the case of a dead-time tracking algorithm turned-on. The results confirm the advantages of the current-dependent optimum dead-time value generation over a fixed dead-time value. In the field-weakening region, the saved power was more significant due to the PMSM characteristics.

6 GaN Bridgeless Converter Variable Dead-Time

This chapter was partly published in Proceedings of the 2023 PIERS International Conference, see [92].

Power factor correction (PFC) bridgeless converters in Fig. 76 with GaN transistors are achieving better efficiency and power density compared to other solutions in the field of PFC converters [8]. Utilizing GaN transistors brings new challenges in the field of control algorithms. Mainly the high frequency operation demanding high resolution PWM generator timers and precise dead-time setting together with fast control loop calculations and feedback values measurements. This chapter presents a software-based solution to on-line dead-time adjustment which improves the efficiency of GaN-based PFC converters.

6.1 On-Line Variable Dead-Time

In case of the PFC converter, the current is changing between zero and peak values each half-period of the grid input voltage. To track the optimum dead-time, we should update the dead-time value at each PWM pulse calculation within the half-period. A strategy that adds this function to the control algorithm of GaN-based bridgeless PFC converter [93] was developed. The theory is experimentally verified on a converter test setup by comparing efficiency curves for constant and time-variable dead-time values. The main contribution of the work is increasing the efficiency achieved only by control algorithm improvement and without additional hardware.

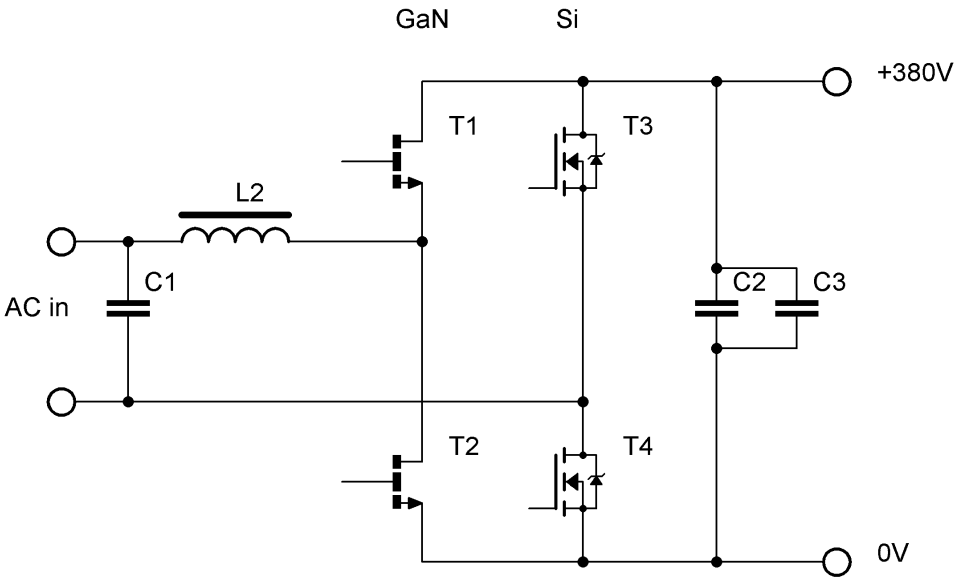

Fig. 76 GaN-based bridgeless PFC converter

The control circuit of the PFC converter in Fig. 77 consists of orthogonal phase locked loop (PLL) synchronization needed to find the zero crossings of the input voltage to properly switch the PWM polarity to the fast GaN totem pole and the Si slow leg.

The sinusoidal reference is also used to create the input current reference for the current PI controller.

The duty feed forward (DFF) helps the current controller to adjust only the difference between real and expected duty cycle according to the input to output voltage ratio. It helps to remove the phase shift created by the PI controller delay as well as the input capacitor current [94].

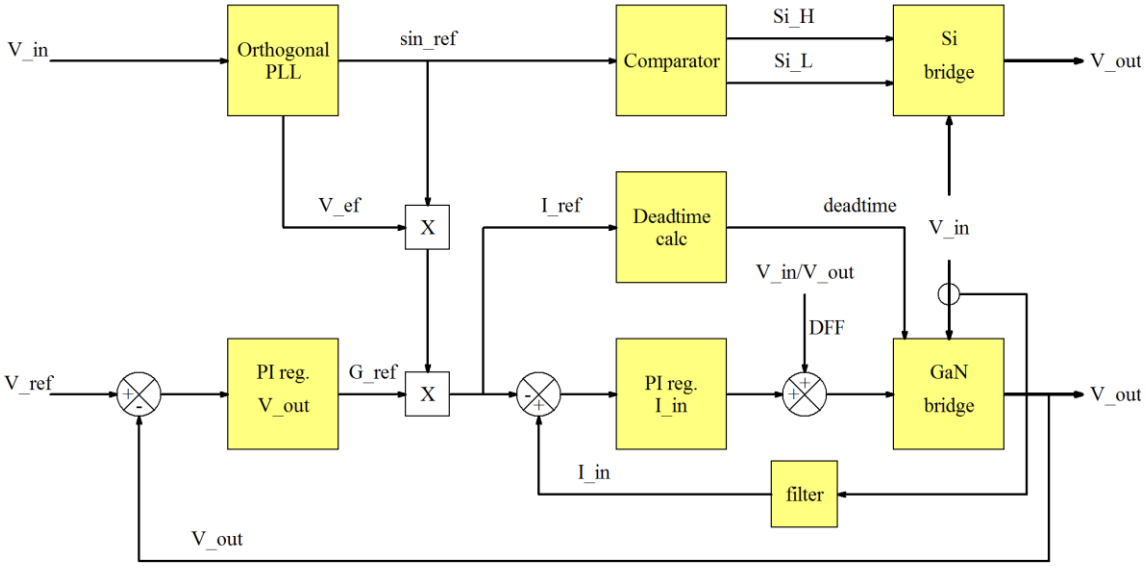

Fig. 77 PFC control circuit

For the proposed improvement it is necessary to add the dead-time calculation block into the control circuit. Based on the reference current the new dead-time value is set in each calculation period together with the duty cycle.

By increasing the dead-time at low current we can optimize the efficiency of the PFC converter, especially at light load. The dead-time value is updated according to the polynomial curve given in Fig. 78.

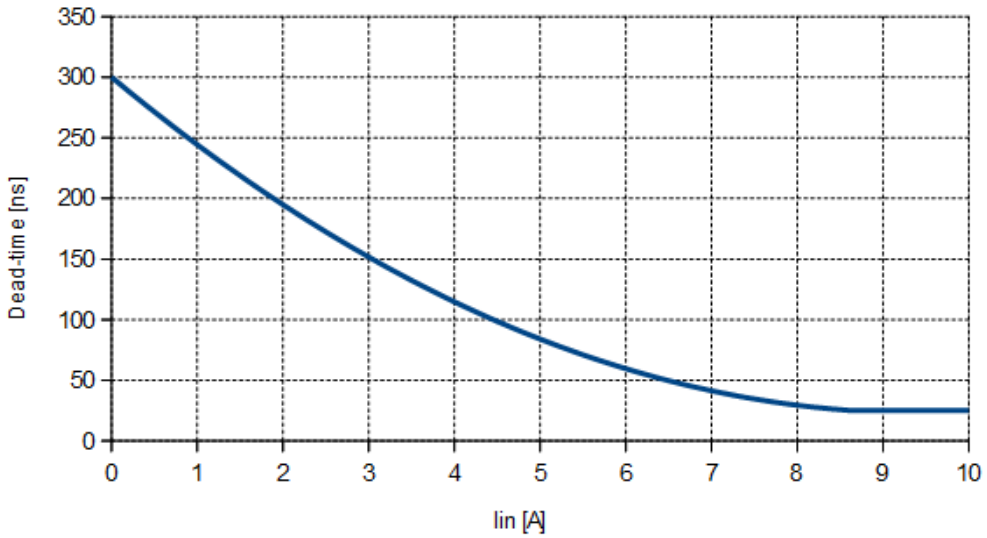

Fig. 78 Set dead-time dependence on half-bridge input current

The reverse voltage during dead-time that causes the losses, can be calculated according to (24).

$$V_{\mathrm{SD(off)}} = V_{\mathrm{GS(th)}} - V_{\mathrm{GS(off)}}. \tag{24}$$

where $V_{GS(th)}$ is the gate threshold voltage given by datasheet of the transistor and $V_{GS(off)}$) is the voltage we use for turning off the transistor. It means, with negative gate voltage the voltage drop in reverse is higher.

The curve of dead-time t_{dt} [ns] dependency on input current i_{in} [A] is experimentally fitted according to (25)

$$t_{dt} = 300 - 58.82 \cdot |i_{in}| + 3.125 \cdot {i_{in}}^2 \tag{25}$$

This requires an extensive measurement on a prototype. The curve can be replaced by look-up table filled automatically by an optimum dead-time tracking algorithm presented in previous chapter.

6.2 Experiment

The experimental setup of the bridgeless converter in Fig. 79 was built with GS66516 GaN transistors (650 V, 25 mΩ) in totem pole and with IPW60R017 Si super-junction transistors (600 V, 17 mΩ) in slow leg. Each half bridge is driven by Si8275 fast isolated driver. The proposed software of the control circuit is written for ARM Cortex M4 microcontroller STM32F334 and again utilizes the high resolution timer.

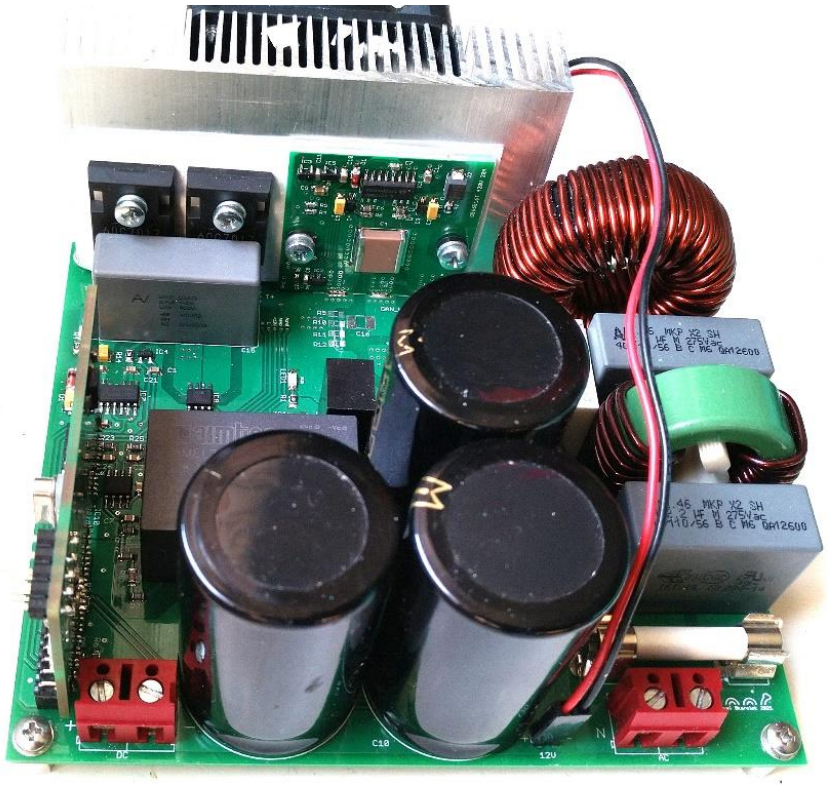

Fig. 79 Experimental setup

The efficiency was measured by means of two power meters GPM-8310 at first with constant value of dead-time (20 ns) and then with the proposed on-line calculated value. Results are presented in Fig. 80. During the measurement the PFC converter was loaded by 50 Ω, while the power was controlled by variable AC source.

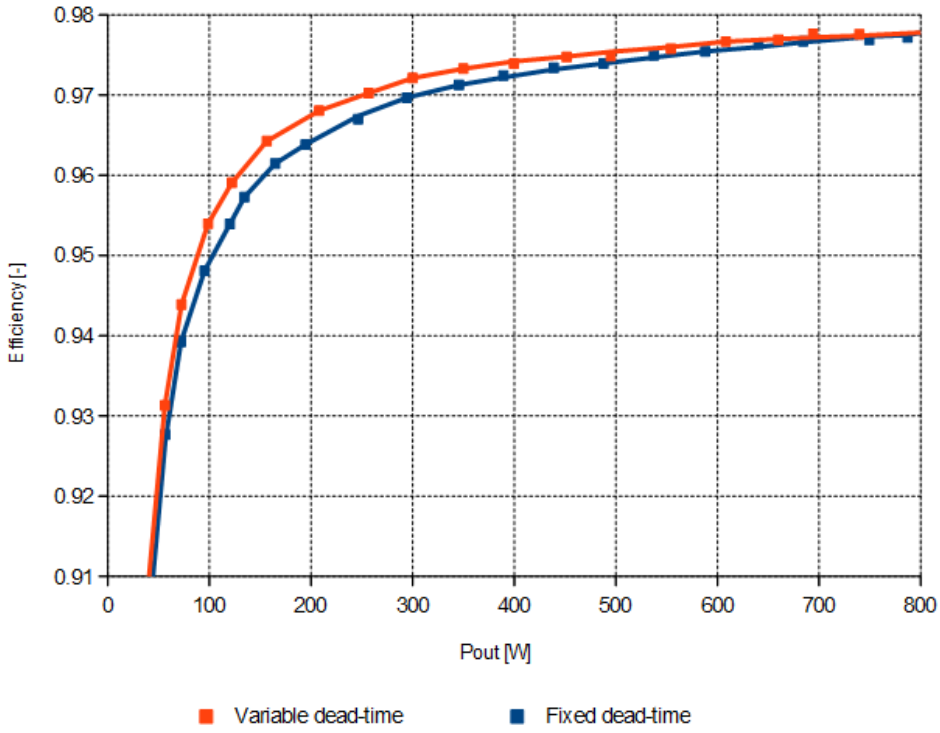

Fig. 80 Efficiency curve with variable and fixed dead-time

6.3 Discussion

The proposed variable dead-time strategy increases efficiency at light load of the PFC converter. The algorithm sets the dead-time each calculation period of the control loop. The resulting optimum dead-time changes with the actual current the GaN half-bridge is operating with. Due to nature of the PFC converter behaviour the half-bridge is expected to operate at optimum efficiency from zero to peak of the AC input current waveform. The main benefit of this solution is no need of hardware changes, the software solution is completely enough. However, the measurement on the prototype converter is necessary to construct the optimum dead-time curve that depends on current. The possible improvement is to add the tracking algorithm that will automatically fill in a look-up table during the converter operation.

7 Conclusions

The main topic of this work are GaN transistors in power converters of the future EV tractive system with high efficiency and power density. Selected objectives are important for achieving expected power, reliability and minimizing losses of GaN-based converters.

As one of the achieved results of this work, the high speed driver with over-current protection for GaN transistors in half-bridge was developed and tested. The designed driver reached three times faster over-current protection compared to recent drivers.

Multiple cooling options were analysed and compared to each other at the same dissipated power. From the compared cases, the lowest steady state transistor's temperature was achieved using the IMS board. In order to minimize the parasitic inductances in gate current path, a special board including driver circuit placed as close as possible to the transistor was designed.

As a significant research contribution to the GaN-based power converters' development can be considered the proposed methods minimizing the losses caused by the current-collapse and dead-time. Possible software solution minimizing the conduction losses induced by current-collapse is described. Very important reducing the dead-time losses in reverse conduction region is developed specially for GaN-based converter feeding 3-phase motor. Similar method of reducing the dead-time losses was tested on GaN-based PFC converter designated for electric vehicle on-board charger.

7.1 Fulfilment of the Thesis Objectives

1. Improving drivers' performance to maximize utilizing the devices' capability.

To ensure safe operation of the GaN transistor operating at high switching frequencies, the new fast drivers are needed. Therefore, the new driver circuit was proposed and tested to provide fast over-current protection for new GaN transistors operated in power converters. The measured over-current protection response is three times shorter compared to recent drivers. The designed driver enables the transistor safe operation at full load.

2. Analysing the new perspective devices' cooling possibilities.

Three DC/DC converters were built using different cooling methods of GaN power devices. From the tested and compared means of cooling, the proposed method using the IMS board provides the lowest steady state temperature. It was necessary to design the IMS board including a gate driver stage that minimizes the parasitic inductances caused by placing the transistors of half-bridge on the separate IMS board. This solution was successfully tested and the gate driving requirements were achieved.

3. Minimizing the new devices' losses in their switch-on state by the software control algorithm extension only.

The control algorithm of PMSM drive was extended by a variable minimum pulse width limit of the SVPWM switching pattern to find the optimum operation point with respect to current-collapse losses and losses in the motor. Operating the drive in optimum points trajectory decreases the drive losses. Providing the same output power on the shaft, the decrease of total drive power consumption up to 3 % was proven.

4. Minimizing the new devices' losses in their switch-off state by the software control algorithm extension only.

The optimal dead-time tracking algorithm was added to the PMSM drive control software together with the dead-time compensation block. The added tracking algorithm is able to find successfully an optimal dead-time value at which the converter reverse conduction losses are minimized. It is reached without adding any other sensors. The software extension was successfully tested and the drive total power consumption decrease up to 5 % was proven.

5. Reducing the converters' output voltage drop by the on-line dead-time control.

Because the half-bridge transistor's switching-off time depends on the actual current value, the optimum dead-time must depend on the current value, too. The half-bridge losses were further minimized, especially at light load condition, by implementation the on-line dead-time calculation algorithm based on the measured current value. This was verified on a GaN-based PFC converter that is a necessary part of electric vehicle on-board charger.

7.2 Future Work

Nowadays GaN transistors are found more and more low power applications such as chargers where the high power density is very practical.

Future work will depend on the GaN devices development. Transistors with higher breakdown voltages will bring new challenges for drivers and losses minimization. In case the breakdown voltage will remain unchanged, new power converters' topologies with GaN transistors should be developed to utilize GaN transistors' benefits in motor drives or other applications.

The field of GaN transistors' application in power converters will certainly bring many significant opportunities for the future scientific research.

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Author’s Publications Related to the Thesis

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