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Faculty of Electrical Engineering
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Highly Efficient RF Power Amplifiers for Medical and Industrial Applications

Doctoral Thesis

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The work contained in this thesis has not been previously submitted to meet requirements for an award at this or any other higher education institution. To the best of my knowledge and belief, the thesis contains no material previously published or written by another person except where due reference is made.

in Prague, ...

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Jesús Anzoátegui Cumana Morales

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Abstract

Cutting down energy consumption in electronic systems is required to increase operating time in battery-powered products, to reduce size and weight by alleviating cooling requirements and is essential to reduce carbon dioxide emissions. Since power amplifiers are among the power hungriest components in an RF transmitting system, improving their efficiency is essential to reduce overall power consumption.

This thesis studies the class-E power amplifier, a high-efficiency amplifying concept, in which the active device behaves like a switching element. Applications like RF heating in which linearity is not a demanding requirement, can resort to this kind of concept. It has been shown that excessive transistor output capacitance degrades performance in this amplifier class, reducing efficiency and limiting its highest frequency of operation. In this thesis, a new circuit topology is proposed to accommodate devices with excessive output capacitance, thereby improving efficiency and extending maximum frequency of operation. The proposed topology, composed of an inductor in series with sub-harmonic resonators, replaces the DC feed inductor in the classical finite-feed class-E amplifier circuit. In this way, output capacitance compensation is achieved. The corresponding theory and design equations are developed in this work. To validate the proposed concepts, a circuit demonstrator has been designed, built and measured.

This compensating approach, which is called Frequency-Dependent Inductive Compensation (FDIC) in this thesis, is further evaluated to understand its validity at microwaves. After extracting a simplified large-signal model of a GaN HEMT, extensive simulations are used to evaluate the impact of excessive transistor output capacitance on class-E. This approach removes the main idealization when analyzing this amplifier class, i.e., the switch is replaced by a voltage-controlled current source. Using the extracted model instead of the ideal switch, allows us to evaluate the effects of non-ideal switching, intrinsic capacitance voltage-dependency, feedback capacitance and saturation resistance. The effect of the FDIC on the transistor drain voltage and current waveforms in the class-E topology is studied and the limitations of this approach are discussed. Once more, a circuit demonstrator is designed and built to validate the study.

The final part of the thesis addresses power amplifiers for hyperthermia systems. A 250 W amplifier prototype operating at 70 MHz for regional hyperthemia is designed and built. In this case, two design approaches are studied, namely, using the conventional class-E design method based on existing equations, and secondly, by performing load-pull simulations using the available large-signal model of the LDMOS device. The intrinsic drain current and voltage waveforms are used to guide the design process and to optimize efficiency. Finally, RF heating experiments using an agar phantom are performed to evaluate the amplifier when delivering power under close-to-real conditions.

Abstrakt

Snížení spotřeby energie v elektronických systémech je nutné ke zvýšení provozní doby u produktů napájených bateriemi, ke snížení velikosti a hmotnosti snížením požadavků na chlazení a je nezbytné pro snížení emisí oxidu uhličitého. Vzhledem k tomu, že výkonové zesilovače patří mezi energeticky nejnáročnější komponenty ve vysokofrekvenčním vysílacím systému, zlepšení jejich účinnosti je zásadní pro snížení celkové spotřeby energie.

Tato práce studuje výkonový zesilovač třídy E, koncept vysoce účinného zesilovače, ve kterém se aktivní zařízení chová jako spínací prvek. Tento druh konceptu mohou využít aplikace, jako je vysokofrekvenční ohřev, pro kterou linearita nepatří mezi kritické parametrem. Bylo prokázáno, že nadměrná výstupní kapacita tranzistoru snižuje výkon v této třídě zesilovačů, snižuje účinnost a omezuje jeho nejvyšší provozní frekvenci.

V této práci je navržena nová obvodová topologie pro umístění zařízení s nadměrnou výstupní kapacitou, čímž se zvýší účinnost a prodlouží maximální frekvence provozu. Navrhovaná topologie, složená z induktoru v sérii se subharmonickými rezonátory, nahrazuje stejnosměrný napájecí induktor v klasickém obvodu zesilovače třídy E.

Tímto způsobem je dosaženo kompenzace výstupní kapacity. V této práci jsou vyvinuty odpovídající teorie a návrhové rovnice. Pro ověření navržených konceptů byl navržen, postaven a změřen obvodový demonstrátor. Tento kompenzační přístup, který se v této práci nazývá frekvenčně závislá indukční kompenzace - FDIC (Frequency-Dependent Inductive Compensation), je dále hodnocen, tak aby byla pochopena jeho platnost ve spodní části mikrovlnného spektra.

Po extrahování zjednodušeného modelu GaN HEMT pro velké signály jsou využity rozsáhlé simulace k vyhodnocení dopadu nadměrné výstupní kapacity tranzistoru na třídu E. Tento přístup odstraňuje hlavní idealizaci při analýze této třídy zesilovačů, tedy, že přepínač je nahrazen napěťově řízeným zdrojem proudu. Použití extrahovaného modelu místo ideálního spínače nám umožňuje vyhodnotit účinky neideálního spínání, vlastní kapacitní závislost na napětí, zpětnovazební kapacity a saturačního odporu. Je studován vliv FDIC na průběhy napětí a proudu tranzistoru v topologii třídy E a jsou diskutována omezení tohoto přístupu. Ještě jednou je navržen a postaven demonstrátor obvodu pro ověření studie.

Závěrečná část práce se zabývá výkonovými zesilovači pro hypertermické systémy. Je navržen a postaven prototyp 250 W zesilovače pracujícího na frekvenci 70 MHz pro regionální hypertemii. V tomto případě jsou studovány dva přístupy k návrhu, a to pomocí konvenční metody návrhu třídy E založené na existujících rovnicích a za druhé pomocí load-pull simulací s využitím dostupného modelu zařízení LDMOS pro velký signál. Vlastní průběhy proudu a napětí se používají k vedení procesu návrhu a k optimalizaci účinnosti.

Nakonec se provádějí experimenty s vysokofrekvenčním ohřevem s použitím agarového fantomu, aby se vyhodnotil zesilovač při dodávání energie za podmínek blízkých reálným.

Keywords

power amplifier, class E amplifier, class J amplifier, switched mode amplifier, high efficiency, excess capacitance, inductive compensation, GaN HEMT, LDMOS, hyperthermia, agar phantom

Klíčová slova

výkonový zesilovač, zesilovač třídy E, zesilovač třídy J, spínaný zesilovač, vysoká účinnost, nadměrná kapacita, indukční kompenzace, GaN HEMT, LDMOS, hypertermie, agarový fantom

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List of Acronyms

ADS	Advanced Design System (trademark of Keysight)
AWG	American Wire Gauge
BOM	Bill of Materials
CCA	Current Conduction Angle
CMOS	Complementary Metal-Oxide Semiconductor
DAQ	Data Acquisition Unit
DDS	Direct Digital Synthesis
DXF	Drawing Interchange File Format
HPA	High Power Amplifier
IMN	Input Matching Network
MESFET	Metal Semiconductor Field Effect Transistor
MMIC	Monolithic Microwave Integrated Circuit
MRI	Magnetic Resonance Imaging
MW	Microwave
OMN	Output Matching Network
PA	Power Amplifier
PAE	Power Added Efficiency
PC Board	Printed Circuit Board
PC Class-E	Parallel-Circuit Class-E
SiC	Silicon Carbide
SMA	SubMiniature version A
SMD	Surface Mount Device
UHF	Ultra High Frequency
WPT	Wireless Power Transfer
ZCS	Zero-Current Switching
ZCD	Zero-Current Derivative Switching
ZDS	Zero Derivative Switching
ZDVS	Zero Derivative Voltage Switching
ZVD	Zero-Voltage Derivative Switching
ZVS	Zero-Voltage Switching

1 Introduction

1.1 Motivation

High-efficiency power amplifiers are not new to the industrial and medical fields being used in applications such as:

- RF welding of plastic materials [2]
- RF tumor ablation [16]
- Drivers for CO2 lasers [17]

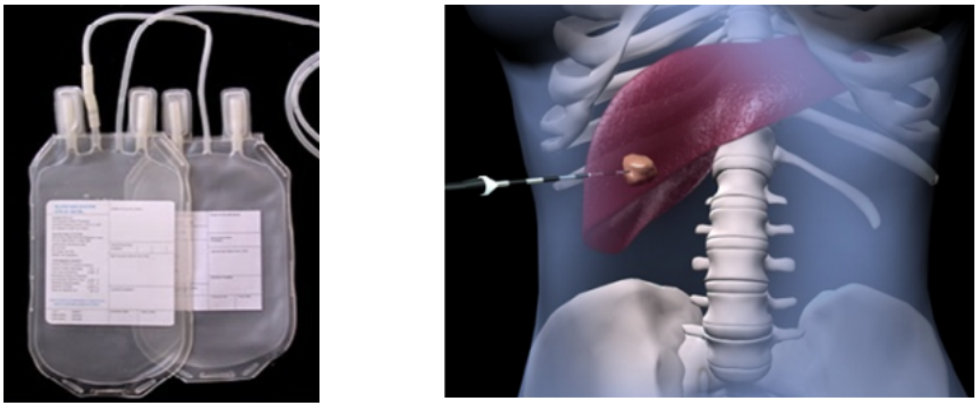
Those applications mostly use the ISM frequencies with power levels ranging from approximately 200 W to as high as 40 kW [2] - [17]. Figure 1.1 depicts two applications in which high RF power is used in medicine and industry, namely, RF welding of plastics and in tumor ablation. The powering of biomedical implants (e.g. by means of WPT[1]), biotelemetry and portable diagnostics are areas in which energy-efficient circuitry is required as revealed by the use of high-efficiency power amplifiers in those applications (see amplifier examples in figure 1.2). WPT for implants uses very low frequencies (< 1 MHz) [3] whereas biotelemetry might operate in the microwave range (e.g. 2.4 GHz) [4]. In both cases very low power levels (< 1 W) are required.
Among the high-efficiency power amplifier classes, the so-called switching-mode power amplifiers are widely used in industrial applications requiring high RF power (see examples in [18] [19]). The class-E power amplifier belongs to this category and is a very attractive solution, due to its high efficiency, simplicity of the load network at the same time that keeps its performance even under non-optimum driving conditions [20].

Although the use of higly-efficient power amplifiers in industrial and medical applications seems to be a subject which does not require major justification, having an idea of its impact is important. Therefore, few illustrative examples are given here. In order to do so, let's start by introducing the conventional definition of power amplifier efficiency:

$$\eta(\%) = \frac{P_{out}}{P_{dc}} \cdot 100 \tag{1.1}$$

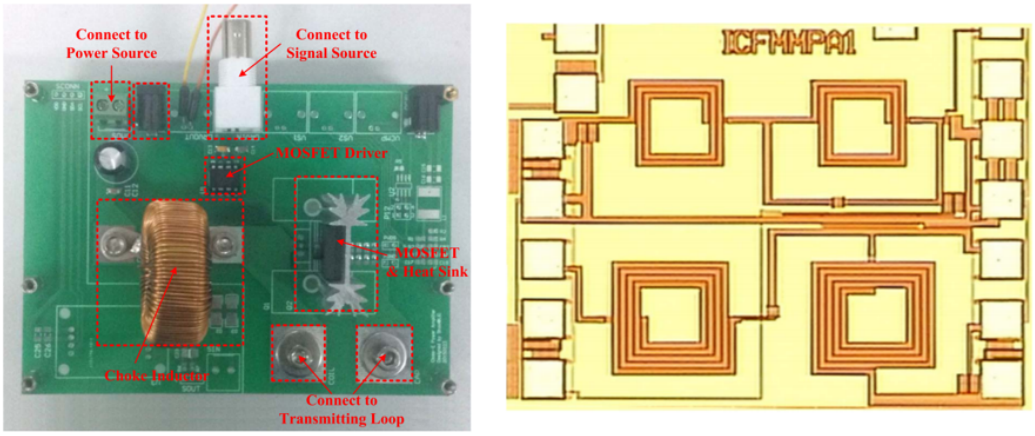
in which P_{out} represents the RF power delivered to the load and P_{dc} the DC power taken from the power supply[2]. Using this expression countours of constant RF output power can be generated.
Figure 1.3 shows the isopower lines for the range $P_{out} = (10 - 100)$ W and $\eta = (10 - 50)$ %.

[1] Wireless Power Transmission
[2] this efficiency is referred to as drain or collector efficiency. If RF input power is taken into account the Power-Added-Efficiency (PAE) is obtained



(a) (b)

Figure 1.1: RF power applied in a) welding of plastics like blood bags [1] and in b) tumor ablation [2]



(a) (b)

Figure 1.2: a) Example of discrete class-E PA ($\eta \approx 91$ %) for WPT in capsule endoscopic system [3] and b) PA in CMOS technology ($\eta \approx 35$ %) for biotelemetry [4]

This selected range fits well power amplifiers used in wireless communications, which are operated into so-called back-off, i.e. well below their saturated output power. This is required to comply with the high linearity requirements resulting from the operation with multi-carrier signals. This kind of operation on the other hand, causes the amplifiers to have very low efficiencies, all well below the 50 % mark. Experience shows that $(10-20)$ % are not unusual. Values reaching $(30-40)$ % are possible using for instance Doherty power amplifiers.[3]

[3] Author's note

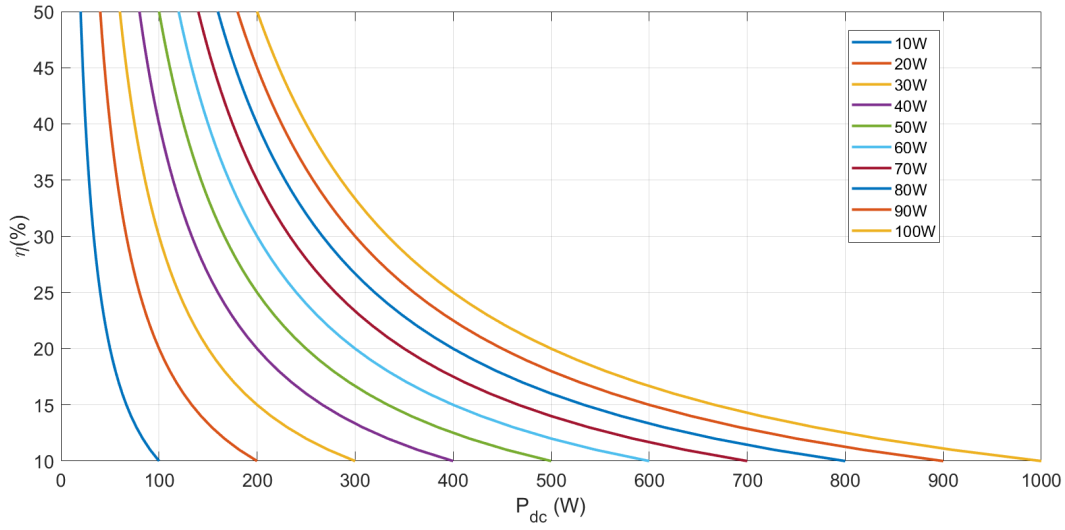


Figure 1.3: Isopower lines for $P_{out} = 10 - 100\ W$

An amplifier designed to deliver for instance 20 W and having an efficiency of 10 %, will consume 200 W from the power supply (see figure 1.3). Being able to double its efficiency (i.e. 20 %) would allow now to reduce the power comsumption to just 100 W. In other words, the power lost as heat on the PA is reduced from 180 W to 80 W. Power amplifiers are among the energy hungriest components in a cellular base station and aming at increasing their efficiency is a must to reduce the carbon footprint of mobile stations.
Power amplifiers used in industrial and medical applications on the other hand need to meet different requirements depending on the application. For Magnetic Resonance Imaging (MRI) for instance, power amplifiers are optimized for pulse operation (accurate and faithful pulse replication required throughout the amplification process [21]), must comply with certain level of linearity and are required to deliver high power. A 1 to 3-Tesla MRI system for extremities (arms, legs) might require between 500 W and 2 kW but for whole body scanners amplifiers up to 35 kW have been used [22].
For hyperthermia applications modern commercial systems exist with different power levels and operating frequencies depending on the location of the tumor to be treated. For superficial hyperthermia, i.e. tumors within 1 inch of the skin surface, an 8-channel systems might deliver up to 480 W (60 W/channel) operating at 915 MHz [23]. For deep regional hyperthermia (e.g. to treat pelvic or abdominal tumors) systems operate at around $(75 - 140)$ MHz for higher penetration and use total[4] power levels in the order of $(1.3 - 1.8)$ kW [24]. These systems require an adequate control of the power per channel and phase of the signals sent to the applicators.
Figure 1.4 now shows the isopower lines for the range $P_{out} = (100 - 1000)$ W and $\eta = (50 - 100)$ %, a range that would better suit amplifiers used in industrial and medical applications.

A $2 - $kW power amplifier for 3T MRI might have an efficiency slighly above 60 % [25],

[4]The power can be delivered through a single channel or distributed among several channels

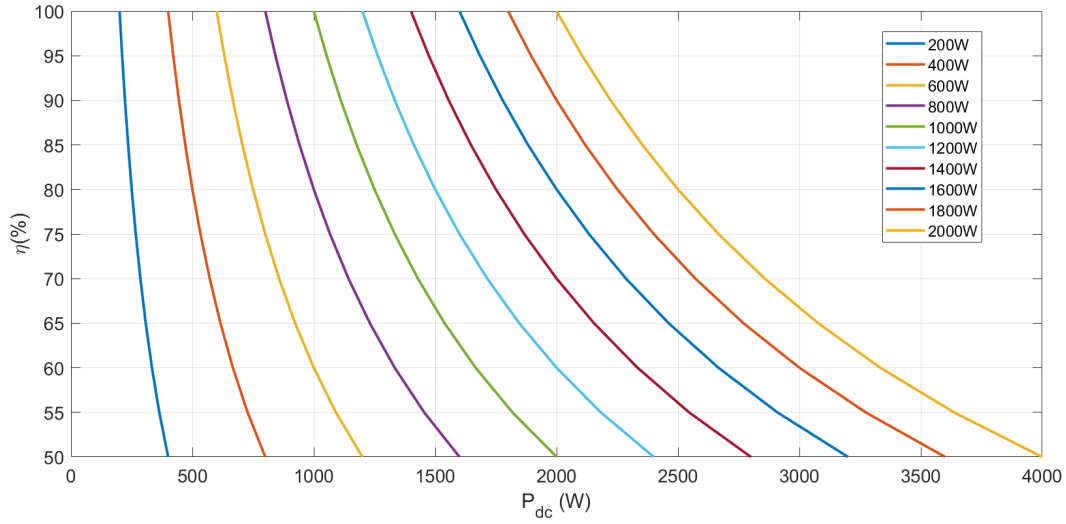


Figure 1.4: Isopower lines for $P_{out} = 100 - 1000\ W$

requiring around 3.3 kW from the power supply (see figure 1.4), i.e. 1.3 kW remain within the PA as heat. Some vendors offer power amplifiers for hyperthermia having efficiencies below 50 % [23]. For RF cooking RF power amplifier modules using solid-state devices have been developed operating at 2.45 GHz and with power levels of 250 W. This development systems offer typical efficiencies around 57 % [26]. A different situation holds for systems used in plasma excitation, in which switch-mode amplifiers are used, obtaining efficiencies in the order of 80 % [18].
As illustrated by these few examples, there is a real need for improving energy efficiency in RF medical systems. The advantages offered by highly-efficient power amplifiers in this case are:

- Reduced operational costs
- Reduced cooling requirements
- Usage of smaller power supplies
- Overall reduction of carbon footprint

In the case of hyperthermia systems, these advantages translate into compact and lighter systems, in agreement with the trend of having the RF sources closer to the pacient (e.g. by embedding RF generators into treatment bed). This allows on the other hand to use shorter cables between sources and the applicators to reduce RF losses and thus further improve the system overall efficiency.

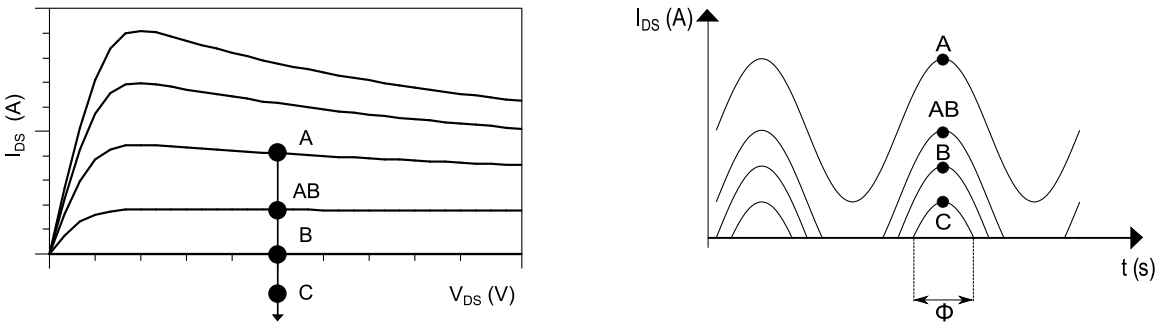
2 RF Power Amplifier Fundamentals

The classification of power amplifiers (PA) seems to obey historical reasons. Although different amplifier working principles have been developed in subsequent years, the use of the *alphabetical classification* is still adopted throughout the PA community, regardeless of the underlying principle of operation. In this section an overview of the existing high-efficiency power amplifier architechtures will be presented, starting with a short introduction of the so-called *conventional* amplifier classes.

2.1 Conventional Power Amplifiers

Conventional power amplifiers are classified in four mayor classes, namely **Class A**, **Class AB**, **Class B** and **Class C** as depicted in figure 2.1a. This classification is made based on either their biasing condition (quiscient point) or in terms of the conduction angle Φ of the current at the output terminals of the device, i.e. the fraction of the radio frequency signal (wihtin a period) where a non-zero current is flowing [27]. Since the the current conduction angle (CCA) might change with the input drive level, this classification criteria is somehow misleading, therefore the classification based on the quiscient point will be used here. A more detailed treatment on amplifier classes and their characteristics can fe found in [28, 29, 30].

The generic topology of a conventional power amplifier is shown in 2.2. For the class-A amplifier, the quiscient point is selected such that a constant DC current of approximately half the maximum drain current (I_{max}) is circulating through the device. The conduction angle is $\Phi = 360°$ and the amplifier operates in the linear portion of its characteristic and hence minimum signal distortion is obtained. Although in theory the parallel-tuned circuit



(a) Quiscent point

(b) Current conduction angle

Figure 2.1: Amplifier class according to a) biasing condition and b) current conduction angle (CCA)

can be omitted, non-ideal devices being not completely linear generate harmonics that must be prevented from reaching the load.

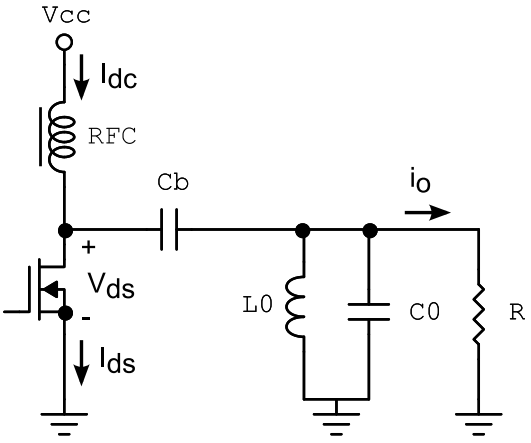


Figure 2.2: Conventional amplifier topology

Some authors use the term Tuned-Load (TL) to refer to the operating mode obtained by conventional power amplifiers (e.g. class-AB) using the topology in figure 2.2, in which the ideal output tank present a short circuit at all harmonics [27]. Although a pure resistive termination could be assumed, the circuit topology shown above not only is widely use in the classical literature [31, 30, 32] but also simplifies the analysis, due to the assumption of sinusoidal output volatge.

2.1.1 Generalized Analysis of Conventional Power Amplifiers

The general class-AB waveforms shown in figure 2.3 will be used as the starting point for the analysis. The device is biased at the gate side with a dc voltage V_{GSQ} producing a quiscient current I_{DSQ} at the drain side, this causes the transistor to have a CCA Φ between π and 2π for input drives high enough to allow the drain current to reach I_{Dmax}. As done in the classical literature and in order to facilitate the notation, a cosine function has been selected to represent the truncated sinewave seen in figure 2.3 [33].

The the drain current is composed of the quiscient current I_{DSQ} and a cosinusoidal wave of peak amplitude I_{dspeak} and can be written as follows

$$i_{ds}(\theta) = \begin{cases} I_{DSQ} + I_{dspeak} \cdot cos(\theta) & |\theta| \leq \Phi/2 \\ 0 & \text{otherwise} \end{cases} \tag{2.1}$$

for $\theta = \Phi/2$ the current is zero, i.e. $i_{ds}(\Phi/2) = I_{DSQ} + I_{dspeak} \cdot cos(\Phi/2) = 0$ and the following equation results

$$cos(\Phi/2) = -\frac{I_{DSQ}}{I_{dspeak}} \tag{2.2}$$

for $\theta = 0$ the current is at its maximum, i.e. $i_{ds}(0) = I_{DSQ} + I_{dspeak} = I_{Dmax}$. This equation can be rewritten as follows

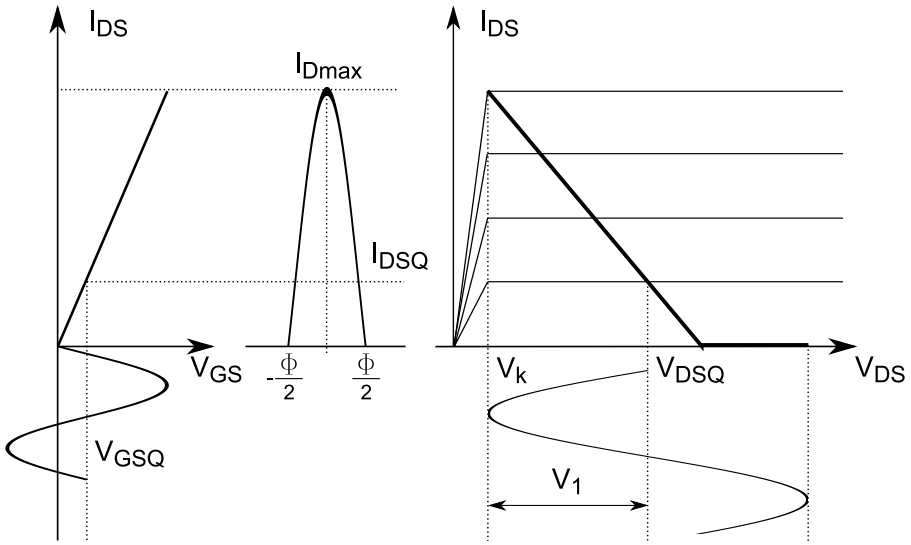


Figure 2.3: General waveform of class-B amplifier

$$I_{Dmax} = I_{dspeak} \cdot \left(1 + \frac{I_{DSQ}}{I_{dspeak}}\right) = I_{dspeak} \cdot [1 - cos(\Phi/2)] \tag{2.3}$$

and by using expressions 2.2 and 2.3 into equation 2.1 the truncated waveform as a function of Φ and I_{Dmax} and for $|\theta| \leq \Phi/2$ can be determined

$$i_{ds}(\theta) = \frac{I_{Dmax}}{1 - cos(\Phi/2)} \cdot [cos\theta - cos(\Phi/2)] \tag{2.4}$$

The Fourier decomposition of an even function as the one described by 2.4 is given by

$$i_{ds}(\theta) = I_0 + \sum_{n=1}^{\infty} I_n \cdot cos(n \cdot \theta) \tag{2.5}$$

with

$$I_0 = \frac{1}{2\pi} \int_{-\Phi/2}^{\Phi/2} \frac{I_{Dmax}}{1 - cos(\Phi/2)} \cdot [cos\theta - cos(\Phi/2)] \cdot d\theta \tag{2.6}$$

$$I_n = \frac{1}{\pi} \int_{-\Phi/2}^{\Phi/2} \frac{I_{Dmax}}{1 - cos(\Phi/2)} \cdot [cos\theta - cos(\Phi/2)] \cdot cos(n \cdot \theta) \cdot d\theta \tag{2.7}$$

Evaluating these integrals results in the expressions 2.8 to 2.10 [27], where the normalization constant $a = I_{Dmax}/2\pi$ has been introduced

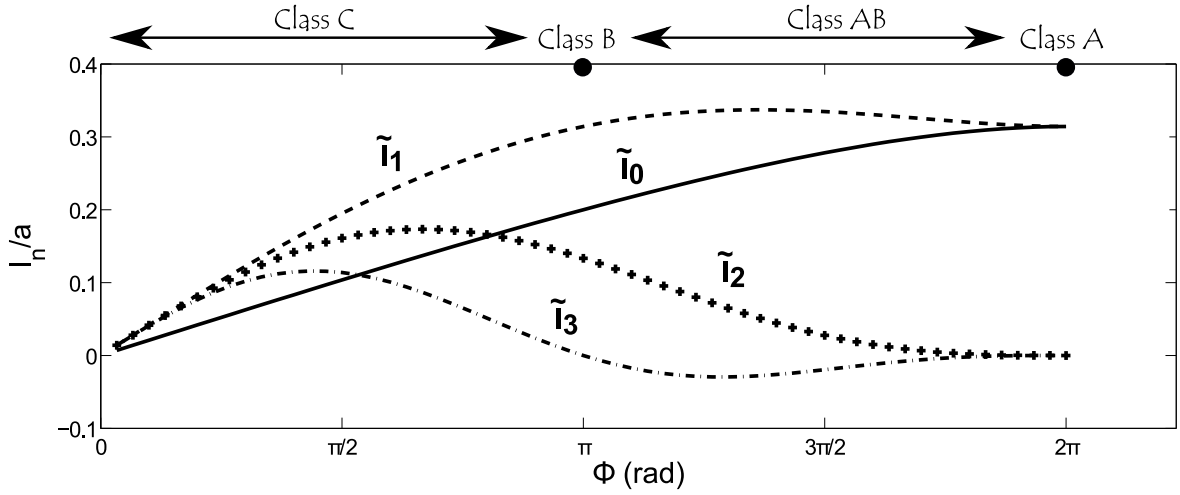


Figure 2.4: Fourier components of drain current

$$I_0 = a \cdot \frac{2 \cdot sin(\Phi/2) - \Phi \cdot cos(\Phi/2)}{1 - cos(\Phi/2)} \tag{2.8}$$

$$I_1 = a \cdot \frac{\Phi - sin(\Phi)}{1 - cos(\Phi/2)} \tag{2.9}$$

$$I_{n\geq 2} = 4a \cdot \frac{sin(n \cdot \Phi/2) \cdot cos(\Phi/2) - n \cdot sin(\Phi/2) \cdot cos(n \cdot \Phi/2)}{n \cdot (n^2 - 1) \cdot [1 - cos(\Phi/2)]} \tag{2.10}$$

The DC, fundamental, second and third harmonic drain current components as function of Φ are shown in figure 2.4, with $\widetilde{I}_n = I_n/a$. As the CCA is reduced the drain/collector waveform goes through a shaping process, starting with a pure sinusoidal signal at $\Phi = 2\pi$ and approaching a current pulse as the CCA get smaller. Furthermore, the duty cycle starts decreasing causing a reduction of the DC component as exposed in figure 2.4. At the same time, the narrowing of the waveform increases the harmonic content present in the signal. For instance, the class-B power amplifier exhibits not only a DC component but also the fundamental as well as the even harmonics, allowing the current waveform to adopt a half-sinusoidal shape[1]. Remarcable is the fact that the class-B power amplifier draws less DC current from the power supply (by a factor of $2/\pi$) compared to the class A case, whereas the the fundamental component for both amplifier classes is equal to $I_1^{A,B} = I_{Dmax}/2$ (giving an indication of efficiency boosting by a factor of $\pi/2$ when moving from $\Phi = 2\pi$ to $\Phi = \pi$).

As it was mentioned at beginning of this section, all harmonics of the load are shorted by the output resonator and consequently the drain voltage is a sinewave whose amplitude will be defined by the fundamental component I_1 and by the load resistor R (see figure 2.2). Therefore, the drain voltage can be expressed as follow

[1] Although only the 2nd and 3rd harmonics are depicted here, in theory an infinite number of harmonics is present

$$V_{ds}(\theta) = V_{DSQ} - V_1 \cdot cos(\theta) \tag{2.11}$$

where V_{DSQ} is the quiscient drain voltage and V_1 the amplitude of the drain voltage swing, assumed to be given by the difference of the drain bias and the knee voltage of the device as depicted in figure 2.3, thus

$$V_1 = V_{DSQ} - V_k = V_{DSQ} \cdot (1 - k) \tag{2.12}$$

By using the values of V_1 and I_1 it is possible to find the relations for the optimum resistance, output power and efficiency as a function of the CCA as follows

$$R_{opt}(\Phi) = \frac{V_1}{I_1(\Phi)} = 2\pi \cdot \frac{V_{DSQ} \cdot (1-k)}{I_{Dmax}} \cdot \frac{1 - cos(\Phi/2)}{\Phi - sin(\Phi)} \tag{2.13}$$

$$P_{DC}(\Phi) = I_0 \cdot V_{DSQ} = \frac{V_{DSQ} \cdot I_{Dmax}}{2\pi} \cdot \frac{2 \cdot sin(\Phi/2) - \Phi \cdot cos(\Phi/2)}{1 - cos(\Phi/2)} \tag{2.14}$$

$$P_{RF}(\Phi) = \frac{1}{2} \cdot V_1 \cdot I_1 = \frac{V_{DSQ} \cdot (1-k) \cdot I_{Dmax}}{4\pi} \cdot \frac{\Phi - sin(\Phi)}{1 - cos(\Phi/2)} \tag{2.15}$$

$$\eta(\Phi) = \frac{P_{RF}(\Phi)}{P_{DC}(\Phi)} = \frac{(1-k)}{2} \cdot \frac{\Phi - sin(\Phi)}{2 \cdot sin(\Phi/2) - \Phi \cdot cos(\Phi/2)} \tag{2.16}$$

As an example the specific values for the class-A and B power amplifiers are presented in table 2.1. The general expressions 2.13, 2.15 and 2.16 can be used to display the relation between the drain efficiency η and output power P_{RF} taking into account the changes in R_{opt} for all values of Φ as can be seen in figure 2.5. In this case the knee voltage has been assumed to be zero ($k = 0$) and the output power has been normalized by using the P_{RF} of the class A in table 2.1.

Table 2.1: Equations for class-A and B amplifiers

Variable	***Class A*** ($\Phi = 2\pi$)	***Class B*** ($\Phi = \pi$)
$R_{opt}\,(\Omega)$	$2 \cdot \frac{V_{DSQ} \cdot (1-k)}{I_{Dmax}}$	$2 \cdot \frac{V_{DSQ} \cdot (1-k)}{I_{Dmax}}$
$P_{DC}\,(W)$	$\frac{1}{2} \cdot V_{DSQ} \cdot I_{Dmax}$	$\frac{1}{\pi} \cdot V_{DSQ} \cdot I_{Dmax}$
$P_{RF}\,(W)$	$\frac{1}{4} \cdot V_{DSQ} \cdot (1-k) \cdot I_{Dmax}$	$\frac{1}{4} \cdot V_{DSQ} \cdot (1-k) \cdot I_{Dmax}$
η	$\frac{1}{2} \cdot (1-k)$	$\frac{\pi}{4} \cdot (1-k)$

In figure 2.5 two relations are displayed. The solid line presents the efficiency η as a function of output power P_{RF} , whereas the dotted line shows the efficiency η as a function of the optimum load resistor $R_{opt(norm)} = R_{opt}(\Phi)/R_{opt}(2\pi)$[2]. The efficiency of the amplifier can be increased by reducing the CCA, theoretically reaching 100 %, but this would imply zero output power (this can be also seen in figure 2.4 where the current and its harmonics go

[2]The scale of the horizontal axis is used for both $P_{RF(norm)}$ and $R_{opt(norm)}$

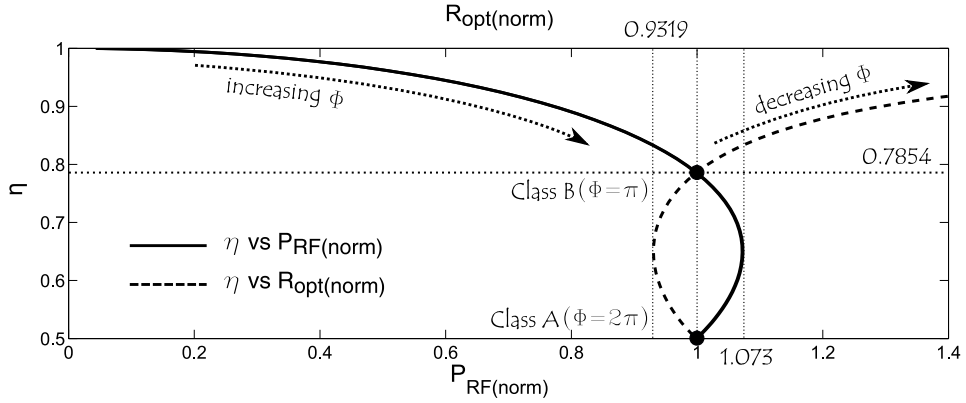


Figure 2.5: Relation between $\eta(\Phi)$ and $P_{RF}(\Phi)$

to zero), in addition to this $R_{opt} \to \infty$[3]. The maximum power is obtained with the class-AB configuration, being approximately 7.3% higher than the power of the class A and B. This increase in the output power is accomplished by reducing R_{opt} by 6.8% and the efficiency in this case is equal to $\sim 65\%$. Although certain idealizations have been considered here (zero knee voltage, constant transconductance, high gate breakdown voltage, infine number of harmonis, etc), these results represent a good approximation in terms of what could be expected from a device operating under certain biasing conditions and using a very specific topology. Nevertheless, later on in the study of high-efficiency amplification techniques, it will be shown that unexpected results can be obtained from conventional amplifier classes by releasing some of these idealizations.

2.2 High Efficiency Amplifier Concepts

This section presents an overview of the most common high-efficiency amplification techniques. Although there is not a straightforward way of classifying those amplifier concepts[4], three mayor groups are used in this section to categorize them, namely *polyharmonic*, *overdriven* and *switched-mode*. The first category is more easily understood when described from the cronological point of view, from here that a short review of early concepts is presented.

2.2.1 Polyharmonic Approaches and Early Concepts

One of the first reports dealing with the efficiency of power amplifiers and RF generators corresponds to the analysis by Latour and Chireix back to 1923 [5]. At that time the authors indicated that the anode-circuit efficiency of three-electrode tubes (triodes)[5] operating as radio frequency generators, could attain values in excess of 70 % to 80 % overcoming the

[3] In the graph the highest value of the abscissa es 1.4 but it extends to infinity to the right

[4] Colantonio et al. [27] propose a classification based on current-mode and switched-mode operation

[5] Triode: 3-terminal active device. The Cathode emits electrons (when heated by a filament) towards the Anode or Plate (biased positively), while the Grid (input) constrols the electron flow between Anode and Cathode

50 % value reported then in the literature. In order to understand how this efficiency increase is achieved consider the basic amplifier topology shown in fig. 2.6.

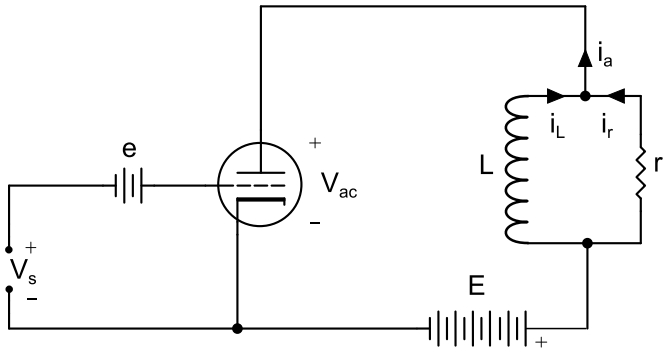


Figure 2.6: Amplifier circuit from [5]

The efficiency in this case can be defined as:

$$\eta = \frac{P_r}{P_{dc}} = \frac{i^2_{r(rms)} \cdot r}{i_{dc} \cdot E} \tag{2.17}$$

The RF choke L can be considered as a short circuit at DC, therefore $i_L = i_{dc} \left(= \frac{1}{T} \int_0^T i_a \cdot dt \right)$ and the current i_r flowing through the resistor r is given by $i_r = i_a - i_{dc}$. Using the expression for the root mean square value of the current throught the load results in:

$$\begin{aligned} \eta &= \frac{\left(\sqrt{\frac{1}{T} \int_0^T (i_a - i_{dc})^2 \cdot dt} \right)^2 \cdot r}{i_{dc} \cdot E} = \frac{\left[\frac{1}{T} \int_0^T \left(i_a^2 - 2 \cdot i_a i_{dc} + i_{dc}^2 \right) \cdot dt \right] \cdot r}{i_{dc} \cdot E} \\ &= \frac{\left(i^2_{a(rms)} - i^2_{dc} \right) \cdot r}{i_{dc} \cdot E} \end{aligned} \tag{2.18}$$

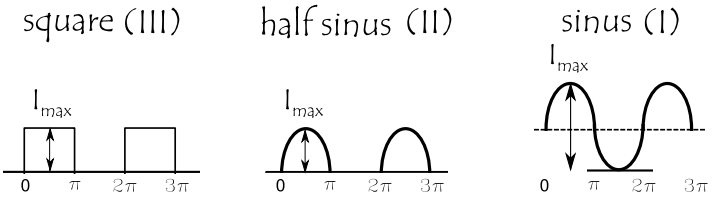
In [5] it is assumed that the anode current reaches a maximum value i_{max} (saturation current) ocurring at maximum grid potential. In this case, the voltage across the anode and cathode is given as follows[6]

$$\varepsilon = V_{ac} \,|_{i_a = i_{max}} = E - r \cdot (i_{max} - i_{dc}) \tag{2.19}$$

resulting in the following expression for the efficiency

$$\eta = \frac{\left(i^2_{a(rms)} - i^2_{dc} \right)}{i_{dc} \cdot E} \left(\frac{E - \varepsilon}{i_{max} - i_{dc}} \right) = \left(1 - \frac{\varepsilon}{E} \right) \frac{\left(\frac{i^2_{a(rms)}}{i^2_{dc}} - 1 \right)}{\left(\frac{i_{max}}{i_{dc}} - 1 \right)} = \left(1 - \frac{\varepsilon}{E} \right) \cdot K_i \tag{2.20}$$

[6] This anode-catothe voltage is equivalent to the knee voltage in a field effect transistor with r designating the load line



$i_{a(rms)}$	$\frac{i_{max}}{\sqrt{2}}$	$\frac{i_{max}}{2}$	$\sqrt{\frac{3}{8}} i_{max}$
i_{dc}	$\frac{i_{max}}{2}$	$\frac{i_{max}}{\pi}$	$\frac{i_{max}}{2}$
K_i	1	0.685	0.5
η	$1 - \frac{\epsilon}{E}$	$0.685\left(1 - \frac{\varepsilon}{E}\right)$	$0.5\left(1 - \frac{\varepsilon}{E}\right)$

Figure 2.7: Summary of waveform-dependent efficiency according to [5]

Equation 2.20 suggests that different wave-shapes of the anode current will result in different levels of efficiency. Three types of waveforms are considered in [5] as examples of possible anode currents. These results are summarized in figure 2.7.

Waveform (I) represents the classical class-A case with 50% efficiency, whereas case (II) exhibits the same current waveform as the conventional class-B amplifier. On the other hand, it can be seen that the efficiency in this case is merely 68.5% instead of the 78.5% expected for this operating class (see figure 2.5). Due to the absence of the output resonator in Latour's circuit, this amplifier behaves as a resistive-loaded class-B topology giving rise to different values of efficiency (calculation of the drain efficiency for this specific case can be found in Appendix A).

Figure 2.7 also indicates that increased efficiency can be obtained by shaping the anode current towards a square waveform. It is important to remember that the output current i_r will not be sinusoidal and that filtering is required to allow only the fundamental frequency component to be transmitted to the load. Latour and Chireix proposed an alternative circuit composed of a shunt L_1C_1 resonator followed by a series L_2C_2 resonator (see figure 2.8), both tuned to the fundamental and showed that the efficiency values decrease as compared with those given in figure 2.7. Inspection of this topology reveals that the anode-cathode voltage will be sinusoidal whereas the anode current might be shaped to a half sinusoidal (depending on grid biasing) but not to a square waveform, therefore this circuit resembles the conventional topology shown in figure 2.2.

It is interesting to note that Latour and Chireix did not consider the current conduction angle in their analysis, something done later on by Scott in 1963 [34], who calculated the efficiency for the three waveforms above as a function of Φ.

Prince [6] took a step forward in analyzing the high efficiency operation of radio frequency oscillators and amplifiers. In the third part of his paper from 1923, he indicated that by making the load circuit responsive to certain harmonics, it is possible to change the output power and efficiency of a power oscillator. In order to increase efficiency, it is necessary to keep the instantaneous anode to cathode voltage drop as small as possible for that portion of the period in which a non-zero anode current flows. This can be achieved by using harmonics in proper phase relations to modify the anode-cathode voltage waveform to obtain a flat topped wave. Prince suggested to use a circuit containing a resonance trap

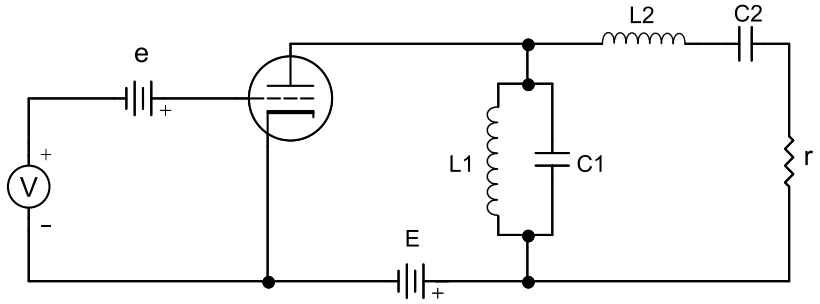


Figure 2.8: Amplifier circuit with output resonators from [5]

to allow for the harmonic to build up. This circuit is shown in figure 2.9. He suggested to use a 3rd or a 5th harmonic component and defined the minimum current conduction angle required to flatten the voltage waveform.

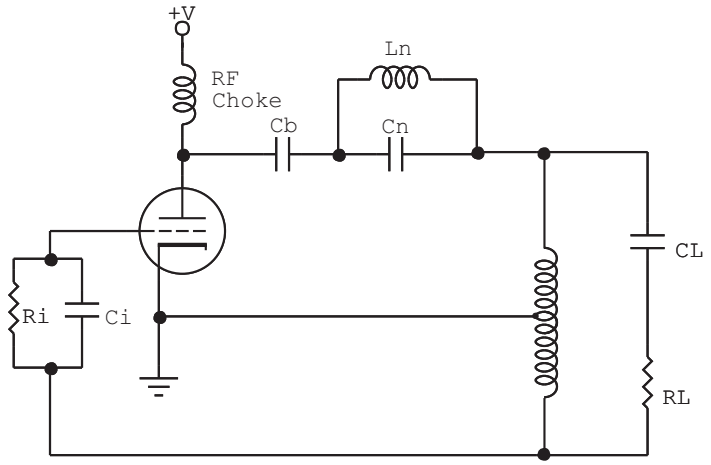


Figure 2.9: Harmonic trap oscillating circuit from [6]

The concept of anode-voltage flattening was retaken by Tyler in 1958 [7], who indicated that by using a large number of resonators in the anode circuit, it is possible to shape the anode-cathode voltage to obtain either a square or a half-rectified sinusoidal signal. In this case a broader anode current pulsed can be used without degrading efficiency. The circuits suggested by Tyler are shown in figure 2.10, whereby the resonators can be made resonant either at the even or odd harmonics to modify the shaping of the voltage waveform. In addition to this, the drive waveform is not required to have the same harmonics for which anode resonators have been provided.

Compared with the most common class-C amplifier, a significant fraction of the power delivered by the amplifier kind shown in figure 2.10 comes from the interaction of the harmonic current and the fundamental voltage[7]. In this case, the non-linear characteristics of the well-driven active device plays also an important role in how these frequency components interact with each other.

[7]Effective power resulting from the interaction of two signals having different frequencies is only possible if the integration is performed over periods shorter than one cycle

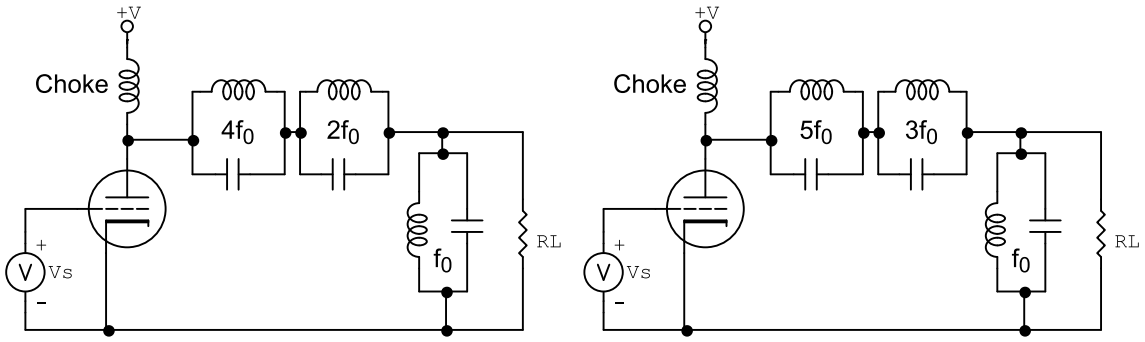


Figure 2.10: Amplifier with even-harmonic resonators from [7]

Several authors have applied the concept of harmonic loading to improve efficiency in power amplifiers [35, 36], but only a few of those have been reported in this section. An extended literature review concerning early high-efficiency amplifier concepts can be found in [37].

The approaches presented in this section can be summarized as follows:

- *Squaring of anode current* (Latour and Chireix): shaping of anode current to obtain $\eta \approx 100\%$
- *Voltage-Current overlap reduction* (Prince): keeping the instantaneous anode to cathode voltage drop as small as possible for that portion of the period in which a non-zero anode current flows. Requires the use of 3rd or 5th harmonic tank at anode side and defining appropriate CCA to flatten voltage waveform
- *Polyharmonic approach* (Tyler): using large number of either even or odd harmonic resonators in anode circuit to obtain square or half sinusoidal signal

In the next section it will be seen that the concept of waveform shaping (by means of harmonic resonators) to decrease current and voltage overlap reappears, but this time as the result of analyzing the conventional power amplifier architectures introduced at the begining of this chapter. It is especially important to remember that although non-overlapping is necessary, it is not enough to guarantee best levels of efficiency. This can be exemplified by considering the squared-shaped voltage and current waveforms in [5], which promise an efficiency of 100% since no overlap is present. Although this is true, only the fundamental component is desired, in which case the efficiency reduces to $\sim 81\%$ since the rest of the power is wasted in harmonic generation (see page 151 in [32]).

2.2.2 Overdriven Power Amplifiers

In his paper from 1967, Snider [38] stated that by appropriate selection of the load impedance at the fundamental and harmonic frequencies, connected at the output terminal of a tuned amplifier, it would be possible to exceed the efficiency and output power of the classical class-B amplifier (see section 2.1.1). Furthermore, a theoretical efficiency of 100% at 1.27 times the output power of class-B is possible. In addition to this, a 46% increase in output power can be obtained by overdriving the amplifier, achieving in this case an efficiency of

about 88%. The first case (having 100% efficiency) is what he called *optimum efficiency* class B amplifier, whereas the latter case is the so-called *overdriven* class-B RF power amplifier.

In order to understand how this efficiency enhancement is obtained, consider the waveforms in figure 2.11. The drain current exhibits the classical class-B waveform with CCA of $\Phi = \pi$, however the drain voltage is allowed to change, showing a rather flat topped waveform.

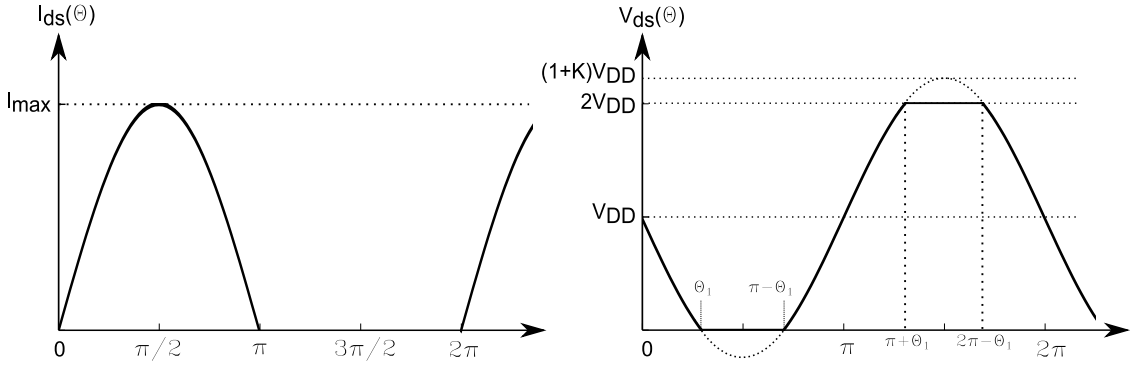


Figure 2.11: Waveforms for optimum efficicency class B

The Fourier coefficients of the current waveform can be obtained by using equations 2.8 to 2.10, obtaining

$$i_{ds}(\theta) = \frac{I_{max}}{\pi} + \frac{I_{max}}{2} \cdot sin(\theta) + \frac{I_{max}}{\pi} \cdot \sum_{n=2,4,6...} \left[\frac{1}{1-n} + \frac{1}{1+n} \right] \cdot cos(n \cdot \theta) \tag{2.21}$$

where it can be seen that the third term at the right side of the equation represents the even harmonics of the fundamental signal. The DC component of the drain voltage is equal to the supply voltage, i.e. $V_0 = V_{DD}$, but determinig the rest of the coefficients requires integration by parts as follows[8]

$$\begin{aligned} V_n &= \frac{1}{\pi} \left[\int_0^{\theta_1} V_{ds}(\theta) \cdot sin(n \cdot \theta) + \int_{\theta_1}^{\pi-\theta_1} (V_{DD}) \cdot sin(n \cdot \theta) + \int_{\theta_1-\pi}^{\pi+\theta_1} V_{ds}(\theta) \cdot sin(n \cdot \theta) \right. \\ &\quad \left. + \int_{\pi+\theta_1}^{2\pi-\theta_1} (-V_{DD}) \cdot sin(n \cdot \theta) + \int_{2\theta_1-\pi}^{2\pi} V_{ds}(\theta) \cdot sin(n \cdot \theta) \right] \end{aligned} \tag{2.22}$$

with $V_{ds}(\theta) = K \cdot V_{DD} \cdot sin(\theta)$. The integration in 2.22 can be used to obtain the coefficients for the fundamental and harmonics as a function of θ_1 [39, 38]

$$V_1 = V_{DD} \left[\frac{2 \cdot K \cdot \theta_1}{\pi} - \frac{K \cdot sin(2\theta_1)}{\pi} + \frac{4 \cdot cos(\theta_1)}{\pi} \right] \tag{2.23}$$

$$V_n = \frac{2 \cdot V_{DD}}{\pi} \left[K \cdot \frac{sin(1-n)\theta_1}{1-n} - K \cdot \frac{sin(1+n)\theta_1}{1+n} + \frac{2 \cdot cos(n\theta_1)}{n} \right] \tag{2.24}$$

[8]Since $V_{ds}(\theta)$ is an odd function, it does not contain cosine terms in its Fourier expansion

with V_n representing the coefficients of the odd harmonics (i.e. $n = 3, 5, 7...$). In the equations above K represents the overdrive factor and is defined as $K = 1/sin(\theta_1)$ [39].

As θ_1 tends to zero the drain voltage approaches a square wave, so that evaluating equations 2.23 and 2.24 for the case $\theta_1 \to 0$ results in

$$V_1 = \frac{4 \cdot V_{DD}}{\pi} \tag{2.25}$$

$$V_n = \frac{4 \cdot V_{DD}}{\pi \cdot n} \tag{2.26}$$

and the equation for the voltage can be written as

$$V_{ds}(\theta) = V_{DD} + \frac{4 \cdot V_{DD}}{\pi} sin(\theta) + \frac{4 \cdot V_{DD}}{\pi} \cdot \sum_{n=3,5,...} \frac{sin(n\theta)}{n} \tag{2.27}$$

The Fourier decompositions in 2.21 and 2.27 can be used to determined the key figures of the optimum efficiency tuned amplifier

$$P_{DC} = \frac{1}{\pi} \cdot V_{DD} \cdot I_{max} \tag{2.28}$$

$$P_{out} = \frac{1}{\pi} \cdot V_{DD} \cdot I_{max} \tag{2.29}$$

$$R_{opt} = \frac{8}{\pi} \cdot \frac{V_{DD}}{I_{max}} \tag{2.30}$$

$$Z_n = \begin{cases} 0 & n\,even \\ \infty & n\,odd \end{cases} \tag{2.31}$$

The second approach suggested by Snider [38] is illustrated in figure 2.12. In this case not only the voltage but also the drain current is allowed to change, exhibiting again a flat topped waveform.

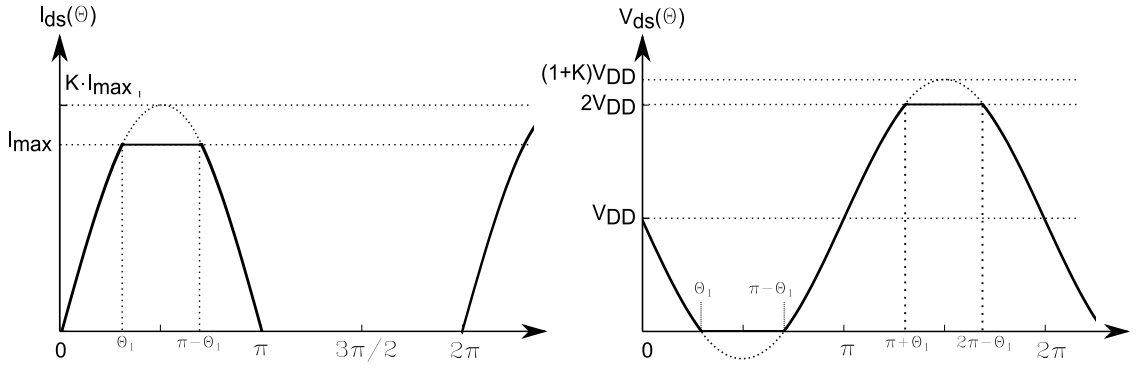


Figure 2.12: Waveforms for optimum power class B

Fourier decomposition of the current waveform results in [38]

$$I_0 = \frac{I_{max}}{2\pi}\left[2K\cdot(1-cos(\theta_1))+\pi-2\theta_1\right] \quad (2.32)$$

$$I_1 = \frac{I_{max}}{2}\left[\frac{2\cdot K\cdot\theta_1}{\pi}-\frac{K\cdot sin(2\theta_1)}{\pi}+\frac{4\cdot cos(\theta_1)}{\pi}\right] \quad (2.33)$$

$$I_n = \frac{I_{max}}{\pi}\left[K\cdot\frac{sin(1-n)\theta_1}{1-n}-K\cdot\frac{sin(1+n)\theta_1}{1+n}+\frac{2\cdot cos(n\theta_1)}{n}\right] \quad (2.34)$$

with I_n representing the coefficients of the odd harmonics (i.e. $n = 3, 5, 7...$). The DC and output power can be calculated using ecuations 2.23,2.32 and 2.33

$$P_{DC} = \frac{V_{DD}\cdot I_{max}}{2\pi}\left[2K\cdot(1-cos(\theta_1))+\pi-2\theta_1\right] \quad (2.35)$$

$$P_{out} = \frac{V_{DD}\cdot I_{max}}{4\pi^2}\left[2\cdot K\cdot\theta_1-K\cdot sin(2\theta_1)+4\cdot cos(\theta_1)\right]^2 \quad (2.36)$$

$$\eta = \frac{1}{2\pi}\frac{\left[2\cdot K\cdot\theta_1-K\cdot sin(2\theta_1)+4\cdot cos(\theta_1)\right]^2}{\left[2K\cdot(1-cos(\theta_1))+\pi-2\theta_1\right]} \quad (2.37)$$

The maximum efficiency of the overdriven class-B is $\eta = 88.6\%$ and occurs at an angle $\theta_1 = 32.4°$. Table 2.2 summarizes the more general features of the optimum efficiency and optimum power class-B amplifiers including the conventional case for comparison purposes.

Table 2.2: Summary of class-B amplifiers

Variable	***Conventional*** ($\theta_1 = \pi/2$)	***Optimum Eff.*** ($\theta_1 = 0$)	***Optimum Power*** ($\theta_1 = 32.4°$)
$R_{opt}\,(\Omega)$	$2\frac{V_{DD}}{I_{max}}$	$\frac{8}{\pi}\cdot\frac{V_{DD}}{I_{max}}$	$2\frac{V_{DD}}{I_{max}}$
$P_{DC}\,(W)$	$\frac{1}{\pi}\cdot V_{DD}\cdot I_{max}$	$\frac{1}{\pi}\cdot V_{DD}\cdot I_{max}$	$0.4125\cdot V_{DD}\cdot I_{max}$
$P_{RF}\,(W)$	$\frac{1}{4}\cdot V_{DD}\cdot I_{max}$	$\frac{1}{\pi}\cdot V_{DD}\cdot I_{max}$	$0.3656\cdot V_{DD}\cdot I_{max}$
η	$\frac{\pi}{4}$	1	0.886
Z_n	$\begin{cases}0 & n\,even\\ 0 & n\,odd\end{cases}$	$\begin{cases}0 & n\,even\\ \infty & n\,odd\end{cases}$	$\begin{cases}0 & n\,even\\ 2\frac{V_{DD}}{I_{max}} & n\,odd\end{cases}$

The optimum efficiency case, having a half-wave rectified drain current and a maximally flat sinewave drain voltage is nowadays known as *class-F* power amplifier [33, 31][9]. The topology of this amplifier type is similar to the one showed in figure 2.10, in which one or multiple resonators in serie are used to control the harmonics of the voltage and current

[9] Additional names are: high-efficiency class C, class C using harmonic injection, class CD, single-ended class D, biharmonic or polyharmonic class C, etc [40]

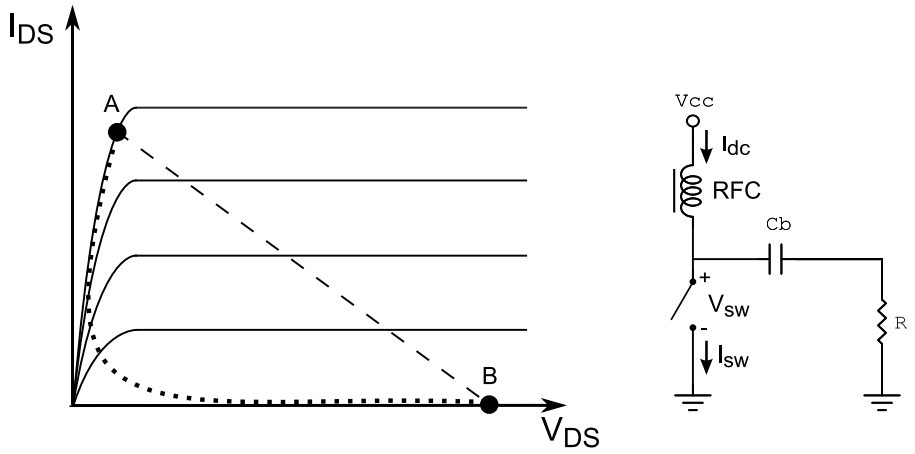


Figure 2.13: Switched amplifier principle

waveforms[10]. In the literatur some categorizations such as class *F1*, *F2* and *F3* are also encontered in order to designate the number of harmonics taken into account [40]. For instance, in the class-F2 amplifier a quarter-wavelenght transmission line is used together with a parallel-tuned output circuit to produce the equivalent of an infine number of harmonics [7, 31].

In addition to the analysis presented here, some authors have determined optimum Fourier coefficients for the case of a finite number of harmonics, as for instance in [41, 42]. Studies on loading networks for class-F amplifier are reported in [43, 44], whereas several design examples can be found in [45, 27].

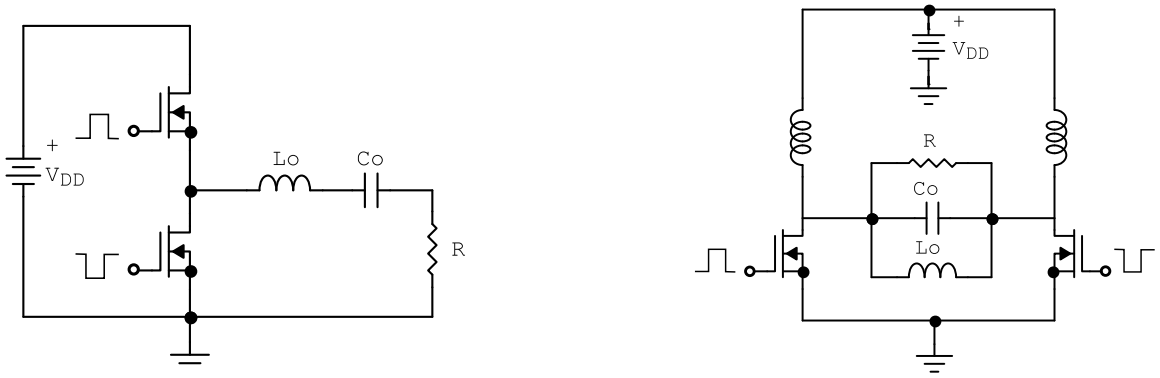
2.2.3 Switched-Mode Power Amplifiers

A switched-mode amplifier is an amplifier in which the transistor operates at either of two operating points, designated with A and B in figure 2.13. The transistor is assumed to behave as an ideal switch, in which the transitions between points A and B occur instantaneously. The concept of using transistors as switches in amplifiers is not new as evidenced by the papers of Milnes from 1956 [46] and from Ettinger and Cooper from 1959 [47]. In the first of them, the author stated that power dissipation in the transistor, causing temperature rise, is the main factor limiting the output power of the device. Therefore, if the transition between A and B occurs rapidly the heat dissipation is reduced considerably[11], and for instance a device reported as delivering $10\,W$ in class B would deliver $40\,W$ operating as a switch [46]. Since the devices are capable of handling more output power and the dissipation is reduced, higher efficiency is obtained achieving levels above 90% at very low frequencies [47].

An idealized switching amplifier is depicted in figure 2.13, in which a switch is terminated with R through a coupling capacitor C_b. The current and voltage waveform of this amplifier

[10] An amplifier exhibiting a half-wave rectified drain voltage and a square-shaped drain current is termed *inverse class-F*

[11] A transition from A to B following the dotted line in figure 2.13 is highly desiderable to reduce power dissipation and increase efficiency



(a) voltage-switching (b) current-switching

Figure 2.14: Class-D amplifier circuits

are non-overlapping squared waves, and consequently dissipating zero power. Nevertheless, as it was mentioned at the end of section 2.2.1, only power at the fundamental is desidred and therefore this ideal switch amplifier would show an efficiency just close to 81% [32]. More practical concepts have been indeed developed and some of the most known family of switched-mode amplifiers are the class-D[12] and class-E amplifiers. Figure 2.14 depicts two subclasses of the class-D power amplifier, namely the voltage mode (VM) and current mode (CM) (additional topologies of the class-D are described in [49, 45, 40]).

The class-D amplifier is characterized by the use of two transistors driven differentially, thus switching ON and OFF in an alternate way. The CM class-D operation (figure 2.14b) can be easily understood by imaging the drain voltages to be out-of-phase (push-pull operation) and so do the odd coefficients in their Fourier decomposition

$$V_{ds1}(\theta) = V_0 + V_1 \cdot sin(\theta) + V_2 \cdot sin(2\theta) + V_3 \cdot sin(3\theta) + ... \quad (2.38)$$

$$V_{ds2}(\theta) = V_0 \boldsymbol{-V_1 \cdot sin(\theta)} + V_2 \cdot sin(2\theta) \boldsymbol{-V_3 \cdot sin(3\theta)} + ... \quad (2.39)$$

By even and odd-mode analysis [50] and by taking into account the symmetry of the circuit, it can be seen that the resulting drain-source voltages only contain even harmonics, whereas the drain currents contain only odd harmonics (in addition to DC and fundamental components). Therefore it is expected V_{ds} to be a half sinuoidal signal and I_{ds} to be square shaped. In this respect, the CM class-D is a push-pull version of an inverse class-F amplifier. The VM class-D could be thought of an inverse version of the CM in terms of the waveforms at the device terminals, displaying a half-sinusoidal drain current and a squared-shaped drain voltage as in the case of the class-F amplifier (optimum efficiency class-B) [31].

The class-E power amplifier is the other high-efficiency concept belonging to the switch-mode family, having output waveforms that do not resemble those introduced so far. This single-ende amplifier will be the topic of the subsequent chapters and therfore will not be presented here.

[12] Invented around 1959 by Baxandall [48]

3 State of the Art on Class-E Power Amplifiers

As stated in chapter 2, the class-E power amplifier represents one of the high-efficiency approaches belonging to the switching-mode family.

The development of this alternative concept seems to have started with the work of Ewing back to 1964 [51]. In his manuscript he describes a *very efficient* class-C amplifier operating as a high-speed switch that is able to achieve higher efficiencies compared to the conventional class-C amplifier. On the other hand, it was Sokal and Sokal who about ten years later coined the term class-E to refer to this new tuned single-ended amplifier topology [52]. From then on, the class-E amplifier has found widespread application due to its design simplicity and high operation efficiency.

In this chapter the fundamentals of this amplifier class will be reviewed, starting with the class-E time-domain analysis and presenting design equations for those amplifier circuits. In addition to this, the power loss mechanisms and frequency limitation in class-E are discussed. Finally, the design of class E at higher frequencies is addressed by using existing frequency-domain techniques.

3.1 Low-Frequency Analysis of Class-E Power Amplifiers

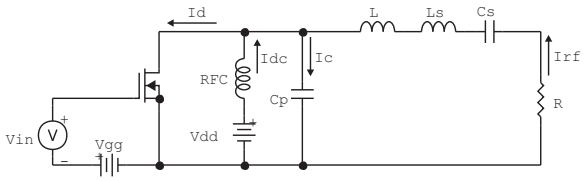
Ewing discovered that very high efficiencies are obtained with a series resonant R, L, C circuit connected about the transistor as shown in figure 3.1 [51].[1]

The analysis of this circuit starts with the introduction of the following assumptions [45]:

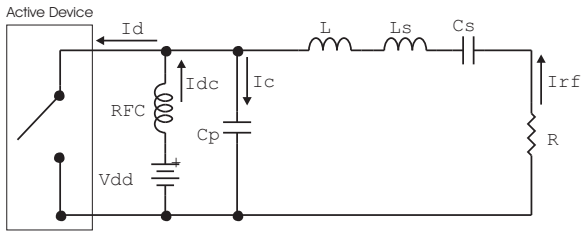
- the transistor has zero saturation voltage, zero saturation resistance, infinite off resistance and its switching action is instantaneous and lossless.
- the total shunt capacitance is independent of the collector/drain voltage and is assumed to be linear.
- the loaded quality factor Q_L of the series resonant circuit $L_s - C_s$ tuned to the fundamental frequency is high enough for the output current to be sinusoidal.
- the only resistive element in the circuit is the load R.
- A duty cycle of 50 % ($D = 0.5$) is used.[2]

[1] In Ewing's manuscript the inductor L in series with L_s is not shown. However, he indicated that the series resonant circuit must appear inductive at the operating frequency, which requires an adjustment in the inductor or capacitor's value.

[2] This value is close to $D = 0.511$, the value for maximum output power [53]



(a) Basic class-E topology



(b) Active device as a switch

Figure 3.1: General class-E amplifier topology

In addition to these assumptions, two additional conditions need to be satisfied by the voltage $v(\omega t)$ across the switch in order to obtain lossless operation. Those conditions are referred to as *zero-voltage switching (ZVS)* and *zero-voltage derivative switching (ZVD)*[3] and are given by equation 3.1 and 3.2 respectively [49].

$$v(\omega t)\big|_{\omega t=2\pi} = 0 \tag{3.1}$$

$$\left.\frac{dv(\omega t)}{d\omega t}\right|_{\omega t=2\pi} = 0 \tag{3.2}$$

The first of these two conditions implies that the energy stored in the shunt capacitor C_p is zero when the transistor turns on, yielding zero turn-on switching loss. Since the derivative of $v(\omega t)$ is zero at the time when the switch turns on, the switch current $i_d(\omega t)$ increases gradually from zero after the switch is closed[4]. The operation for which both conditions are satisfied simultaneously is called the *nominal operation* or *optimum operation* [49].

In addition to the topology shown in figure 3.1, there exist circuits in which the parallel capacitor C_p is not included. One example is given in the paper by Avratoglou et al. from 1988 [54] and on the *inverse Class-E* topologies described in [55, 56]. In those approaches the switch current and voltage waveforms are interchanged, whereas optimum operation is characterized by the fulfilling of the *zero-current switching (ZCS)* and *zero-current derivative (ZCD)* conditions [57]. These alternative class-E topologies will not be considered here since they do not allow the inclusion of the transistor parasitic output capacitor into the circuit, a factor of prime importance when working with this amplifier class.

[3] Mostly referred to as *zero derivative switching (ZDS)*

[4] For the case in which this second condition is satisfied, the operation is called *soft-switching*

3.1.1 Shunt Capacitor Class-E Analysis

In the following analysis[5], the assumptions made above regarding the ideal behavior of the switch and of the circuit are to be used. Furthermore, the RF choke is represented by a infinite-valued inductor having zero resistance and which allows the flow of a constant dc current.

The current through the active device, being assumed to act as a switch, is given by the contributions of the dc current, the parallel capacitance current and the load current as follows

$$i_d(\omega t) = I_{dc} - i_C(\omega t) + i_{RF}(\omega t) \tag{3.3}$$

Since the loaded quality factor Q_L is high enough, the current flowing through the load $i_{RF}(\omega t)$ is sinusoidal and given by

$$i_{RF}(\omega t) = I_R \cdot sin(\omega t + \varphi) \tag{3.4}$$

where I_R is the peak value of the load current and φ is the phase angle between the base or gate excitation current and $i_{RF}(\omega t)$.

When the switch is ON for $0 \leq \omega t < \pi$ the current through the capacitance is zero, i.e.

$$i_C(\omega t) = \omega C_p \frac{dv(\omega t)}{d\omega t} = 0 \tag{3.5}$$

therefore equation 3.3 becomes

$$i_d(\omega t) = I_{dc} + I_R \cdot sin(\omega t + \varphi) \tag{3.6}$$

The initial condition for the switch current at $t = 0$ (instant of switching) requires $i_d(0^-) = i_d(0^+) = 0$ and therefore

$$I_{dc} = -I_R \cdot sin\varphi \tag{3.7}$$

Substituting 3.7 into 3.6 results in

$$\begin{aligned} i_d(\omega t) &= I_R \cdot [sin(\omega t + \varphi) - sin\varphi] \\ &= I_R \cdot [sin(\omega t)cos(\varphi) + (cos(\omega t) - 1) \cdot sin\varphi] \end{aligned} \tag{3.8}$$

When the switch is OFF for $\pi \leq \omega t < 2\pi$ the current through the switch is zero, and the current through the capacitor can be obtained from 3.3

$$\begin{aligned} i_C(\omega t) &= I_{dc} + I_R \cdot sin(\omega t + \varphi) \\ &= -I_R \left[sin\varphi + sin(\omega t + \varphi)\right] \end{aligned} \tag{3.9}$$

the voltage across the switch can be obtained by integration of the capacitor current as follows

[5] This shunt capacitor class-E analysis follows closely the one in [45]

$$\begin{aligned} v(\omega t) =& \frac{1}{\omega C_p} \int_{\pi}^{\omega t} i_C(\omega t) \cdot d\omega t \\ =& - \frac{I_R}{\omega C_p} \left[(\omega t - \pi) \cdot sin\varphi + cos(\omega t + \varphi) + cos\varphi \right] \end{aligned} \tag{3.10}$$

and using the ZVS condition from 3.1 the phase different between excitation current and load current is obtained

$$\begin{aligned} 0 =& (2\pi - \pi) \cdot sin\varphi + cos(2\pi + \varphi) + cos\varphi \\ 0 =& \pi \cdot sin\varphi + 2 \cdot cos\varphi \\ \Longrightarrow tan\varphi =& - \frac{2}{\pi} \\ \varphi =& - 32.48^{\circ} \end{aligned} \tag{3.11}$$

the switch voltage is then expressed as follows

$$v(\omega t) = \frac{I_{dc}}{\omega C_p} \left[\omega t - \frac{3\pi}{2} - \frac{\pi}{2} \cdot cos(\omega t) - sin(\omega t) \right] \tag{3.12}$$

in which the following relations have been used [45]

$$\begin{aligned} sin\varphi =& \frac{-2}{\sqrt{\pi^2 + 4}} \\ cos\varphi =& \frac{\pi}{\sqrt{\pi^2 + 4}} \end{aligned} \tag{3.13}$$

the first term in the Fourier decomposition of the switch voltage $v(\omega t)$ represents the dc component and is given by

$$V_{dc} = \frac{1}{2\pi} \int_{0}^{2\pi} v(\omega t) \cdot d\omega t = \frac{I_{dc}}{\pi \omega C_p} \tag{3.14}$$

therefore the normalized voltage across the switch is expressed as follows

$$\frac{v(\omega t)}{V_{dc}} = \begin{cases} 0 & 0 \leq \omega t < \pi \\ \pi \left[\omega t - \frac{3\pi}{2} - \frac{\pi}{2} cos(\omega t) - sin(\omega t) \right] & \pi \leq \omega t < 2\pi \end{cases} \tag{3.15}$$

whereas the current through the switch is given by

$$\frac{i_d(\omega t)}{I_{dc}} = \begin{cases} \frac{\pi}{2} \cdot sin(\omega t) - cos(\omega t) + 1 & 0 \leq \omega t < \pi \\ 0 & \pi \leq \omega t < 2\pi \end{cases} \tag{3.16}$$

The current through the capacitor C_p can be obtained by using 3.5 and the result in 3.15

$$\frac{i_c(\omega t)}{I_{dc}} = \begin{cases} 0 & 0 \leq \omega t < \pi \\ 1 + \frac{\pi}{2} \cdot sin(\omega t) - cos(\omega t) & \pi \leq \omega t < 2\pi \end{cases} \tag{3.17}$$

the load current can be obtained by replacing 3.7 and the value of φ in equation 3.4 as follows

$$i_{RF}(\omega t) = \left(\frac{-I_{dc}}{sin\varphi}\right) \cdot sin(\omega t + \varphi) \tag{3.18}$$

$$\begin{aligned} i_{RF}(\omega t) = &\left(\frac{-I_{dc}}{sin\varphi}\right) \cdot sin(\omega t + \varphi) \\ =&1.86 \cdot I_{dc} \cdot sin(\omega t + \varphi) \end{aligned} \tag{3.19}$$

Figure 3.2 shows the normalized waveforms of the general class-E topology. As can be seen here, there is no overlap of the current and voltage at the active device plane. In the ON state the switch current is the sum of the output rf current and the dc current, whereas in the OFF state the sum of these currents flows through the parallel capacitor. In addition to this, the drain (or collector) current exhibits a jump, which according to Molnar [58] needs to be tolerated if non-zero output power is to be obtained.

The non-overlaping of the drain voltage and current indicates that there is no dissipation in the transistor acting as a switch. Moreover, since the harmonics of the current and volage are in quadrature, no power dissipation occurs at the harmonic frequencies. As a cosequence, the whole dc input power is transformed into rf power at the ouput resistor, guaranteeing 100 % efficiency.

Taking into account the 100 % efficiency condition the following relation is obtained

$$I_{dc} \cdot V_{dc} = \frac{1}{2} I_R^2 \cdot R \tag{3.20}$$

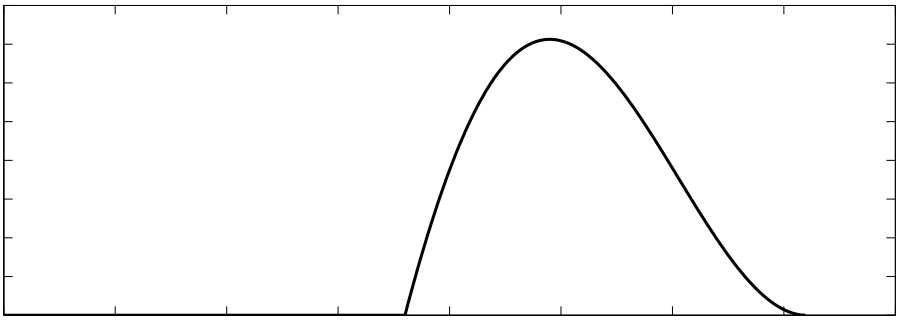
hence the dc supply current can be obtained by using 3.7 and the relations in 3.13

$$\begin{aligned} I_{dc} =&\frac{2 \cdot V_{dc} \cdot (sin\varphi)^2}{R} \\ =&\frac{8}{\pi^2 + 4} \cdot \frac{V_{dc}}{R} \\ =&0.577 \cdot \frac{V_{dc}}{R} \end{aligned} \tag{3.21}$$

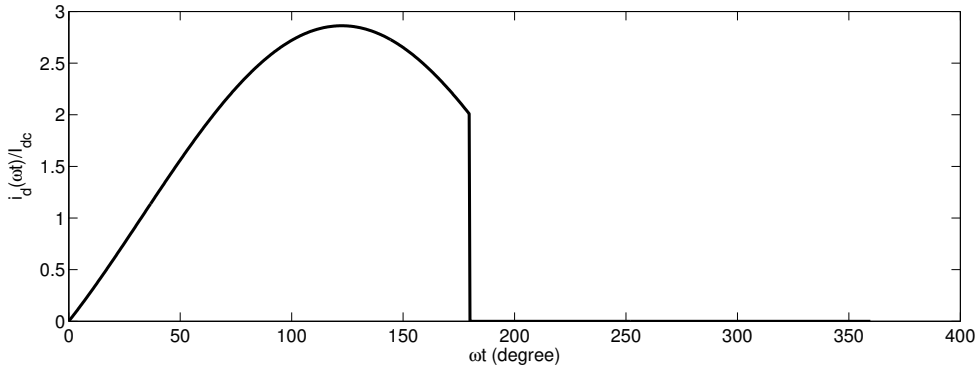
The peak values for the switch current and voltage can be determined by differentiating equations 3.16 and 3.15 with respect to ωt and equating them to zero

$$I_{peak} = \left(\frac{\sqrt{\pi^2 + 4}}{2} + 1\right) \cdot I_{dc} = 2.86 \cdot I_{dc} \tag{3.22}$$

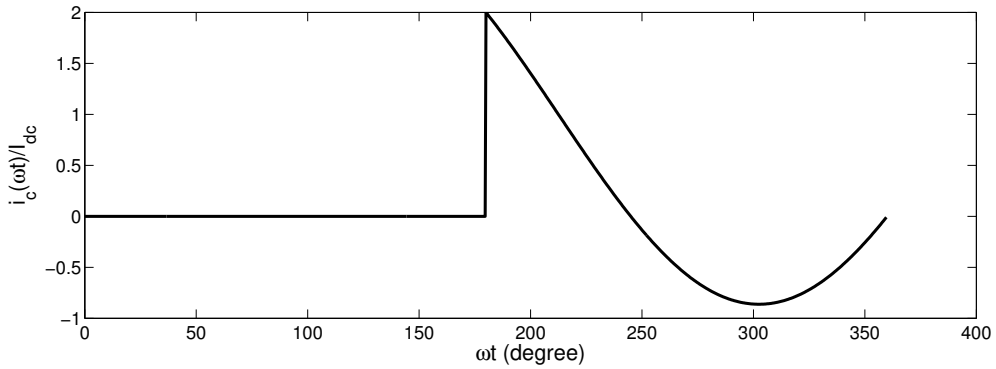
$$V_{peak} = -2\pi\varphi V_{dc} = 3.56 \cdot V_{dc} \tag{3.23}$$



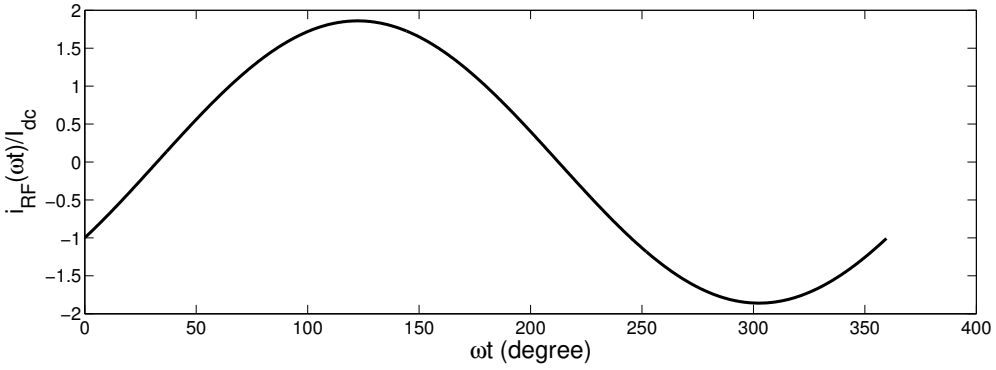
(a) voltage across switch



(b) current through switch



(c) capacitor current



(d) load current

Figure 3.2: General class-E waveforms

the amplitude of the output voltage is given by[6]

$$\begin{aligned} V_R =& - I_R \cdot R \\ =& - \frac{I_{dc}}{sin\varphi} \cdot R = 0.577 \cdot \frac{V_{dc}}{R} \cdot \frac{R}{sin\varphi} \\ =& 0.577 \cdot V_{dc} \cdot \frac{\sqrt{\pi^2+4}}{2} = 1.074 \cdot V_{dc} \end{aligned} \tag{3.24}$$

The fundamental component of the voltage across $L_s - C_s$ is zero because at resonance the reactance of this circuit is zero. The fundamental component of the voltages across resistor R and the series inductor L are

$$v_R(\omega t) = V_R \cdot sin(\omega t + \varphi) \tag{3.25}$$

$$v_L(\omega t) = -j\omega L \cdot I_R \cdot sin(\omega t + \varphi) = V_L \cdot cos(\omega t + \varphi) \tag{3.26}$$

with $V_L = -\omega L \cdot I_R$. These voltages represent an in-phase and a quadrature component that add up to give the total fundamental switch voltage as follows

$$v_{fund}(\omega t) = v_R(\omega t) + v_L(\omega t) \tag{3.27}$$

Applying Fourier decomposition over the even and odd component of this voltage results in (see [45])

$$V_R = \frac{1}{\pi} \int_0^{2\pi} v(\omega t) \cdot sin(\omega t + \varphi) \cdot d(\omega t) = -\frac{I_R \cdot sin\varphi}{\pi \omega C_p} \left[-\frac{\pi}{2} cos\varphi + 2 sin\varphi - \frac{\pi^2}{4} sin\varphi \right] \tag{3.28}$$

$$V_L = \frac{1}{\pi} \int_0^{2\pi} v(\omega t) \cdot cos(\omega t + \varphi) \cdot d(\omega t) = -\frac{I_R \cdot sin\varphi}{\pi \omega C_p} \left[2 cos\varphi - \frac{\pi^2}{4} cos\varphi + \frac{\pi}{2} sin\varphi \right] \tag{3.29}$$

where 3.14 and 3.7 have been used. With the equations above and knowing that $V_R = -I_R \cdot R$ and $V_L = -\omega L \cdot I_R$ respectively, the following is obtained

$$\omega C_p R = \frac{sin\varphi}{\pi} \left[-\frac{\pi}{2} cos\varphi + 2 sin\varphi - \frac{\pi^2}{4} sin\varphi \right] = 0.1836 \tag{3.30}$$

$$\omega C_p \omega L = \frac{sin\varphi}{\pi} \left[2 cos\varphi - \frac{\pi^2}{4} cos\varphi + \frac{\pi}{2} sin\varphi \right] = 0.2116$$

$$\Rightarrow \frac{\omega L}{R} = 1.1525 \tag{3.31}$$

and the optimum load resistance can be obtained by using 3.24

[6] Recall that the current has opposite direction (see figure 3.1)

Table 3.1: Design equations for class-E with $DC = 50\,\%$

Parameter	***Equation***
supply voltage (V_{dc}) operating frequency (ω) output power (P_{out}) quality factor (Q)	defined by designer
load resistor	$R = 0.5768 \cdot \frac{V_{dc}^2}{P_{out}}$
parallel capacitor	$C_p = \frac{0.1836}{\omega \cdot R}$
series inductor	$L = \frac{1.1525 \cdot R}{\omega}$
series resonator inductor	$L_s = \frac{Q \cdot R}{\omega} - L$
series resonator capacitor	$C_s = \frac{1}{\omega^2 \cdot L_s}$

$$R = \frac{1}{2}\frac{V_R^2}{P_{out}} = \frac{1}{2}\frac{(1.074 \cdot V_{dc})^2}{P_{out}} = 0.5768\frac{V_{dc}^2}{P_{out}} \tag{3.32}$$

The admittance seen by the switch at resonance is given by

$$\underline{Y}_{switch} = j\omega C_p + \frac{1}{R + j\omega L} = \frac{(1 - \omega^2 L C_p) + j\omega C_p R}{R + j\omega L} \tag{3.33}$$

with expression 3.33 and the results in 3.30 and 3.31, the angle of the load network seen by the switch ($1/\underline{Y}_{switch}$) as required for optimum class-E operation can be obtained as follows

$$\phi = tan^{-1}\left(\frac{\omega L}{R}\right) - tan^{-1}\left(\frac{\omega C_p R}{1 - \omega^2 L C_P}\right) = 35.945° \tag{3.34}$$

The design parameters as well as equations used to determine the component values of a basic class-E amplifier topology seen in 3.1 are summarized in table 3.1. This equations correspond to a duty cycle DC of $50\,\%$.

The analysis of the general class-E topology (for $50\,\%$ duty cycle) shown above allows to understand the basic operating principle of this amplifier concept. Several assumptions were introduced, which allowed the analysis to be more tractable. Furthermore, the two additional conditions given by equations 3.1 and 3.2 were assumed to be fulfilled for lossless operation. This optimum operation is only achieved if the relations among C_p, L, R, D and ω, as given above, are satisfied. Kazimierczuk [49] indicates that in order to achieve zero-voltage switching the operating frequency f must satisfie

$$f_{01} < f < f_{02} \tag{3.35}$$

in which the resonant frequencies f_{01} and f_{02} are given by

$$f_{01} = \frac{1}{2\pi\sqrt{(L + L_s) \cdot C_s}} \tag{3.36}$$

$$f_{02} = \frac{1}{2\pi\sqrt{(L + L_s) \cdot C_{eq}}} \tag{3.37}$$

where C_{eq} is the equivalent capacitance seen during the OFF state and is given by

$$C_{eq} = \frac{C_s \cdot C_p}{C_s + C_p} \tag{3.38}$$

Deviation from ZVS causes the device to switch without the capacitor C_p being fully discharged, resulting in turn-on switching losses.

On the other hand, the actual implementation of a class-E power amplifier requires an awareness of the obvious non-idealities causing a reduction in the efficiency of this architechture. The biggest deviation is in active device operation, for the device cannot behave as an ideal switch and therefore causes efficiency degradation [27]. Several authors have proposed ways to evaluate the losses caused by the non-idealities in class-E. Starting with Ewing [51] who considered the effect of saturation resistance in amplifier performance, Raab and Sokal [59] consider that in a properly loaded and tuned class-E amplifier, power losses are primarily caused by active device saturation voltage and resistance, nonzero switching time and lead inductance. The efficiency degradation can be determined by calculating the power dissipation in each case and applying the following relation[7]

$$\eta = \frac{P_{out}}{P_{out} + P_{diss}} \tag{3.39}$$

In table 3.2 the expression for the power dissipation P_{diss} for different loss mechanisms according to [59] is summarized

Table 3.2: Power losses in the class-E power amplifier

Mechanism	***Power Dissipation*** (P_{diss})
Saturation resistance	$1.365 \left(\frac{R_{ON}}{R}\right) P_{out}$
Transition time	$19.739 \left(\frac{t_f}{T}\right)^2 P_{out}$
Wiring inductance	$2 \cdot L_b \cdot I_{dc}^2 \cdot f$

where R_{ON} represents the saturation resistance, t_f the turn-off transistion time, T the signal period and L_b the wiring inductance between the actual collector/drain (inside the

[7] In this equation constant P_{out} is assumed. The efficiency degradation could be also expressed as $\eta = \frac{P_{out} - P_{diss}}{P_{out}}$ if constant DC power is assumed

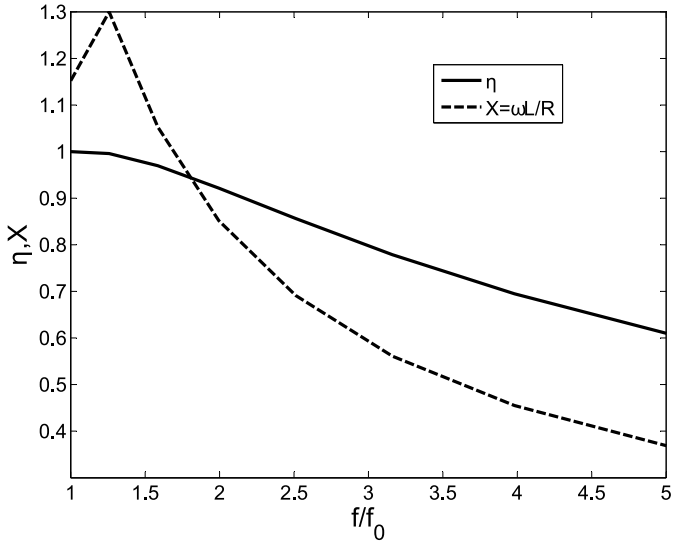


Figure 3.3: Suboptimum operation above critical frequency [8]

package) and the shunt capacitor C_p, as well as the inductance of the wiring between the emitter/source and the ground.

Kazimierczuk [60] and Blanchard et al. [61] have analyzed the effect of the drain current fall time in the efficiency of the class-E power amplifier. In [60] a linear decay of the collector current has been considered whereas in [61] an exponential decay was assumed. Those analyses indicate a relative low-efficiency degradation for a wide range of fall times. For instance, for $\omega t_f = 30°$ about 3 % points in efficiency reduction is obtained from the ideal 100 %, whereas for $\omega t_f = 60°$ the degradation is in the order of 10 % to 13 % points depending on the type of decay assumed. The efficiency degradation due to the finite current fall time is further affected by the non-infinite quality factor.

3.1.2 Frequency limitation in class-E

Several authors have referred to a maximum frequency of operation within the context of class-E amplifiers [8, 62, 63]. Raab [8] writes that in optimum class-E operation, as defined by ZVS and ZDS, the load network discharges the parallel capacitance (C_p in figure 3.1) prior to turn on of the switching device. There is however a critical frequency in which this parallel capacitance is entirely provided by the output transistor capacitance, i.e. $C_p = C_{ds}$. Below this critical frequency, in which $C_p > C_{ds}$, optimum conditions can be easily restored by using an external capacitor in parallel with C_{ds}. On the other hand, above this critical frequency, efficiency starts decreasing below the ideal 100 % as displayed in figure 3.3.

Figure 3.3 shows the theoretical maximum efficiency that can be obtained from a class-E amplifier over frequency, including the corresponding normalized value of series reactance required to keep that level of efficiency. It is worth mentioning that this efficiency degradation is solely due to the excessive output capacitive effect, i.e. efficiency degradation due to switching speed reduction and passive component losses are not considered and therefore

it is expeted that the final efficiency will be much lower than the one presented here.

The critical or maximum frequency ($f_{max,classE}$) of the shunt capacitor class-E can be obtained by using the relations derived in section 3.1.1. From equation 3.30 [8]

$$R = \frac{1}{\omega C_p} \cdot \frac{8}{\pi(\pi^2 + 4)} \tag{3.40}$$

introducing this relation into equation 3.21 yields

$$I_{dc} = \pi \omega C_p V_{dc} \tag{3.41}$$

now using the relation 3.22 for I_{peak} and replacing C_p with C_{ds} results in the expression for the maximum frequency

$$f_{max,classE} \approx \frac{I_{max}}{56.5 \cdot C_{ds} \cdot V_{dc}} \tag{3.42}$$

Note that in this case the maximum allowable peak current has been used, i.e $I_{peak} = I_{max}$, this representing a true physical limit of the device.

By using equations 3.41, 3.21 and 3.32 this expression can be alternatively written as function of the output power as follows

$$f_{max,classE} \approx 0.0507 \cdot \frac{P_{out}}{C_{ds} \cdot V_{dc}^2} \tag{3.43}$$

The expressions 3.42 and 3.43 are valid for a shunt capacitor class E with $D = 0.5$. Kazimierczuk [49] indicates that $f_{max,classE}$ increases as duty cycle D decreases as discussed in [64] and even a moderate reduction from 0.5 to 0.43 leads to a two-fold increase in $f_{max,classE}$ [65]. On the other hand, the analysis presented in [66] shows that for duty cycles below approximatelly 0.25 the efficiency starts decaying very rapidly.

In addition to this, Raab [8] has demonstrated that releasing the soft-switching condition (equation 3.2) would offer the possibility to increase the critical frequency. This regime of operation was denominated *suboptimum operation* of class-E amplifiers.

Some approaches have been deviced to overcome the limitations of the class-E amplifier topology and a overview of them will be presented in the next chapter.

3.1.3 Class-E with finite-feed inductance

In the analysis of the class-E topology in section 3.1, as well as in the common approaches encontered in the literature [52, 67], it was assumed that the choke inductance is infinite in value. On the other hand, Zulinski et al. [68] demonstrated that class-E operation is still maintained even after replacing the RF choke by a smaller inductive reactance. As a matter of fact, the elimination of this non-practicable condition adds a new degree of freedom in the class-E scenario, offering certain advantages that will be discussed in subsequent sections.

The general topology of a class-E power amplifier having a finite-feed inductor is depicted in figure 3.4. The series output resonator $L_0 - C_0$ is again tuned to the fundamental frequency, and the series reactance jX performes the phase shift required to terminate the transistor drain side with an inductive reactance at the fundamental frequency.

[8] The expression $\frac{8}{\pi(\pi^2+4)} \approx 0.1836$ is obtained by subsituting the relations in 3.13 into equation 3.30

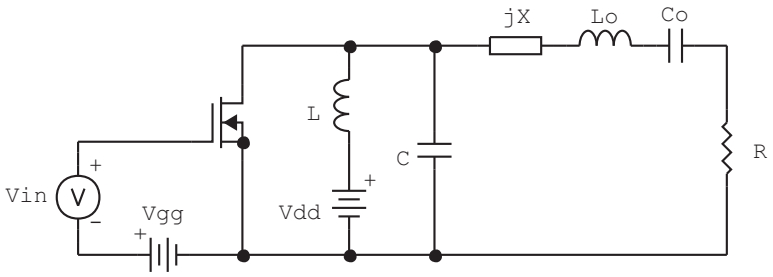


Figure 3.4: Class-E power amplifier with finite feed.

Instead of showing the whole time-domain analysis required to determine the component values and the respective waveforms, only the most important steps and outcomes of this analysis are described here. According to the flow chart in figure 3.5, the switch is considered to be in the ON state (closed) for $0 \leq \theta < \pi$ and in the OFF state (open) for $\pi \leq \theta < 2\pi$, with $\theta = \omega \cdot t$. The currrent through the switch is the sum of the load current and feed inductor current for the ON state, whereas the shunt capacitor current is zero (equations *i* and *ii* in chart). The voltage across the switch is obtained by using the shunt capacitor current (equation *iv*) and by taking into account the initial ON state conditions. As a result, a second order differential equation is obtained, the solution of which is of the form[45]:

$$\frac{V_{switch}(\theta)}{V_{DD}} = C_1 \cdot cos(q \cdot \theta) + C_2 \cdot sin(q \cdot \theta) + 1 - \frac{q^2 p}{q^2 - 1} cos(\theta + \varphi) \tag{3.44}$$

in which the following parameters have been introduced

$$q = \frac{1}{\omega\sqrt{L \cdot C}} \tag{3.45}$$

$$p = \frac{\omega L I_R}{V_{DD}} \tag{3.46}$$

The parameter q represents the normalized parallel resonant frequency of the $L - C$ branch, i.e. $q = \omega_p/\omega_0$. Using equation 3.44 (equation *vi* in flow chart) and the initial OFF state conditions, it is possible to represent the coefficients C_1 and C_2 as a function of p, q and of the the phase angle φ between the gate excitation current and the load current [45]. Now the circuit components can be calculated as function of these three variables. In the last step, the conditions for optimum operation, namely, ZVS and ZDS, can be applied to equation 3.44 resulting in equations *xii* and *xiii* in the chart. From these two equations, values for p and φ can be obtained as a function of q. The expressions for the coefficients A_i and B_i as a function of q can be found in Appendix B.

Consequently, different subsets or members of the class-E family, having different component values and waveforms, are obtained depending on the values taken by the normalized parallel resonance frequency q.

Figures 3.6 to 3.8 show the normalized current ($\tilde{I}_{switch} = i_{switch}(\theta)/I_{DD}$) and normalized voltage ($\tilde{V}_{switch} = V_{switch}(\theta)/V_{DD}$) at the switch plane for three different values of the parameter q, namely, $q = 0.5, 1.412, 2$. Those class-E subsets are designated in the literature as *subharmonic*, *parallel-circuit* and *even-harmonic* class-E amplifiers [69, 70, 45].

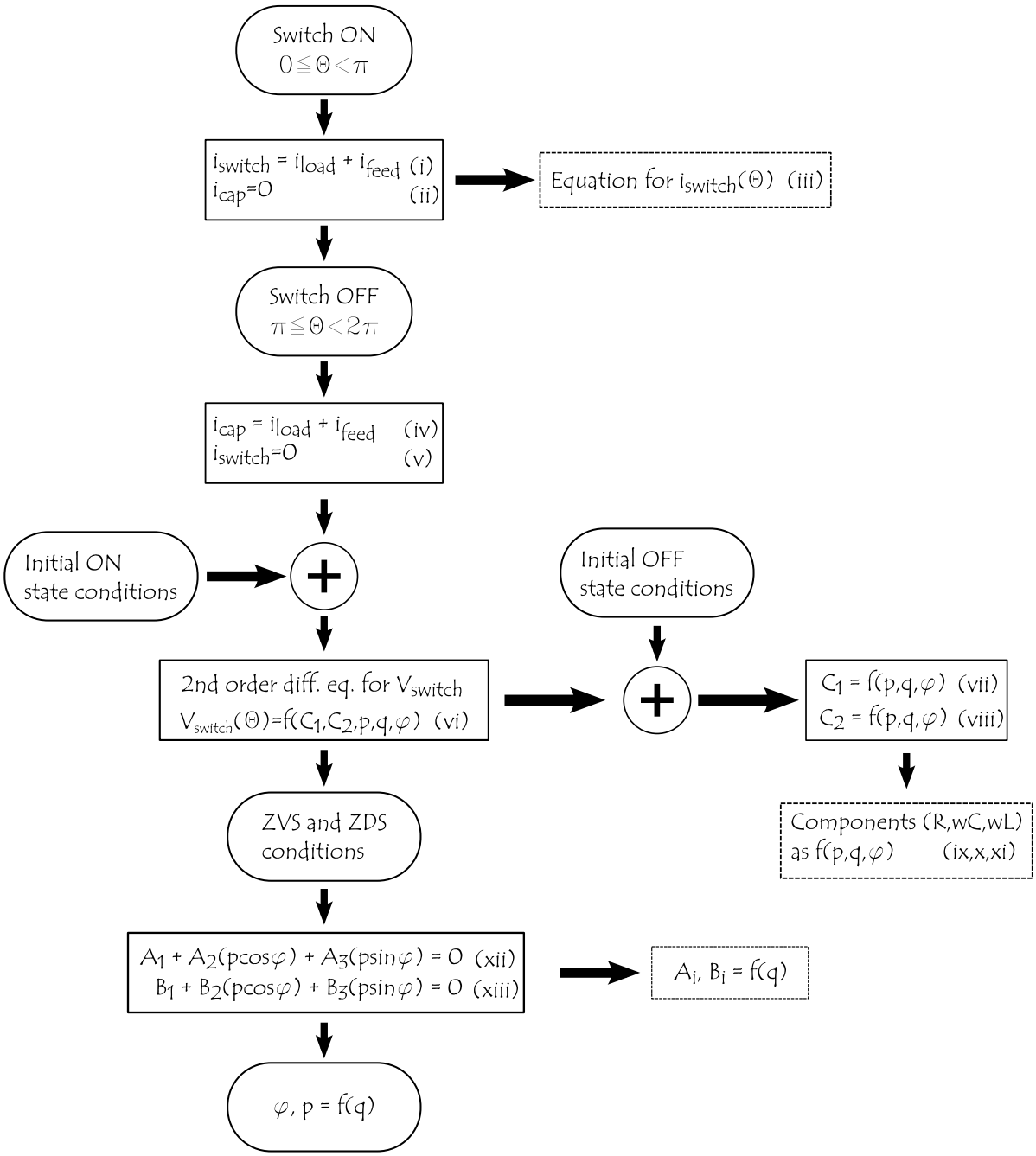


Figure 3.5: Flow diagram for analysis of finite-feed class E

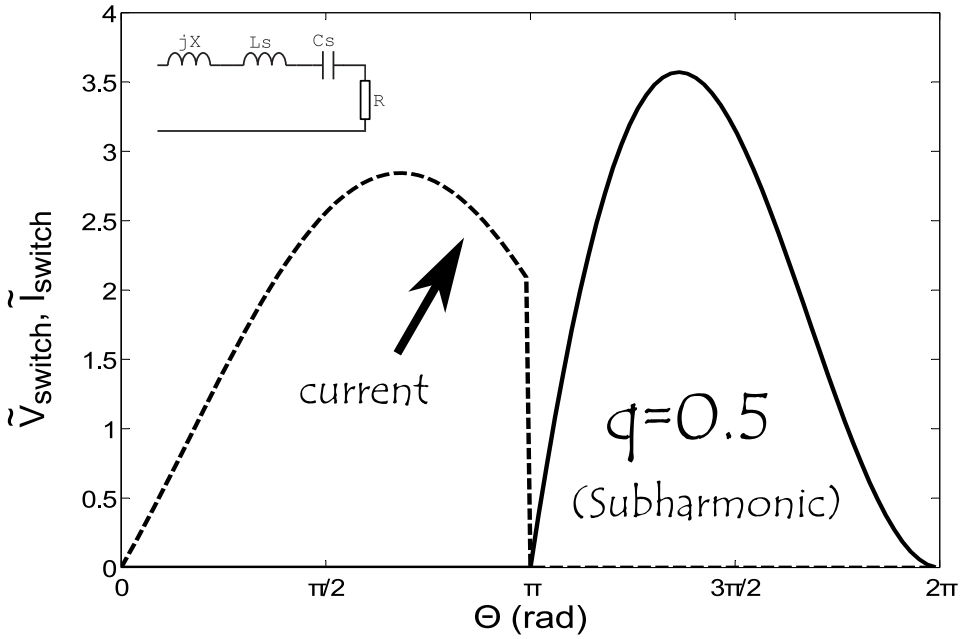


Figure 3.6: Class E amplifier for $q = 0.5$

The corresponding output network seen in each case by the parallel $L - C$ branch is also presented.

These topologies exhibit larger critical frequency ($f_{max.classE}$) and as it will be shown later can be used as the starting to point to derive enhanced class-E amplifier schemes.

3.2 High-Frequency Analysis of Class-E Power Amplifiers

The time-domain analysis presented in section 3.1.1 allows deducing the current and voltage waveforms as well as the component values of any class-E topology, like those presented in section 3.1.3. Nevertheless, most of the existing power amplifier concepts, including the high-efficiency approaches presented in chapter 2, have been analyzed in the frequency domain. For this reason and in order to obtain a better insight into class-E operation, it is equally important to resort to frequency-domain techniques.

While this is true that the frequency-domain analysis described in this section is based merely on Fourier decomposition, two main approaches for implementing the class-E concept can be identified and they have been designated here as *harmonic suppression approach* and *multiharmonic load network synthesis*.

3.2.1 Harmonic Suppresion Network Approach

In analyzing the class-E topology, Mader [9] assumes the capacitance for optimum operation to be equal to the output capacitance of the device. He applies Fourier decomposition to obtain the fundamental component of the voltage across the switch as given in [67] and with

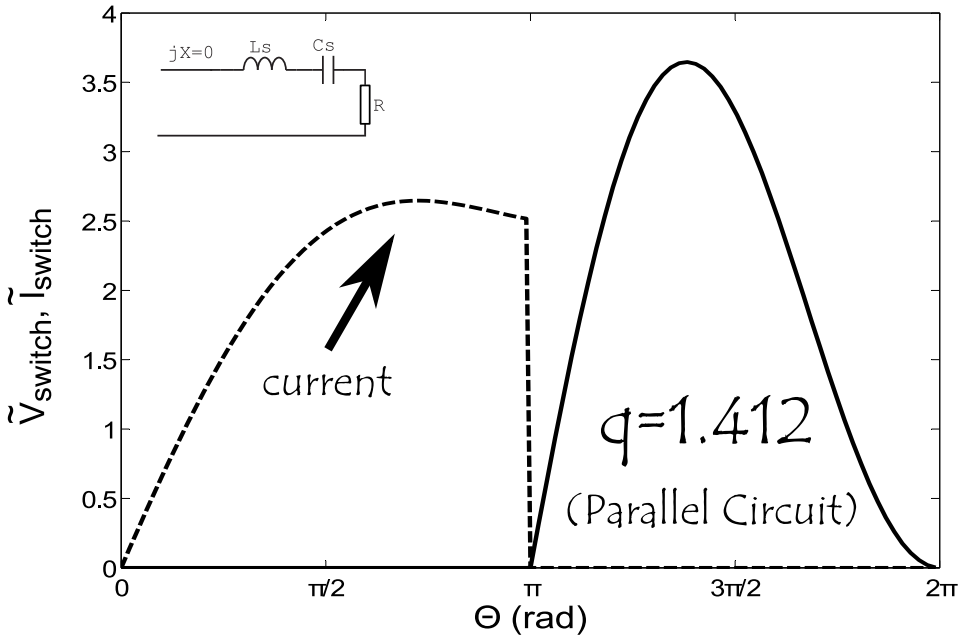


Figure 3.7: Class E amplifier for $q = 1.412$

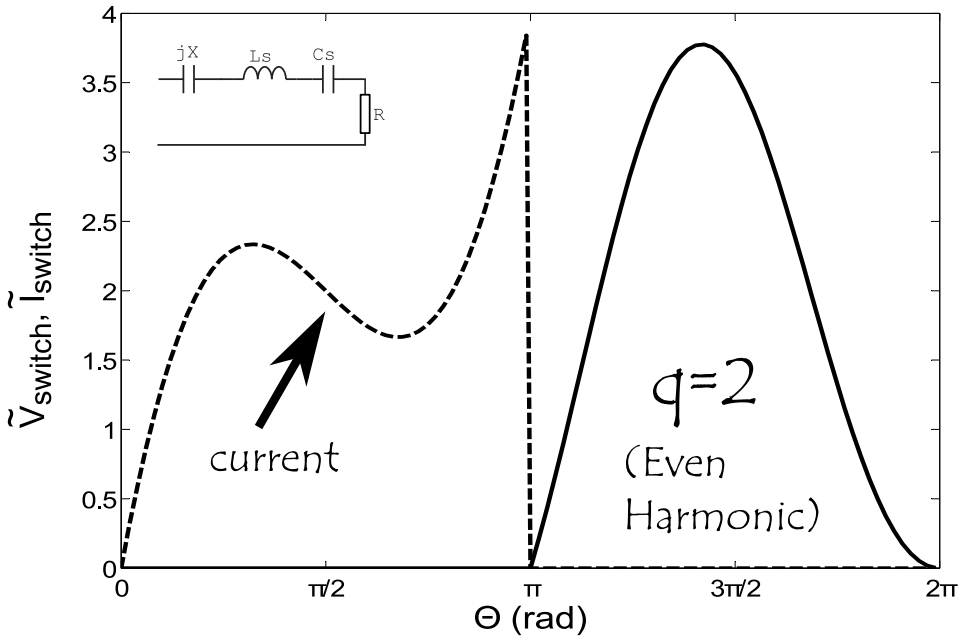


Figure 3.8: Class E amplifier for $q = 2$

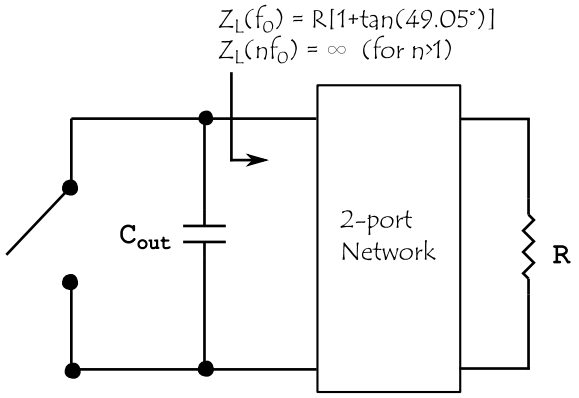


Figure 3.9: Class-E approach according to Mader [9]

this the impedance seen by the switch-C_p combination is obtained. Mader's expression can be easily derived by using the relations for $v_R(\omega t)$ and $v_L(\omega t)$ given by equations 3.28 and 3.29, and by taking into account the value of φ as well as the relation $I_R = -I_{dc}/sin\varphi$ as follows:

$$\begin{aligned} v_{fund}(\omega t) &= v_R(\omega t) + v_L(\omega t) && (3.47)\\ &= \frac{-I_R}{\omega C_p}\left[0.1836 \cdot sin(\omega t + \varphi) + 0.2116 \cdot cos(\omega t + \varphi)\right] && (3.48)\\ &= \frac{I_{dc}}{\omega C_p sin\varphi}\left[0.1836 + j \cdot 0.2116\right] \cdot sin(\omega t + \varphi) && (3.49) \end{aligned}$$

and using the fundamental value of load current from equation 3.19

$$i_{fund}(\omega t) = \frac{I_{dc}}{sin\varphi} \cdot sin(\omega t + \varphi) \qquad (3.50)$$

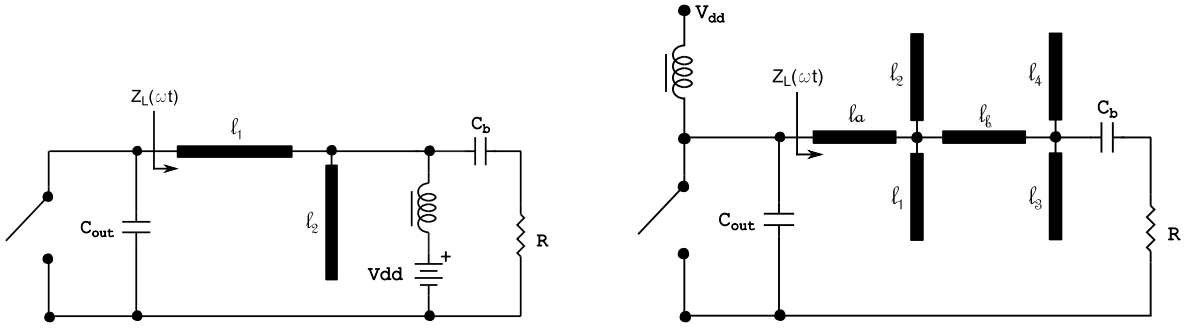
yields

$$\begin{aligned} Z_{fund}(\omega t) &= \frac{0.2801}{\omega C_p} \cdot e^{j49.05°} = \frac{0.1836}{\omega C_p} \cdot [1 + j \cdot tan(49.05°)] && (3.51)\\ &= R \cdot [1 + j \cdot tan(49.05°)] && (3.52) \end{aligned}$$

In addition to this, Mader writes that the load network is assumed to be a near-infinite impedance at the higher harmonics. This concept is summarized in figure 3.9.[9]

Undoubtedly, this is a simple yet significant simplification of the class-E concept, for it indicates that all what need to be done is to provide this complex impedance at the fundamental frequency and a near-open circuit at the harmonics. Examples of lumped as well as transmission-line network topologies implementing these class-E conditions are given in [9]. Those network topologies are designed to suppress a certain number of harmonics, for instance up to the 2nd or 3rd. Three class-E power amplifiers with 2nd-harmonic

[9]For simplicity, the load resistor R_{load} in this figure is designated as R, but this is not strictly required



(a) 2nd-harmonic suppression (b) 5th-harmonic suppression

Figure 3.10: Class-E circuits with a) $2nd$ and b) multiple harmonic suppression from [10] and [11]

suppression were presented in [10] using the circuit in figure 3.10a. The transmission lines ℓ_1 and ℓ_2 having an electrical length close to 45°, not only provide fundamental impedance matching according to equation 3.52 but also present a high impedance to the switched capacitor at the $2nd$ harmonic. Several authors have followed this approach to design class E amplifiers, using transmission line stubs for harmonic suppression up to the fifth harmonic [11, 71]. For instance, the circuit in figure 3.10b uses four transmission line stubs (ℓ_1 to ℓ_4), with an electrical length of 90° at $2f_0$, $3f_0$, $4f_0$ and $5f_0$ respectively, to suppress a high number of harmonics[10]. In addition to this, a design-oriented analysis of microwave class-E amplifiers using multiharmonic transmission-line load networks can be found in [72]. In this analysis different networks are compared in terms of harmonic suppression and their effects in output power and efficiency.

3.2.2 Mutiharmonic Load Network Synthesis

The harmonic suppression approach arose from a frequency-domain analysis in which only the fundamental components of the switch voltage and current were taken into account. As an extension to this, it is possible to perform the Fourier decomponsition to determine higher order terms. Although Sokal and Raab [73] had already calculated the harmonic structure of the switch voltage in 1977, it was not until 2001 when Raab [74] performed a broader analysis including the harmonic content of the switch current and determinig the harmonic impedances seen by the active device in class-E operation.

The relations 3.15 and 3.16 for the normalized voltage and current respectively (see section 3.1.1) can be re-writen as follows

$$\frac{V(\omega t)}{V_{dc}} = 1 + \sum_{k=1}^{\infty} [a_{vk} \cdot cos(k\omega t) + b_{vk} \cdot sin(k\omega t)] \tag{3.53}$$

$$\frac{I(\omega t)}{I_{dc}} = 1 + \sum_{k=1}^{\infty} [a_{ik} \cdot cos(k\omega t) + b_{ik} \cdot sin(k\omega t)] \tag{3.54}$$

[10]For example, the first stub (ℓ_1) not only suppresses $2f_0$ but also $6f_0$ and $10f_0$. See [11] for more details

Table 3.3: Fourier coefficients of switch voltage and current

	Switch Voltage		***Switch Current***	
k	a_{vk}	b_{vk}	a_{ik}	b_{ik}
1	-0.4674	$-\pi/2$	$-1/2$	1.4220
2	$-2/3$	$\pi/6$	$-1/3$	$-4/(3\pi)$
3	$2/9$	0	0	$2/(3\pi)$

where the a and b coefficients are calculted using following relations

$$a_{(v\,or\,i)k} = \frac{1}{\pi}\int_0^{2\pi} (V\,or\,I)\cdot cos(k\omega t)\cdot d(\omega t) \tag{3.55}$$

$$b_{(v\,or\,i)k} = \frac{1}{\pi}\int_0^{2\pi} (V\,or\,I)\cdot sin(k\omega t)\cdot d(\omega t) \tag{3.56}$$

The first three harmonics are presented in table 3.3. These coefficients can be used to obtain a reasonable approximation to the classical class-E waveforms as depicted in figure 3.11.

As a consequence, the input impedance seen from the switch reference plane at the fundamental and harmonic frequencies, can be calculated as the relation of the normalized complex voltage $V_k = a_{vk} - j\cdot b_{vk}$[11] and current $-I_k = -a_{ik} + j\cdot b_{ik}$[12] resulting in the following equations

$$Z(f_0) = 1.0872\cdot\left(\frac{V_{dc}}{I_{dc}}\right)\cdot e^{j35.94^\circ} \tag{3.57}$$

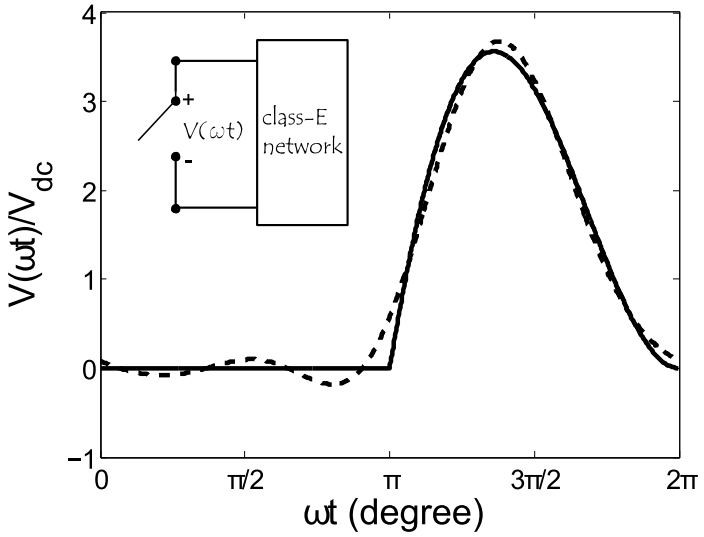
$$Z(n\cdot f_0) = -j\cdot\left(\frac{\pi}{n}\right)\cdot\left(\frac{V_{dc}}{I_{dc}}\right) \tag{3.58}$$

An example of the application of this approach to the design of class-E power amplifiers is given by Ortega-Gonzalez [75]. In his design, he uses a $3rd$ order band-pass network to synthesize the load impedances according to equations 3.57 and 3.58, achieving in this way a maximum efficiency close to 80% at an operating frequency of $115\,MHz$ with $P_{out} = 15\,W$.

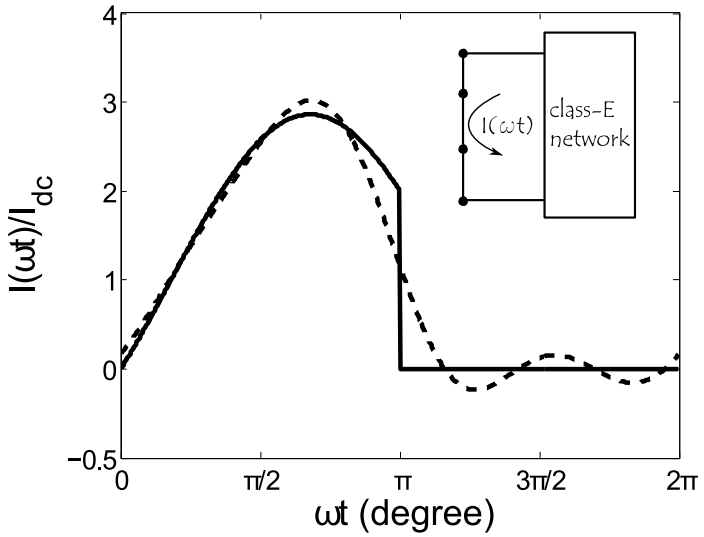
Beltran [76] uses the cascade of three networks, namely, fundamental-frequency matching network, broadband harmonic trap and a dipole network to present the harmonic impedances according to equation 3.58 up to the $10th$ harmonic. Although the impedances synthesized by this load network only provides the theoretical values for the fundamental and $2nd$ harmonic, with deviation larger than 45% for the rest of the harmonics, a peak drain efficiency of 85% at $400\,MHz$ with an output power of $10\,W$ is achieved. Beltran uses the term $Class - E_{2,3,n}$ to designate the number of harmonics used to approach true class-E operation, i.e $class - E_\infty$.

[11] This is the phasor representation and since $sin\theta = cos(\theta - \pi/2)$ the b coefficients are multiplied by $e^{-j\pi/2} = -j$

[12] Since the load current flows towards the class-E network a minus sign is added to the switch current



(a) Vswitch



(b) Iswitch

Figure 3.11: Switch voltage a) and current b) waveforms truncated up to $3rd$ harmonic

4 Aim of the Dissertation Thesis

The doctoral thesis focuses on highly efficiency power amplifiers, specifically class-E power amplifiers to be used in industrial and medical applications. Following aspects are to be covered within the context of the present work:

1. Theoretical analysis of Class-E amplifiers
   a) Analysis of class-E power amplifiers using switch as well as large-signal transistor models
   b) Evaluation via theory and simulation to understand factors limiting efficiency in this kind of amplifier
2. Efficiency improvement in class-E amplifiers
   a) Developing of new topologies/circuits to mitigate theirs limitations
   b) Class-E in-depth study suitable for microwaves
   c) Developing of new design approaches and experimental verification
3. Investigation of class-E amplifier for medical/industrial applications
   a) Evaluation and analysis of class-E power amplifiers in Hyperthermia (or Ablation) applications
   b) Investigating of different amplifier concepts (e.g. Doherty amplifiers) together with the class-E concept
   c) Developing of proof-of-concept or demonstrators within a medical/industrial scenario

4.1 Outline

The core of this thesis is organized as follows:

Chapter 5 starts by reviewing the frequency limitation in class-E power amplifiers. The characteristic polynomial equations for the class-E topology are used to demonstrate the problem posed by the transistor output capacitance. A simplified analysis in the frequency domain is presented to determine the value of the inductor required to compensate excess output capacitance. Here it is shown that this inductor is frequency dependent. In this chapter a parameter called *excess factor* (α) is introduced, as a way to quantify the amount of excessive output capacitance. Expressions for the driving point impedance seen from the transistor plane as function of α are derived and shown here. Two new class-E topologies are introduced in this chapter. They result from replacing the finite-feed inductor in the conventional class-E topology by the frequency-dependent inductor derived in this chapter.

Finally, the simulation and measurement results of a 7.8 W amplifier demonstrator operating at 434 MHz are presented.

Chapter 6 addresses the topic of inductive compensation at microwaves. The term FDIC-class-E PA is introduced here to refer to a class-E amplifier having a frequency-dependent excess capacitance compensation mechanism. In this chapter the concept of FDIC is reviewed and examples shown of how this concept has been adopted and extended by other authors. As a novel element, the FDIC mechanism is evaluated in this chapter by employing a simplified large-signal model. The chapter shows how to extract the simplified model from an existing commercial model and its implementation in the simulation environment. The extracted model can be fully controlled, i.e., its parameters can be modified and sections of it de-activated if required. Extensive simulations are shown here to evaluate operation below and above the class-E maximum frequency of operation. Results of the conventional vs. the FDIC-class-E are presented. The chapter also introduces design equations for a generalized class-E output matching network, which can be used in the design of the FDIC-class-E amplifier. Finally, the simulation and measurement results of a 10 W amplifier demonstrator operating at 1.96 GHz are presented.

Chapter 7 discusses power amplifiers for hyperthermia systems. The chapter starts with an overview of radio frequency hyperthermia and discusses the requirements of power amplifiers used in hyperthermia systems. For this purpose, a short list of available commercial systems is also shown. The design of a first demonstrator for regional hyperthermia at 70 MHz requiring 100 W is shown. In this section, system design considerations are discussed. Measurement results of the built driver and power amplifier are presented. Following this, the design of a 250 W amplifier for the same frequency is introduced. Two approaches for designing the amplifier are reviewed (class-E vs. load-pull) and evaluated via simulations. The large-signal model for the LDMOS device is used to generate drain voltage and current waveforms for both approaches, which help to guide the design process. Different aspects of the design process are discussed and the measurement results of the power amplifier demonstrator are shown. Finally, the carried out RF heating experiments using an agar phantom are presented.

Chapter 8 concludes the thesis with a summary of the most important achievements and suggests further research directions.

5 New Topologies of Class-E Power Amplifiers

In this section an alternative approach is presented that allows to extend the frequency operation of class-E power amplifiers by using a so-called frequency-dependent inductive compensation (FDIC)[1]. As already introduced in chapter 3 section 3.1.3, the analysis of the class-E power amplifier employing a finite inductor (instead of an ideal RF choke) reveals that the maximum frequency of operation can be increased due to the compensation effect that causes excess capacitance mitigation.

5.1 Class-E with finite DC feed Inductance

5.1.1 Simplified Analysis

The basic circuit topology of a general-circuit class-E power amplifier with finite-feed inductance presented in section 3.1.3 is reproduced once again in fig. 5.1. This circuit is usually analyzed by introducing preliminary assumptions: the transistor is considered an ideal switch that is operating in an off-state and an on-state mode. The transistor has zero saturation voltage and zero on-resistance, infinite off-resistance and its switching action is instantaneous. The output capacitance is linear and the loaded quality factor of the series resonant L_0C_0 circuit tuned to the fundamental frequency is high enough for the output current to be sinusoidal [45]. By taking into account these assumptions and the optimum conditions for soft-switching, i.e zero-voltage switching (ZVS) and zero-derivative switching (ZDS), a set of equations can be obtained to solve for the component values of the circuit topology in fig. 5.1. As described in [45] the component values are function of three main parameters, namely: q, p and of the initial phase shift φ of the sinusoidal current through the load. These parameters have been introduced in section 3.1.3 and are shown again in equations (5.1) and (5.2).

$$q = \frac{1}{\omega_0 \sqrt{L \cdot C}} \tag{5.1}$$

$$p = \frac{\omega_0 L I_R}{V_{dd}} \tag{5.2}$$

Here ω_0 represents the operating angular frequency, V_{dd} the supply drain voltage and I_R the amplitude of the load current. Commonly, the parameter q is considered as a variable and p and φ are expressed as a function of it. Thus, it is possible to evaluate the components

[1] The FDIC technique presented in this section has been published in the *IEEE Transactions on Microwave Theory and Techniques* [77]

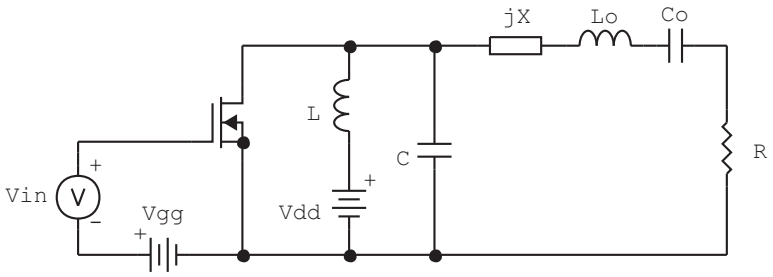


Figure 5.1: General circuit of class-E power amplifier.

of the circuit in fig. 5.1 by selecting different values of the variable q. As a matter of fact, a set of simplified equations can be found representing the variation of the circuit parameters as a function of q. In [78] and [79] the polynomial form of these equations were obtained by fitting the responses over q. For the purpose of analyzing the general class-E circuit, the set of equations corresponding to $1 < q < 1.65$ are re-written below in equations (5.3) through (5.6) [2]. These equations will be used to demonstrate the problem encountered when dealing with high values of the output capacitance.

$$K_L(q) = 8.085q^2 - 24.530q + 19.230 = \frac{\omega_0 L}{R} \tag{5.3}$$

$$K_C(q) = -6.970q^3 + 25.930q^2 - 31.071q + 12.480 = \omega_0 CR \tag{5.4}$$

$$K_P(q) = -11.900q^3 + 42.753q^2 - 49.630q + 19.700 = \frac{P_0 R}{V_{dd}^2} \tag{5.5}$$

$$K_X(q) = -2.900q^3 + 8.800q^2 - 10.200q + 5.020 = \frac{X}{R} \tag{5.6}$$

When realizing idealized optimum class-E operation mode, it is useful to define the maximum frequency up to which such an efficient operation mode can be achieved [45]. This maximum frequency of operation can be defined in terms of the output capacitance, drain supply voltage and output power in the following way. From (5.4):

$$R = \frac{K_C(q)}{\omega_0 C} \tag{5.7}$$

substituting (5.7) in equation (5.5)

$$K_P(q) = \frac{P_0}{V_{dd}^2} \frac{K_C(q)}{\omega_0 C} \tag{5.8}$$

the maximum frequency for nominal class-E operation can be now defined by replacing C by C_{OUT} in (5.8)

$$F_{max} = \frac{K_C(q)}{2\pi K_P(q)} \frac{P_0}{V_{dd}^2 C_{OUT}} \tag{5.9}$$

and using the normalized output capacitance $C_{OUT}^{norm} = C_{OUT}/(P_0/V_{dd}^2)$

[2] Equations for $0.6 < q < 1.0$ and $1.65 < q < 1.9$ can be found in [79]

$$F_{max} = \frac{K_C(q)}{2\pi K_P(q)} \frac{1}{C_{OUT}^{norm}} \tag{5.10}$$

Once C_{OUT}^{norm} has been defined, the expression in (5.10) can be evaluated in order to determine optimum values for q that allow to maximize F_{max}. The range of q to be considered here cover values up to $q = 1.9$. As indicated in [78] and [79], for larger values of q ($q > 1.65$) K_C and K_P decrease considerably and approach zero at $q = 1.9$. Figure shows the maximum frequency for several values of q and C_{OUT}^{norm}. An obvious feature displayed in fig. is the increase of F_{max} for lower values of the output capacitance. The highest value of F_{max} is obtained for $q = 1.9$.

As an example, consider a device that is desired to operate in class-E mode at 434 MHz with drain supply voltage of 20 V and RF output power equal to 10 W. F_{max} is set to this frequency of operation and the plots in 5.2 are used to determine the maximum permissible C_{OUT} as well as an optimum value for q in each of the three ranges:

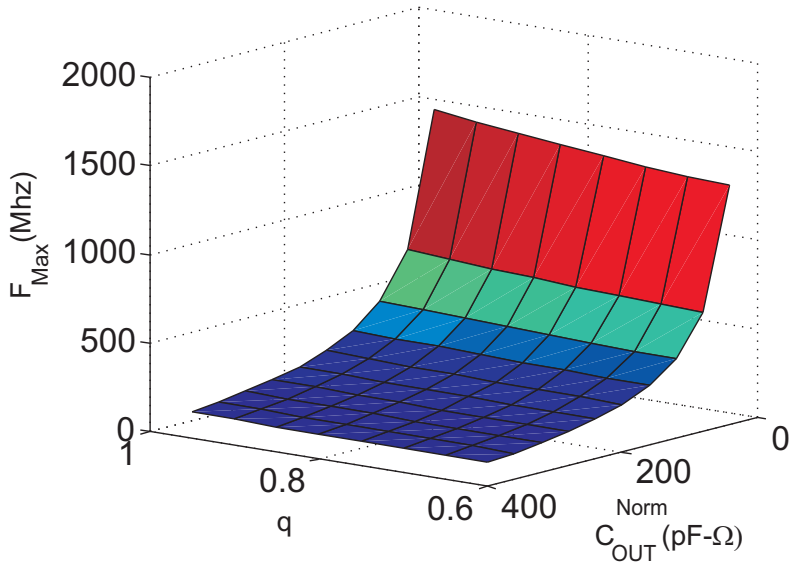
- $0.6 < q \leq 1$: a value of $F_{max} \geq 434$ MHz is obtained for all q as long as the output capacitance does not exceed 3 pF.
- $1 < q < 1.65$: in this case the capacitance should not exceed 4 pF and $q > 1.25$. Lower q values can be selected as long as $C_{OUT} < 4$ pF.
- $1.65 < q \leq 1.9$: the maximum permissible value of output capacitance is about 6 pF if $q \geq 1.68$.

It is important to mention that for lower output powers the values of permissible capacitances decrease further. Although the analysis described so far is helpful in determining the range of permissible C_{OUT} and q that can be used when designing a class-E with finite-feed inductor, it does not provide any solution for the case when C is larger than the value for nominal operation. In the next section, a solution is proposed, starting with the study of a subclass of finite-inductor class-E and its analysis in the frequency domain.

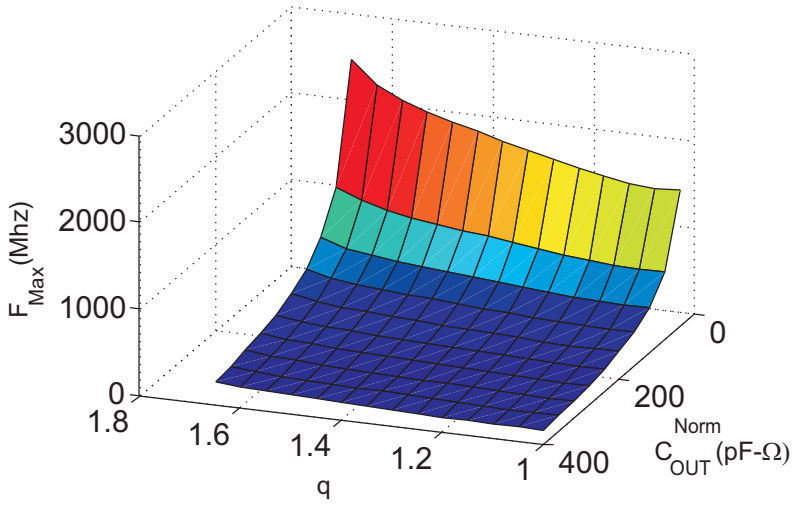
5.1.2 Frequency-Domain Analysis of Parallel-Circuit Class-E

In the following analysis, the parallel circuit class-E amplifier (PC class-E) shown in fig. 5.3will be used as our starting circuit topology. This topology valid for $q = 1.412$ offers the advantage of maximum value of optimum load for the same supply voltage and power, combined with a small value of feed inductor [45].

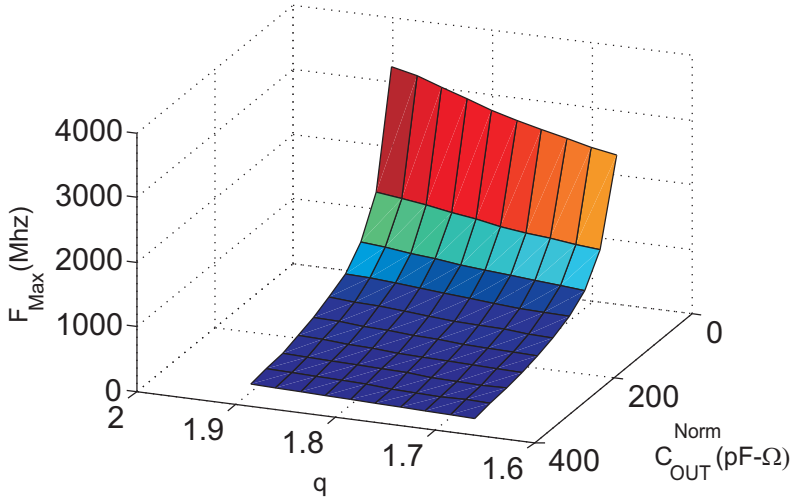
The elements' values can be expressed as a function of drain bias voltage, RF output power and frequency of operation and are shown in equations (5.11) to (5.13) [45]. In the following, it is assumed that the output capacitance of the transistor C_{OUT} is larger than the optimum value obtained from (5.13), i.e $C_{OUT} = C + C_{EX}$, with C_{EX} representing the excess capacitance.



(a) Fmax for $0.6 < q < 1$



(b) Fmax for $1 < q < 1.65$



(c) Fmax for $1.65 < q < 1.9$

Figure 5.2: Maximum frequency for nominal class-E operation

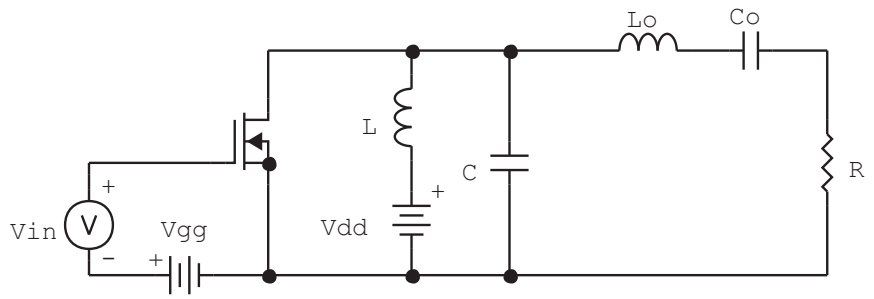


Figure 5.3: Basic circuit of parallel circuit class-E power amplifier

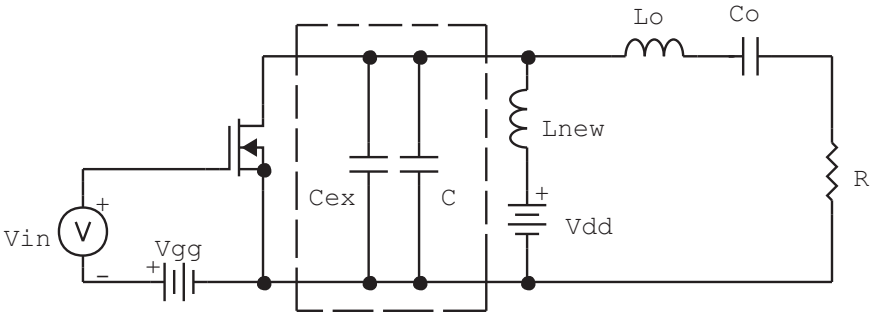


Figure 5.4: Parallel circuit class-E power amplifier showing excess capacitance

$$R = 1.365\frac{V_{dd}^2}{P_{out}} \tag{5.11}$$

$$L = 0.732\frac{R}{\omega_0} \tag{5.12}$$

$$C = \frac{0.685}{\omega_0 R} \tag{5.13}$$

In order to obtain optimum class-E operation, a different value of feed inductor is required as depicted in fig. 5.4. The value of this inductor has to be chosen in such a way that the capacitive susceptance of C_{EX} is compensated not only for the fundamental operating frequency but also for the harmonic components. Adding the susceptance of C_{EX} and L_{new} should result in the susceptance of L for all ω, i.e.:

$$\frac{1}{j\omega L} = j\omega C_{EX} + \frac{1}{j\omega L_{new}} \tag{5.14}$$

Therefore the value of the required inductor is equal to:

$$L_{new} = \frac{L}{1 + (\frac{\omega}{\omega_{EX}})^2} \tag{5.15}$$

with $\omega_{EX}^2 = 1/(L \cdot C_{EX})$. Equation (6.1) indicates that this inductor is frequency dependent. Later on it will be shown that this frequency-dependent function can be realized

by means of an appropriate arrangement of lumped components that vary according to the number of harmonics to be accounted for.

Taking into account that the output series resonator has a high Q factor and is tuned to the fundamental frequency ω_0, the input impedance seen at the C_{OUT}-plane[3] is obtained:

$$\begin{aligned} Z_{in}(\omega_0) &= \frac{j\omega_0 R L_{new}}{R + j\omega_0 L_{new}} \\ &= \frac{j\omega_0 R \left[\frac{L}{1+(\omega_0/\omega_{EX})^2}\right]}{R + j\omega_0 \left[\frac{L}{1+(\omega_0/\omega_{EX})^2}\right]} \end{aligned} \tag{5.16}$$

To simplify the derivation, define the following quantity:

$$\beta_{EX} = 1 + \left(\frac{\omega_0}{\omega_{EX}}\right)^2 \tag{5.17}$$

Now (5.16) can be re-written as:

$$\begin{aligned} Z_{in}(\omega_0) &= \frac{j\omega_0 RL}{R\beta_{EX} + j\omega_0} \\ &= \frac{\omega_0^2 RL^2 + j\omega_0 R^2 L\beta_{EX}}{R^2\beta_{EX}^2 + \omega_0^2 L^2} \\ &= \frac{\left(\frac{\omega_0 L}{R}\right)}{\beta_{EX}^2 + \left(\frac{\omega_0 L}{R}\right)^2} R\left[\left(\frac{\omega_0 L}{R}\right) + j\beta_{EX}\right] \end{aligned} \tag{5.18}$$

Using (5.12) in (5.18)

$$\begin{aligned} Z_{in}(\omega_0) &= \frac{0.732R}{\beta_{EX}^2 + (0.732)^2}(0.732 + j\beta_{EX}) \\ &= \frac{R[1 + j1.366\beta_{EX}]}{1 + 1.866\beta_{EX}^2} \end{aligned} \tag{5.19}$$

and using the expression for β_{EX}

$$Z_{in}(\omega_0) = R \cdot \frac{1 + j1.366[1 + (\omega_0/\omega_{EX})^2]}{1 + 1.866[1 + (\omega_0/\omega_{EX})^2]^2} \tag{5.20}$$

The impedance seen at the harmonics can be obtained by taking into account the high Q assumption and (6.1):

$$Z_{in}(n\omega_0) = j\frac{n\omega_0 L}{1 + n^2(\omega_0/\omega_{EX})^2} \quad n = 2, 3... \tag{5.21}$$

[3]The nodes of the 1-port network consisting of the switch in parallel with C_{OUT} is referred here to as C_{OUT}-plane.

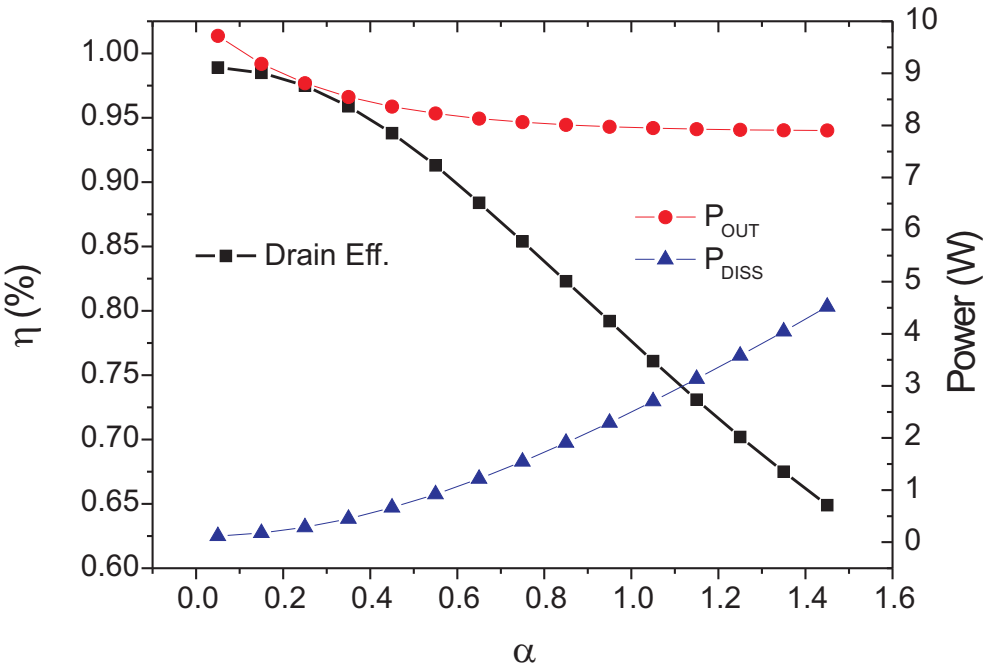


Figure 5.5: Drain efficiency, output power and power dissipation vs. α.

Defining the *excess factor* $\alpha = C_{EX}/C$ and using (5.12) and (5.13) in the equation of ω_{EX}:

$$\omega_{EX} = \left(\sqrt{\frac{2}{\alpha}}\right)\omega_0 \tag{5.22}$$

The input impedance seen by the switch-C_{OUT} combination can be written as a function of the excess factor α as shown below:

$$Z_{in}(\omega_0) = R \cdot \frac{1 + j1.366(1 + 0.5\alpha)}{1 + 1.866(1 + 0.5\alpha)^2} \tag{5.23}$$

and at the harmonics

$$Z_{in}(n\omega_0) = j\frac{n\omega_0 L}{1 + 0.5\alpha n^2} \quad n = 2, 3... \tag{5.24}$$

In order to have an idea of the impact of the excess factor (excess capacitance), the drain efficiency, output power and power dissipation have been calculated using the MATLAB code available in [80]. The data in fig. 5.5 has been obtained by varying the parallel capacitance of the PC class-E according to $C_{parallel} = C(1 + \alpha)$ while keeping constant the rest of the circuit components.

By replacing the value of the inductor obtained in (5.12) with the new value obtained in (6.1), it is possible to compensate for C_{EX} achieving optimum class-E operating conditions.

5.2 Lumped Equivalent Circuit of New Inductor

For $\alpha = 0$ the excess capacitance $C_{EX} = 0$ and therefore a single-valued inductor is enough to obtain optimum PC-Class-E operation. As the value of α increases, different values of the inductor are required for each harmonic component as defined by (6.1). The normalized values of the inductive reactance according to (6.11) are shown in fig. 5.6 for several values of α. Four regions can be identified in fig. 5.6 by taking into account the values of the harmonic reactances relative to each other. For values of $\alpha < 1/3$ (region I) the reactance of the 3rd harmonic is higher than the reactance of the 2nd and fundamental one, i.e $X_{3f0} > X_{2f0} > X_{f0}$. The values of the harmonic reactances change with respect to each other as α varies and for $\alpha > 1$ (region IV) $X_{f0} > X_{2f0} > X_{3f0}$.

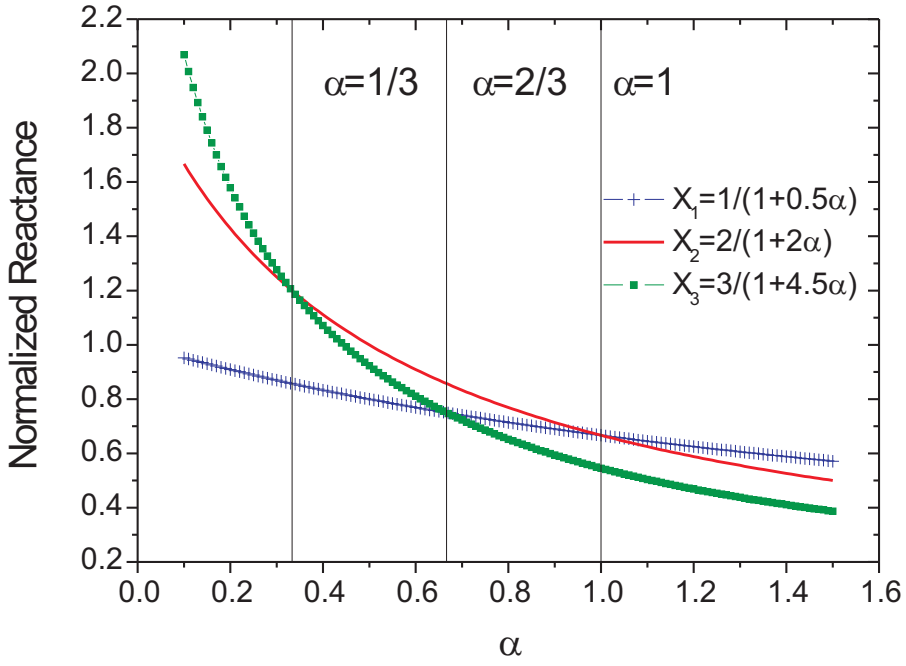


Figure 5.6: Normalized inductive reactance vs α.

The impedance magnitude corresponding to the fundamental, 2nd and 3rd harmonics for four values of the excess parameter in each of the four regions are shown in fig. 5.7.

In order to model the response in fig. 5.7, a lumped-element equivalent circuit composed of a series inductor and two parallel LC resonators is proposed here[4]. The PC-Class-E including this equivalent network is depicted in fig. 5.8a. By observing the corresponding magnitude diagram of each of the impedances of this equivalent network, it is possible to figure out how the response in fig. 5.7 is obtained. Figure 5.9 shows the diagrams of the impedances $Z_1 = j\omega L_1$, $Z_2 = j\omega L_2//(1/j\omega C_2)$ and $Z_3 = j\omega L_3//(1/j\omega C_3)$.

The resonance frequency ω_2 of the L_2C_2 branch is located between ω_0 and $2\omega_0$, whereas

[4] A similar network as the one shown in fig. 5.8b was used in [43] and [81] to approximate the three-harmonic impedance conditions in class-F amplifiers.

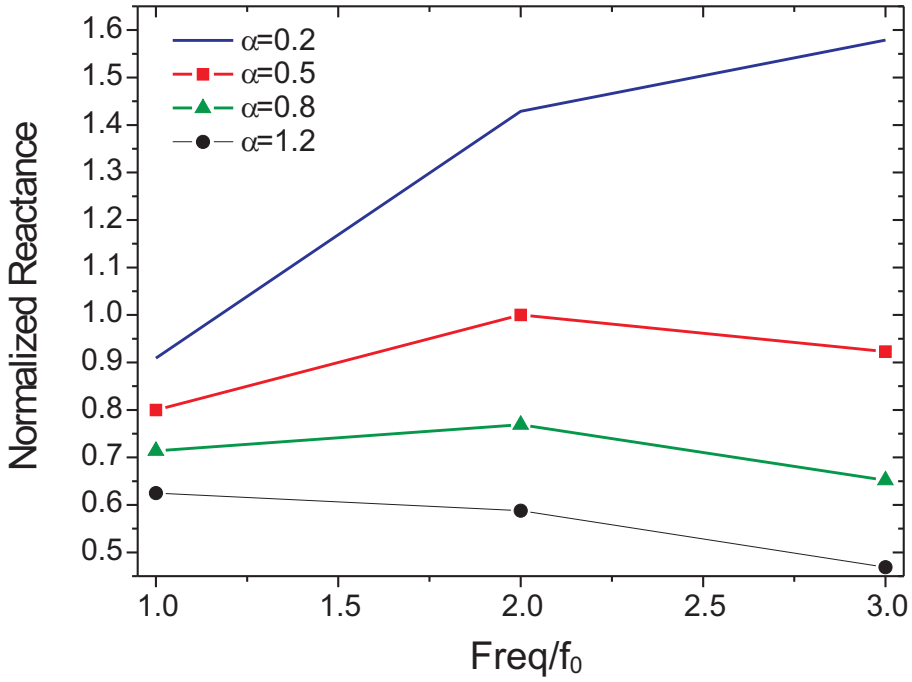
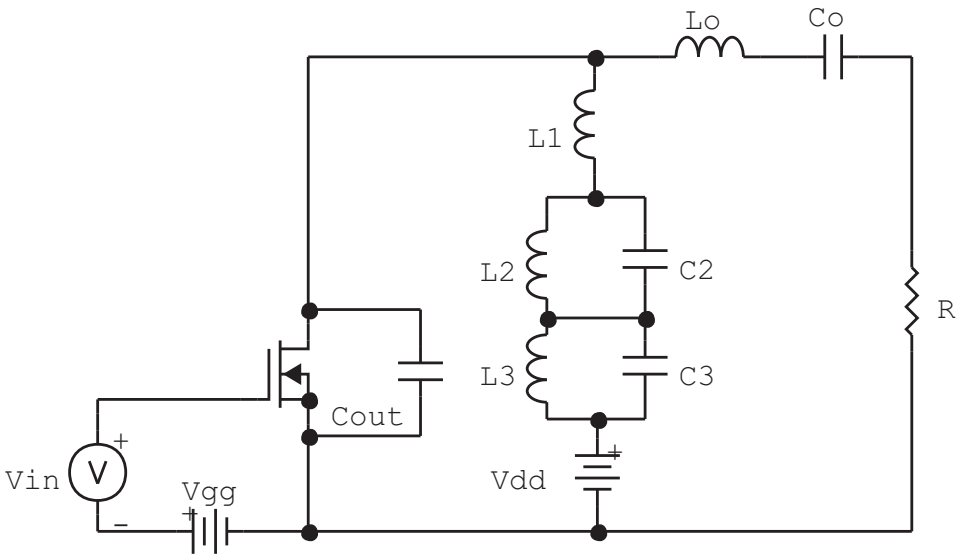
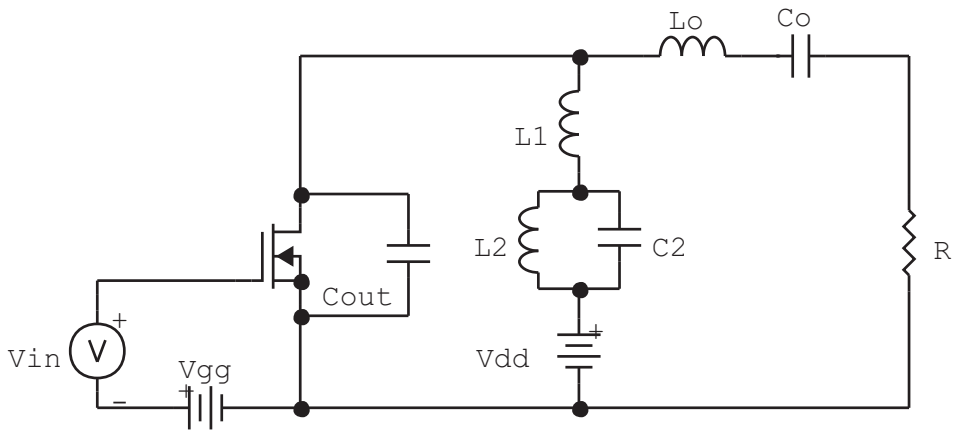


Figure 5.7: Normalized inductive reactance vs α.

the resonant frequency ω_3 of the branch L_3C_3 is located between $2\omega_0$ and $3\omega_0$. Fixing the value of these resonances and selecting appropriate values for L_1, L_2 and L_3, allows to obtain the right value of harmonic reactance. In fig. 5.7, the change in harmonic reactance can be noticed by observing the slope of the lines connecting two consecutive harmonic reactance values. For lower values of α, the value of inductance L_1 is made large enough and therefore dominates the frequency response of the network. The slopes in this case are both positive. As α takes larger values,L_1 needs to be reduced whereas L_2 and L_3 has to be increased. The larger the value of L_2, the lower the value of the harmonic reactance at the 2nd and 3rd harmonic (Z_2 exhibits a negative phase at $2\omega_0$). The same applies to L_3, which plays a major role in defining the reactance at $3\omega_0$. This qualitative analysis indicates that each of the resonators allows to control the amplitude of the different harmonics and therefore, at least in theory, the larger the number of resonators, the better it is possible to obtain the desired class-E operation, i.e ZVS and ZDVS. On the other hand, in practical applications, compensation up to the 2nd harmonic suffices. This assertion can be easily justified by inspection of fig. 5.7 once more. As α increases considerably, the reactances X_{2f0} and X_{3f0} to be synthesized by L_{new} decrease substantially up to a point in which their values might be in the order of magnitude of the circuit parasitics. Having this in mind, a simplified topology with only one resonator is considered here as depicted in fig 5.8b (equations for the $L_1L_2C_2L_3C_3$ network can be found in Appendix C). The equations relating the values of the components to the excess factor α can be obtained by equating the impedance of the $L_1L_2C_2$ network to the impedances in (6.11) for $n = 1$ and $n = 2$, as follows:



(a) Two-resonator topology



(b) Single-resonator topology

Figure 5.8: New topology of PC class-E

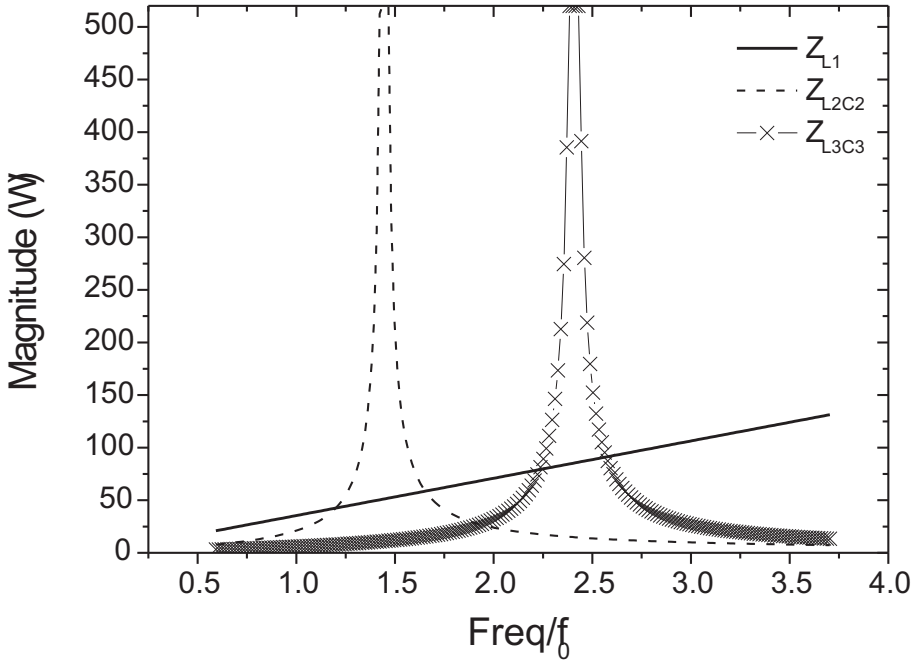


Figure 5.9: Input impedance magnitude of each component in $L_1L_2C_2$ network.

$$\omega_0 L_1 + \frac{\omega_0 L_2}{1 - \omega_0^2 L_2 C_2} = \frac{\omega_0 L}{1 + 0.5\alpha} \tag{5.25}$$

$$2\omega_0 L_1 + \frac{2\omega_0 L_2}{1 - 4\omega_0^2 L_2 C_2} = \frac{2\omega_0 L}{1 + 2\alpha} \tag{5.26}$$

The resonant frequency ω_2 of theL_2C_2 resonator fulfills $\omega_o < \omega_2 < 2\omega_o$ and can be related to the fundamental frequency ω_0 by means of a new parameter denoted here as γ. Equations (5.25) and (5.26) can now be written as:

$$\gamma = \left(\frac{\omega_o}{\omega_2}\right)^2 \tag{5.27}$$

$$\omega_0 L_1 + \frac{\omega_0 L_2}{1 - \gamma} = \frac{\omega_0 L}{1 + 0.5\alpha} \tag{5.28}$$

$$2\omega_0 L_1 + \frac{2\omega_0 L_2}{1 - 4\gamma} = \frac{2\omega_0 L}{1 + 2\alpha} \tag{5.29}$$

Solving these system results in

Table 5.1: Parameters of experiment

Parameter	Value
Device	MRF21010
Frequency	434 MHz
Drain Voltage	20 V
Output Capacitance	10 pF
Expected P_{OUT}	10 W

Table 5.2: Circuit Parameters for $q = 1.412$

Parameter	Value
L	14.66 nH
R	54.60 Ω
C	4.60 pF
C_{EX}	5.40 pF
α	1.174
L_1	5.93 nH
L_2	1.62 nH
C_2	42.40 pF

$$L_1 = \frac{L(2\gamma + \alpha)}{\gamma(2\alpha^2 + 5\alpha + 2)} \tag{5.30}$$

$$L_2 = -\frac{\alpha L(4\gamma^2 - 5\gamma + 1)}{\gamma(2\alpha^2 + 5\alpha + 2)} \tag{5.31}$$

$$C_2 = \frac{\gamma}{\omega_o^2 L_2} \tag{5.32}$$

5.3 Simulations and Measurements

In this section, a design example is given to verify the validity of the approach introduced in the preceding sections. The objective of the design is to demonstrate high efficiency class-E operation for values of C_{OUT} larger than the optimum parallel capacitance required by the conventional PC class-E topology. Table 5.1 shows the main parameters of the experiment.

With the value of $\alpha = 1.174$ shown in Table 5.2 and fig. 5.5, a maximum drain efficiency close to 72 % seems to be attainable by using the conventional PC class-E topology. It is important to consider that the efficiency plot depicted in fig. 5.5 does not include losses due to the non-ideal behavior of the switch. Alinikula [82] has calculated the impact of switch resistance (R_{ON}) on drain efficiency of a lossy class-E amplifier. The device used in this report exhibits an R_{ON} value close to 1.3 Ω [5]. Hence the expected maximum efficiency

[5] The value of R_{ON} has been obtained from the simulated IV curves using Motorola's large-signal model.

(for $\alpha = 0$) falls below 95 %, originating a downwards shifting of the whole efficiency curve in fig. 5.5.

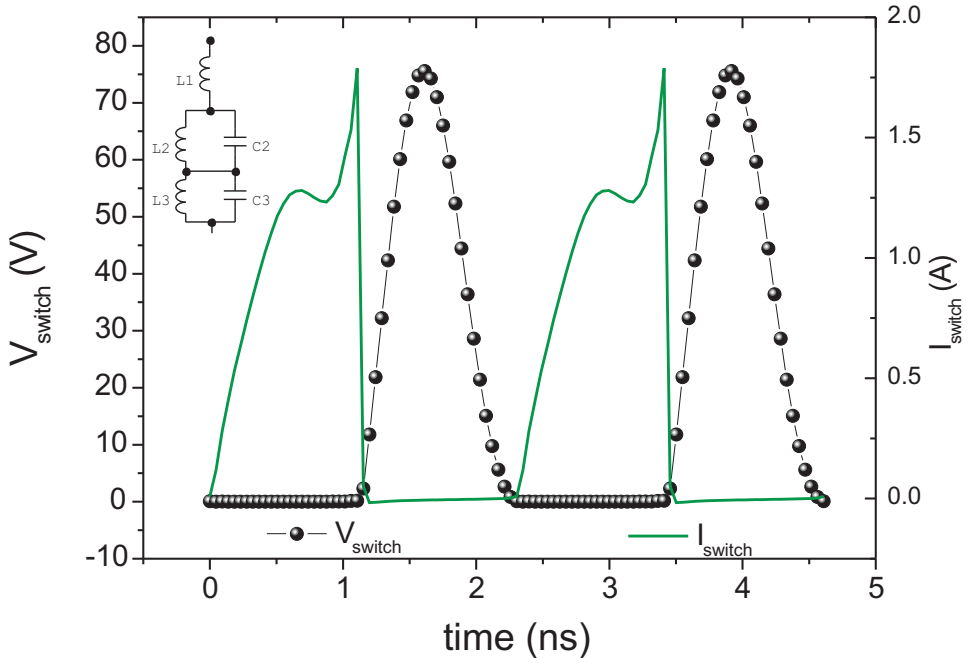
The design steps are summarized as follows:

- Selection of operating frequency, drain supply voltage and expected output power. This information is shown in Table 5.1.
- Use of equations (5.11) to (5.13) to determine the optimum parameters of the conventional PC class E (results in Table 5.2).
- Calculation of the excess capacitance with: $C_{EX} = C_{OUT} - C$, and of the excess factor $\alpha = C_{EX}/C$.
- Selection of the resonant frequency ω_2 taking into account $\omega_o < \omega_2 < 2\omega_o$ and calculation of γ using equation (6.7). A good choice for ω_2 is $1.5\omega_o$, resulting in $\gamma = 4/9$. In this example, this resonance frequency was selected as to maximize the value of L_2 making easier its physical implementation. Taking the derivative of (6.5) with respect to γ and equating to zero results in $\gamma = 0.5$.
- Use of equations (6.4) to (6.6) to obtain the values of the $L_1L_2C_2$ network.

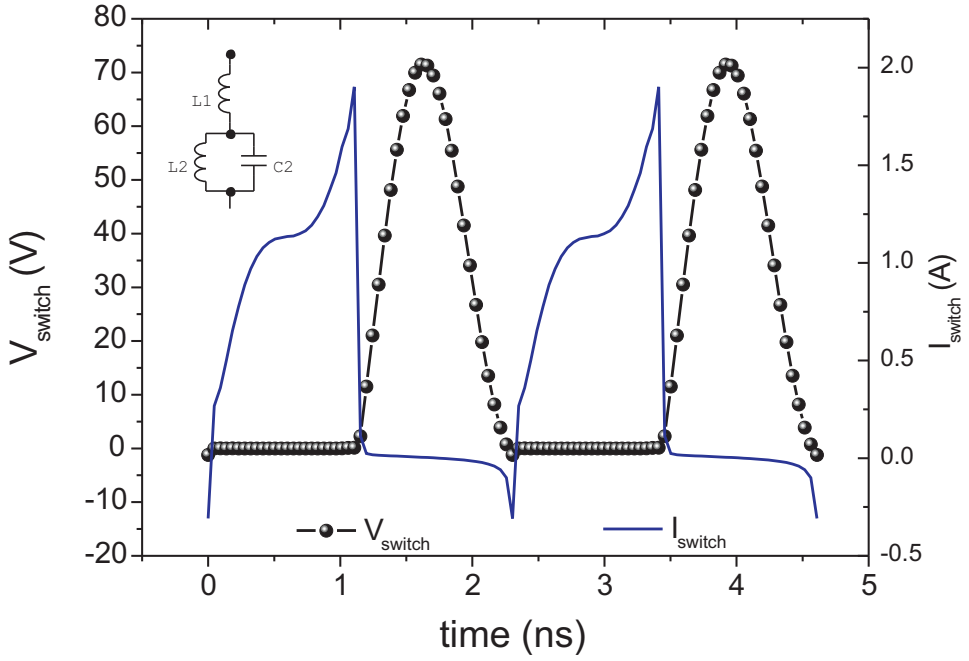
Initial simulations using an ideal switch indicates that class-E operation is still obtained by using the proposed topology as depicted in fig. 5.10a. For a single-resonator, the switch current exhibits a small negative peak that is seen to disappear when using two resonators. As a matter of fact, the switch voltage also displays a very small negative value (close to zero) at the turn-on time, indicating that C_{OUT} is not totally discharged. When observing the current through C_{OUT} in the frequency domain, it is seen that the 3rd harmonic component, together with the fundamental one, contributes to reduce the total current through C_{OUT} making it zero at the turn-on time. The magnitude of the 3rd harmonic component in the single-resonator case is smaller and consequently a non-zero current at turn-on is obtained.

The component values of the output series resonator L_o and C_o (fig. 5.8b) were obtained by selecting $Q = 8$ and by setting the resonance frequency equal to 434 MHz. At this point it is important to recall that the high-Q assumption was used in the preceding calculations. Kazimierczuk and Puczko [83] have analyzed the effect of the using a non-infinite Q factor when calculating the optimum circuit parameters of a class-E amplifier. They concluded that for the range $7 \leq Q \leq 10$ this effect can be neglected as errors are found to be less than 10 %. Therefore the value for Q chosen here is within acceptable limits. The input of the transistor was conjugately matched at the frequency of operation.

The transistor was biased below pinch-off at a gate voltage $V_{GS} = 3.0\,V$. The equivalent circuit of the implemented amplifier is shown in fig. 5.11a. Inductors $LM1$ and $LM2$ as well as $Lgate$ were replaced by transmission lines implemented in 30 mil RO4350B. The resonator L_2C_2 at the output of the amplifier is connected to L_1 at one side and to an RF ground (bypass capacitors) at the other side. In this caseC_2 was directly connected to the ground plane without affecting the topology. An additional finite DC feed (100 nH) and additional bypass capacitors were used to provide additional protection to the DC source. The capacitor C_p and series inductor L_s transform the 50 Ω impedance to a higher value



(a) Two-resonator topology



(b) Single-resonator topology

Figure 5.10: Simulated waveforms using proposed class-E networks

in order to provide an impedance close to the value indicated in Table 5.2. The fabricated test board is shown in fig. 5.11b. The $L_1L_2C_2$ branch was implemented by means of SMD Accu-L inductors from AVX and ATC600S capacitors. L_1 is made of three series-connected inductors (2.2, 1.8 and 1.5 nH) resulting in a total nominal inductance equal to 5.5 nH. L_2 has a nominal value of 1.5 nH and C_2 is the parallel connection of two ATC capacitors resulting in a nominal value of 40 pF. The C_{bypass} close to L_2 consists of four capacitors each of them equal to 100 pF. The circuit was simulated in Agilent ADS using the measured S-parameters of the passive components and the large-signal model available from Freescale. The output resonator uses a Midi Spring inductor from Coilcraft with nominal value of 56 nH in series with a 2 pF capacitor. The output matching network is composed of a coil (2 turn no. 24 AWG, 1.5 mm ID) for L_s and two paralleled 1 pF capacitors for C_s.

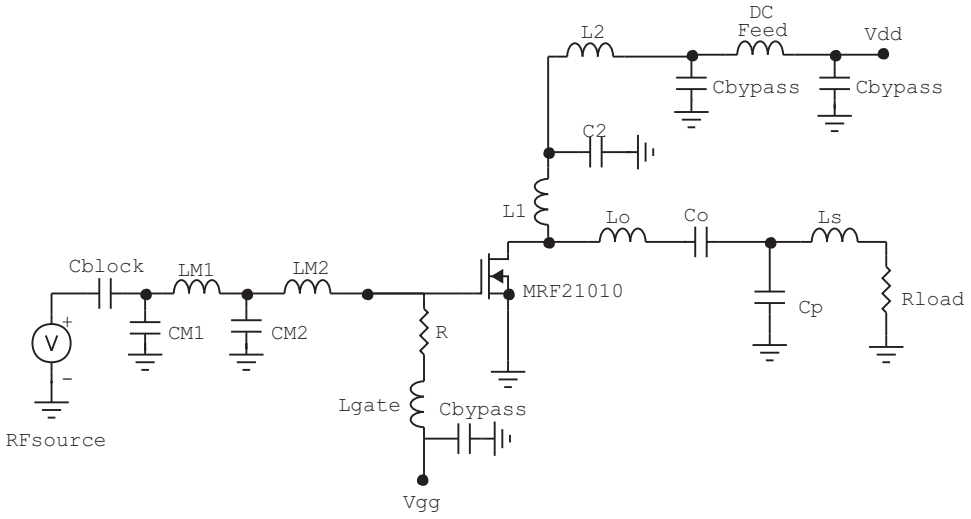
A sinusoidal signal was used to drive the device. Although more complex waveforms such as rectangular or trapezoidal might be used instead, their use increases circuit complexity. Sine-wave drive has been successfully used in class-E amplifiers [84], since it represents a usable approximation to the trapezoidal form (although not optimum) that can be improved by slightly overdriving the device [45].

Figure 5.12 shows the power sweep, gain and efficiency obtained by measurements and simulations at the operating frequency of 434 MHz. A maximum drain efficiency and PAE of 80.7 % and 78.6 %, respectively, were obtained during the measurement at an output power level of 4.91 W. The measured gain was larger than 15 dB. The measured harmonic suppression for the 2nd harmonic was larger than 27 dBc. It is seen that the measured values are much lower than the obtained by simulation. A possible explanation might lie in the incapability of the used transistor model to accurately predict large-signal operation (at least in class-E mode), a fact that has been reported in the existing literature [85].

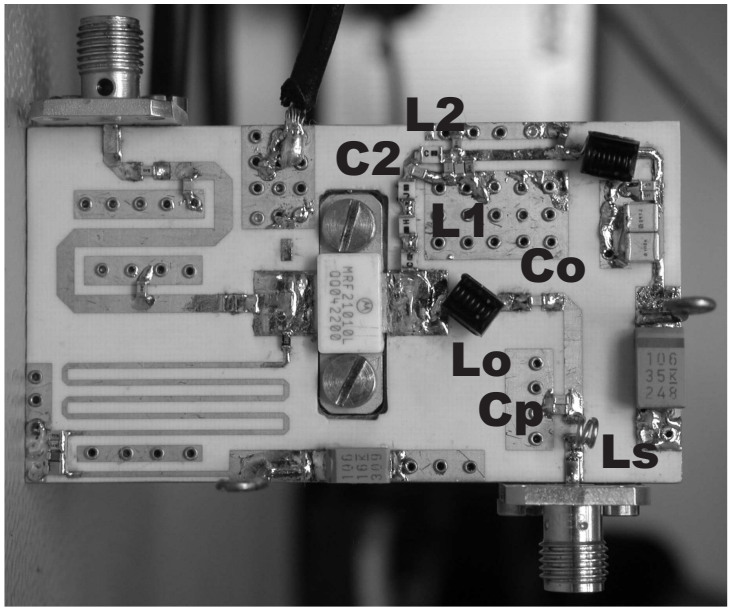
In order to evaluate the operation of the amplifier around the frequency of operation, a frequency sweep in a narrow band (±16 MHz) was performed. The results in fig. 5.13 indicate a maximum drain efficiency of 82 % and a PAE of 80.5 % at 428 MHz with an output power of 5.6 W. The influence of drain supply voltage in the performance of the amplifier was also investigated. It is important to take into account that in order to accommodate the saturation resistance and any other potential losses, which reduce the nominal value of class-E load resistance, an increase in the drain supply might be required. Additional measurements indicated that for a value of V_{DD} equal to 25 V the output power increased by 58.45 % with only a reduction in η and PAE of 1.65 % and 5.1 % respectively.

In Table 5.3 a summary of some RF power amplifiers encountered in the literature is depicted. Four of them (*i* to *iv*) use the same LDMOS device as in this work. Reference [86] uses a SiC MESFET. Common to all of them is the operation in a region in which the output capacitance is small enough to guaranty proper operation without need of inductive compensation. Please notice that this table gives an idea of the expected levels of efficiency and power when using the specified device.

The theory in Section IIB as well as the experimental verification presented in here, were initially based in the topology obtained for $q = 1.412$, i.e a parallel-circuit class-E. It is important to remark that the design procedure described here does not depend on the values of q assumed. For cases in which α increases considerable (and $q = 1.412$), the values taken by the lumped components of the $L_1L_2C_2$ network might become impractical. In this case the authors recommend the selection of a more suitable value for q. An alternative



(a) Circuit of designed PA



(b) The manufactured PA

Figure 5.11: Schematic and picture of designed prototype

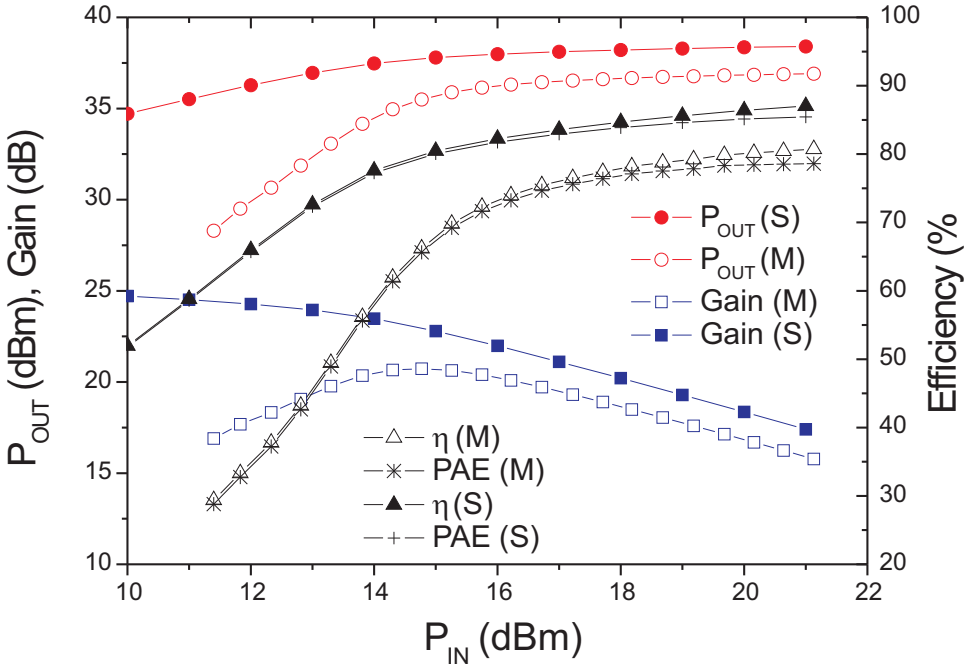


Figure 5.12: Large-signal response of amplifier

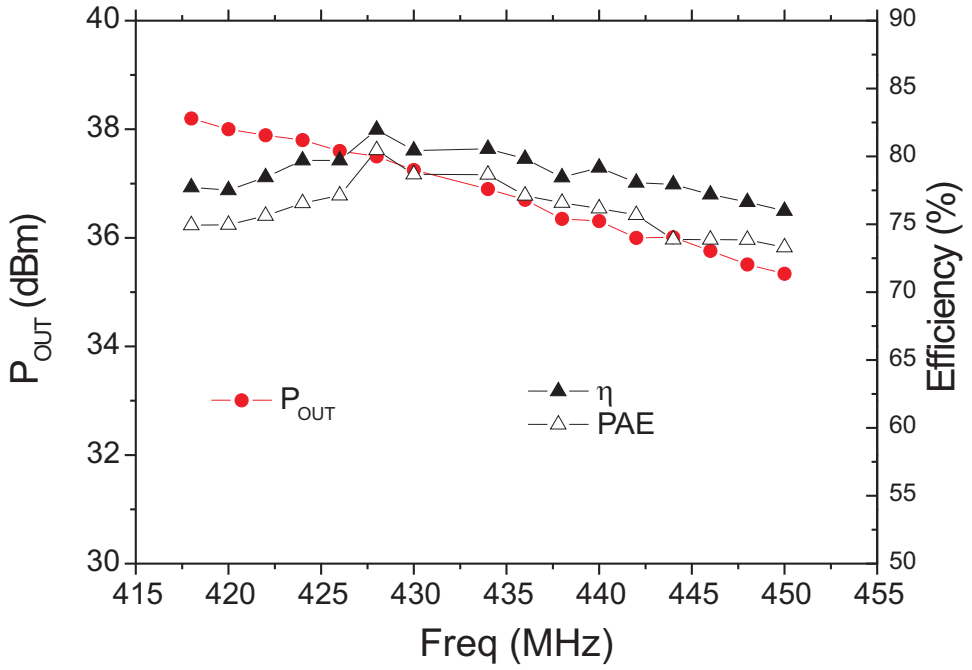


Figure 5.13: Large-signal performance over frequency

Table 5.3: Performance summary of various high-efficiency power amplifiers

	PA Class	$P_0\,(W)$	$\eta\,(\%)$	$f_0\,(MHz)$	$V_{DD}\,(V)$	Comments	Ref.
i	Class-E	4.17	83.60	100	15	[a]	[87]
ii	inv. Class-E	10.00	78.42	155	21	[b]	[88]
iii	Class-E	1.87	81.77	250	10	[c]	[85]
iv	Class-E/F_2	2.36	86.60	61.44	10	[d]	[89]
v	Class-E	20.50	86.80	145	30	[e]	[86]
vi	Class-E	7.78	79.39	434	25	$f_{0(ref)} = 434\,MHz$	This work
vii	Class-E	5.60	82.00	428	20	——–	This work

[a] $F_{max}(15V) \approx 1.67 \cdot F_{max}(25V)$ and $f_0 = 0.23 \cdot f_{0(ref)}$
[b] $F_{max}(21V) \approx 1.19 \cdot F_{max}(25V)$ and $f_0 = 0.36 \cdot f_{0(ref)}$
[c] $F_{max}(10V) \approx 2.50 \cdot F_{max}(25V)$ and $f_0 = 0.58 \cdot f_{0(ref)}$
[d] $F_{max}(10V) \approx 2.50 \cdot F_{max}(25V)$ and $f_0 = 0.14 \cdot f_{0(ref)}$
[e] Device used: SiC MESFET and $f_0 = 0.33 \cdot f_{0(ref)}$

design procedure is depicted in fig. 5.14.

Table 5.4 shows the circuit values for the finite-feed topology with $L_1L_2C_2$ network using the data on Table 5.1 assuming a $C_{OUT} = 20\,\text{pF}$ for $q = 0.5$ [6]. Even for a value as high as $\alpha = 5.53$, corresponding to the assumed C_{OUT}, the components of the $L_1L_2C_2$ network take values within acceptable limits.

Table 5.4: Example for $q = 0.5$ and $C_{OUT} = 20\,\text{pF}$

Parameter	Value
L	176.05 nH
R	25.40 Ω
C	3.06 pF
X	26.87 Ω
C_{EX}	16.94 pF
α	5.53
L_1	3.85 nH
L_2	1.90 nH
C_2	35.75 pF

[6] This is the so-called *subharmonic* class E from the literature [45].

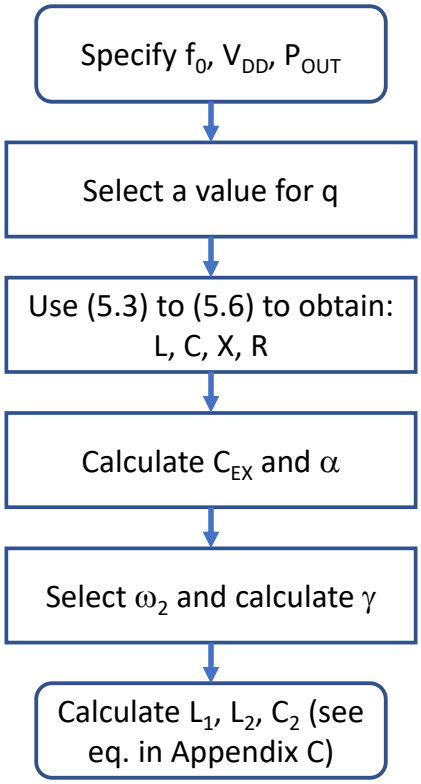


Figure 5.14: Alternative design procedure for variable q

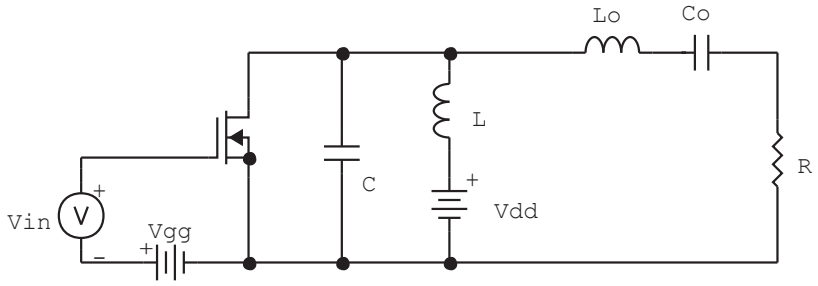
6 Inductive Compensated Microwave Class-E Power Amplifier

In this chapter a simulation-based analysis is presented to firstly evaluate the impact of excessive transistor output capacitance on class-E power amplifiers and to secondly show how inductive compensation can be used to recover optimum class-E operating conditions. As a starting point, the finite-feed inductor in a parallel-circuit topology is replaced by a frequency-dependent inductor, which in turn can be substituted by the new topologies introduced in chapter 5. This complex lumped-element network is then replaced by a generalized transmission line equivalent topology, suitable for microwaves. Calculation of the transmission line impedances and electrical lengths of the proposed generalized network is shown in detail and a design procedure for this modified class-E is provided. The analysis presented here is further extended by using a simplified large-signal model for the employed GaN HEMT device, which allows evaluating the effects of non-ideal switching as well as of capacitance voltage-dependency and feedback capacitance. The analysis is validated by simulation and design of a test board. Measurements of the test board showed a drain efficiency of 80.3%, power-added efficiency of 76.3% and output power of 40.1 dBm at 1.96 GHz, demonstrating the validity of the proposed approach. The approach and results in this chapter have been published in the *International Journal of RF and Microwave Computer-Aided Engineering* [90].

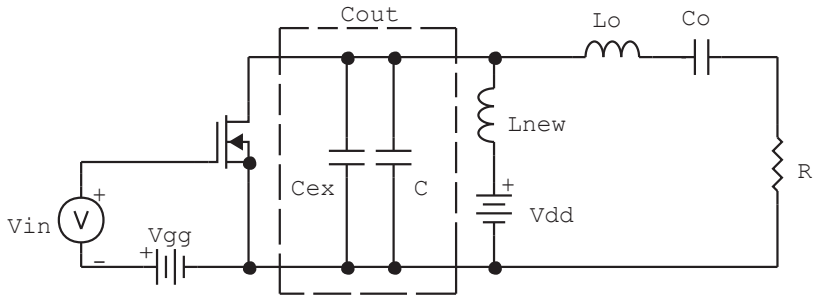
The approach presented in chapter 5 allows to compensate the excessive capacitance not only at the fundamental but also at the harmonic frequencies, recovering in this way the class-E operating conditions. This so-called *Frequency-Dependent Inductive Compensation (FDIC)* will be further investigated to understand its feasibility and limitations at higher frequencies. The new circuit topologies in chapter 5 employ lumped elements that can be used at UHF but are less suitable for microwave frequencies. For that reason, some authors have presented, following the approach in [12], alternative structures using transmission lines to achieve compensation at the fundamental and harmonics as is the case of Leng et al. [13] and Cheng et al. [14]. Liu et al. [91] has also introduced a parallel-circuit class-E/F power amplifier, which includes a transmission line based compensating network to account for excessive transistor output capacitance. Nevertheless, the maximum operating frequency of the network in [91] is below that of a parallel-circuit class-E.

Following aspects are addressed in this chapter:

- Replacing the ideal switch by a more complete transistor model, namely, a voltage-controlled current source (which intrinsically includes pinch-off voltage, saturation resistance, etc.) together with the non-linear transistor capacitances,
- Reviewing the effect of the FDIC on the transistor drain voltage and current wave-



(a) Class-E amplifier without excess capacitance



(b) Class-E amplifier showing excess capacitance

Figure 6.1: Parallel-Circuit Class-E topology

forms and discussing the limitations of the inductive compensation,

- Presenting an alternative design approach for FDIC-Class-E (i.e. a class-E PA employing frequency-dependent inductive compensation), which simplifies the class-E topology by unifying the compensation network, harmonic-suppression and matching network to obtain more design flexibility.

The next section of this manuscript starts by reviewing the frequency-dependent inductive compensation technique and corresponding topologies according to [12]. In addition to this, the transmission line networks presented in [13] and [14] will be shortly described. In section III this approach will be evaluated at microwaves using firstly an ideal switch and then a simplified large-signal transistor model. A general approach to design FDIC-class-E power amplifiers together with simulations and measurement results of a test board are presented in section IV.

6.1 Review of FDIC

6.1.1 General Concept

In chapter 5 it was demonstrated that a frequency-dependent inductor is required to compensate the excess capacitance C_{EX} not only for the fundamental operating frequency f_0 but also for $2 \cdot f_0$ and $3 \cdot f_0$. This can be readily seen with the help of figure 6.1 (previously shown as figures 5.3 and 5.4).

The new inductor L_{new} in figure 6.1b will provide enough inductive susceptance to cancel out the excessive capacitance C_{EX} (with $C_{out} = C_{EX} + C$), at the same time that leaves a remaining inductance L, i.e. the optimum value for proper operation in class-E. The value of the compensating inductor was determined in section 5.1.2 and is given as follows:

$$L_{new} = \frac{L}{1 + (\frac{\omega}{\omega_{EX}})^2}, \tag{6.1}$$

where $\omega_{EX}^2 = 1/(L \cdot C_{EX})$ represents the resonance frequency of the parallel circuit formed by $L - C_{EX}$. This frequency can be related to the *excess factor* $\alpha = C_{EX}/C$ according to equation (6.2)

$$\omega_{EX} = \left(\sqrt{\frac{2}{\alpha}}\right)\omega_0. \tag{6.2}$$

The reactance associated to L_{new} at the fundamental and harmonics is given by

$$X_{new}(n\omega_0) = \frac{n\omega_0 L}{1 + 0.5\alpha n^2} \quad n = 1, 2, 3... \tag{6.3}$$

Table 6.1 shows the normalized reactance $X(n\omega_0) = X_{new}(n\omega_0)/\omega_0 L$ for few values of the excess factor α. The first row ($\alpha = 0$) corresponds to the case $C_{out} = C$ and in this case L_{new} is constant and equal to the optimum value L. As α increases the reactance does not increase directly proportional with frequency, as would be expected for a constant inductor, but rather exhibits a frequency-dependent behavior that is a function of the excess factor α.

Table 6.1: Normalized reactance of L_{new} for fundamental and harmonics

α	C_{out}/C	$X(\omega_0)$	$X(2\omega_0)$	$X(3\omega_0)$
0	1.00	1.00	2.00	3.00
1/3	1.33	0.86	1.20	1.20
2/3	1.66	0.75	0.86	0.75
1	2.00	0.66	0.66	0.54

Once the frequency-domain response of this inductor has been defined, it is necessary to synthesize a passive network capable of describing this behavior. Next subsection review these lumped-element topologies as well as transmission line alternatives for microwave frequencies.

6.1.2 Equivalent Networks of Frequency-Dependent Inductor

Two topologies were proposed in chapter 5. The first one allows compensation up to the 2nd harmonic and is composed of an inductor L_1 in series with a parallel resonators $L_2 - C_2$, whereas compensation up to the 3rd harmonic can be accomplished by including an additional parallel resonator $L_3 - C_3$ in series with the first one. The one-resonator implementation is reproduced once again in figure 6.2.

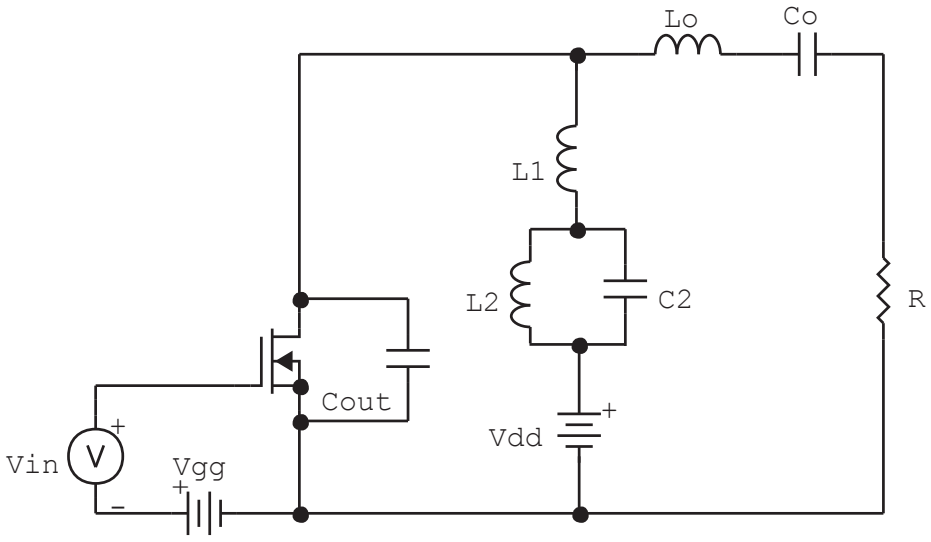


Figure 6.2: One-resonator topology according to [12]

This topology will be used in next section to evaluate the FDIC at microwaves. The equations in section 5.2, which are shown below for completeness, can be used to calculate its circuit elements:

$$L_1 = \frac{L(2\gamma + \alpha)}{\gamma(2\alpha^2 + 5\alpha + 2)} \tag{6.4}$$

$$L_2 = -\frac{\alpha L(4\gamma^2 - 5\gamma + 1)}{\gamma(2\alpha^2 + 5\alpha + 2)} \tag{6.5}$$

$$C_2 = \frac{\gamma}{\omega_o^2 L_2}, \tag{6.6}$$

where γ represents the relation between the fundamental frequency ω_0 and the resonance frequency ω_2 of the $L_2 - C_2$ resonator as given in equation (6.7). For the one-resonator topology to work properly this resonance frequency needs to fulfill $\omega_o < \omega_2 < 2\omega_o$.

$$\gamma = \left(\frac{\omega_o}{\omega_2}\right)^2 \tag{6.7}$$

A drawback of the topology in figure 6.2 is that the inductances of L_1 and L_2 decrease considerable at microwave frequencies. The inductor L_2, for instance, takes values below 0.5 nH for frequencies beyond 2 GHz, making its physical implementation critical and susceptible to fabrication tolerances.

Leng et al. [13] substitutes the one and two-resonator topologies by a cross-shaped transmission line topology, composed of two series lines and two shunt $\lambda/8$ stubs. The circuit used to compensate the excess capacitance for f_0 and $2 \cdot f_0$ is shown in figure 6.3. An alternative topology is presented by Cheng et al. [14] and is depicted in figure 6.4. In this case, the lumped elements are directly mapped to transmission lines according to the

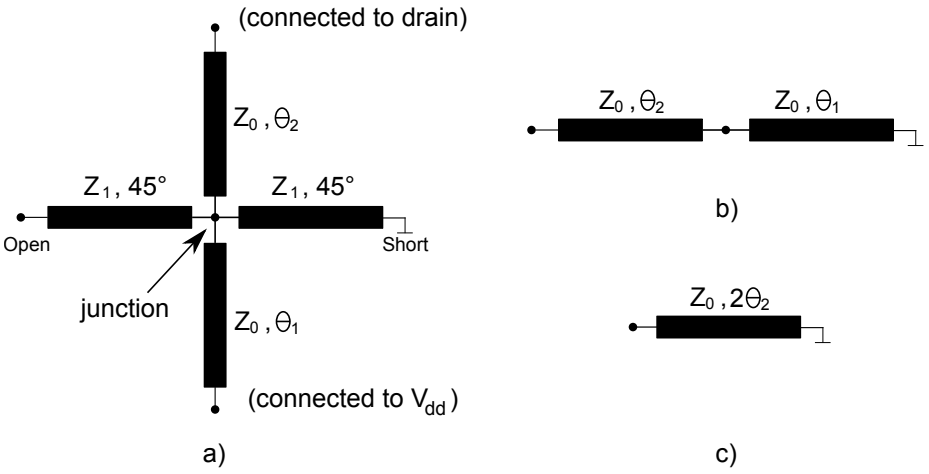


Figure 6.3: Equivalent circuit according to Leng et al. [13] a) General topology b) circuit at f_0 c) circuit at $2 \cdot f_0$

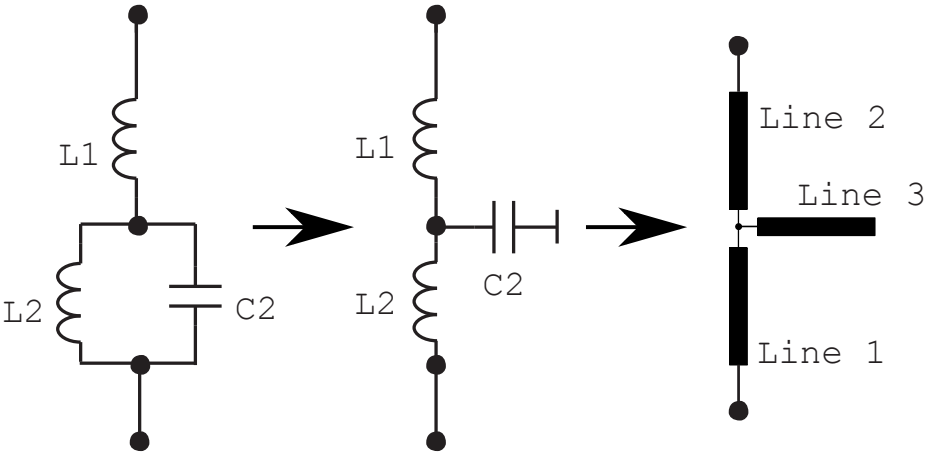


Figure 6.4: Equivalent circuit according to Cheng et al. [14]

methodology described in [11].
Although those approaches seem to offer the possibility of implementing the compensating network a microwaves, they also suffer from a similar problem encountered in the lumped-element topology, namely, as α increases, the electrical length of the transmission lines become too small to be conveniently implemented. In the case of the transmission-line approach, the lengths of the series lines Line 1 and Line 2 also become too small. In [13] the electrical lenght θ_1 of Line 1 is approximately 8 degrees, which is shorter than 1.5 mm when using, for instance, the well-known substrate RO4350B [92].

6.2 FDIC Evaluation using Transistor Model

6.2.1 Extraction of compact HEMT Model

Figure 6.5a shows the simplified transistor model, which will be used to replace the ideal switch in the class-E amplifier circuit. In order to describe the dependency of the drain current on the gate and drain voltages, the Curtice current equation has been used as shown in equation (6.8) [93]

$$I_{ds}(V_{gs}, V_{ds}) = p \cdot (V_{gs} - V_{to})^n (1 + \lambda \cdot V_{ds}) \cdot \tanh(q \cdot Vds). \tag{6.8}$$

The parameters of this expression have been determined by fitting the IV response obtained by simulation using the proprietary HEMT model for the device CGH60015 [94]. Figure 6.5b shows the simulated drain current for both cases, i.e. for the simplified model and for the large-signal proprietary model.

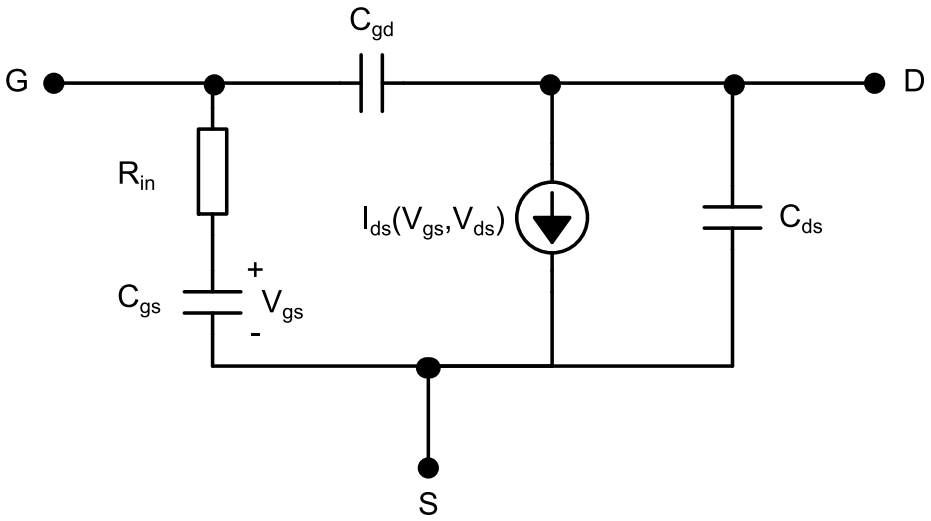
In addition to this, the voltage dependency of the intrinsic capacitances has been obtained from the imaginary part of the admittances according to [95]. Figure 6.6 presents the gate-source capacitance C_{gs} as a function of the gate-source voltage and the gate-drain capacitance C_{gd} as a function of the drain-source voltage. C_{gd} also varies with the gate voltage although this effect is more pronounced in the ohmic region where drain voltages are low. At higher V_{ds} a weaker dependency on V_{gs} is observed [96]. In this manuscript we consider only a V_{ds}-dependency for the sake of simplicity. The equation used to fit these voltage-dependent responses is given as follows [97]

$$C(v) = a + b \cdot (1 + \tanh(c \cdot v + d)). \tag{6.9}$$

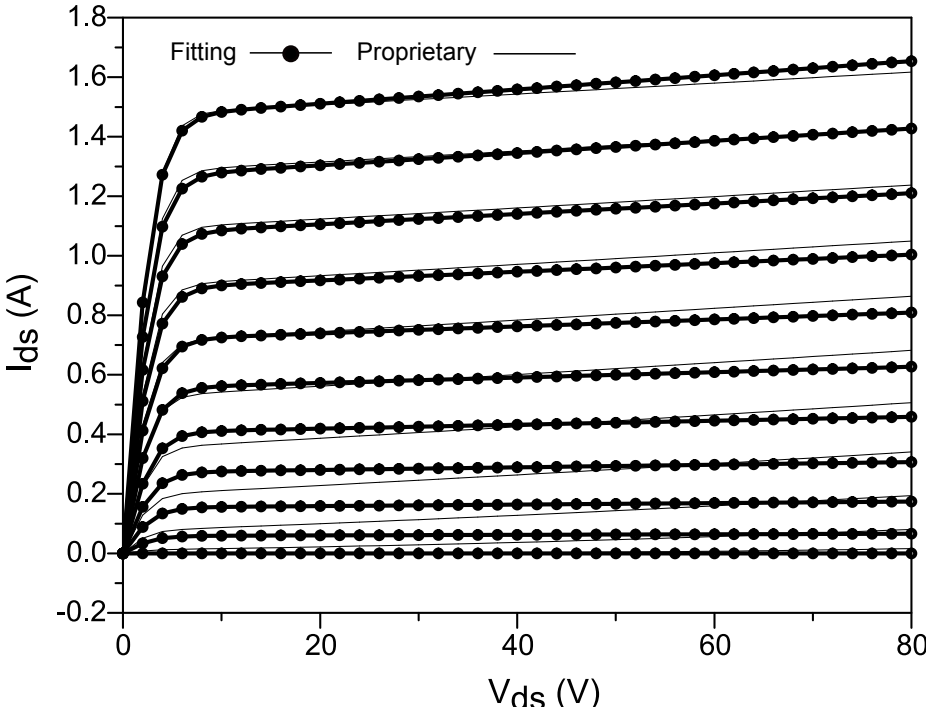
The values of the parameters in equations (6.8) and (6.9) can be found in table 6.2. The value of $R_{in} = 0.59\ \Omega$ (in series with C_{gs} in figure 6.5a) was chosen to match the input reflection coefficient S_{11} (see section 4.2, page 225 in [93]) while the device was biased at deep class AB, in this case $(V_{gsQ}, V_{dsQ}) = (-2.9\ \text{V}, 28\ \text{V})$. The drain-source capacitance C_{ds}, having a value of 0.92 pF, was found to be approximately constant over the drain-source voltage.

The equivalent circuit of the transistor using *Symbolically-Defined Devices* (SDD) [98] can be seen in figure 6.7.

Although the intrinsic elements C_{gs}, C_{gd}, C_{ds} and R_i could have been included into the main SDD2P block, it was preferred to use several subblocks and circuit elements to

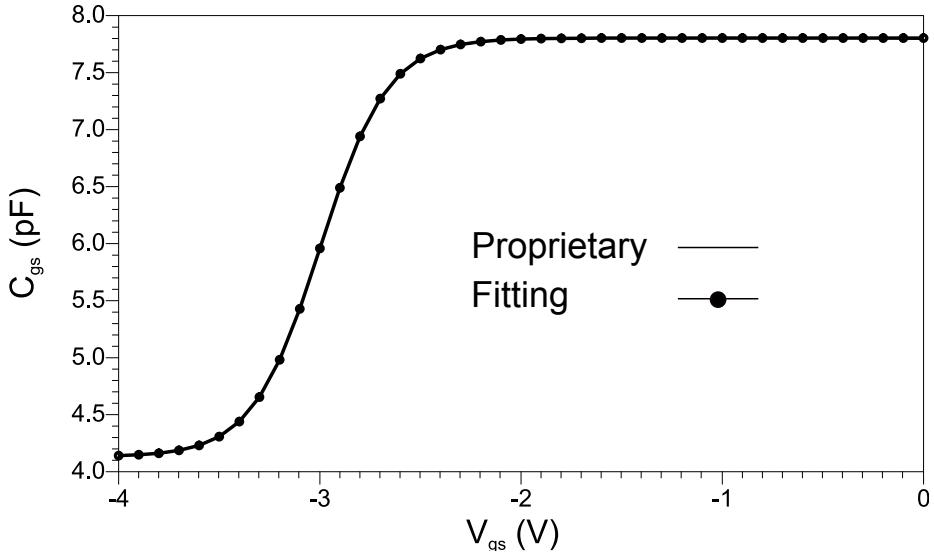


(a) Simplified HEMT model

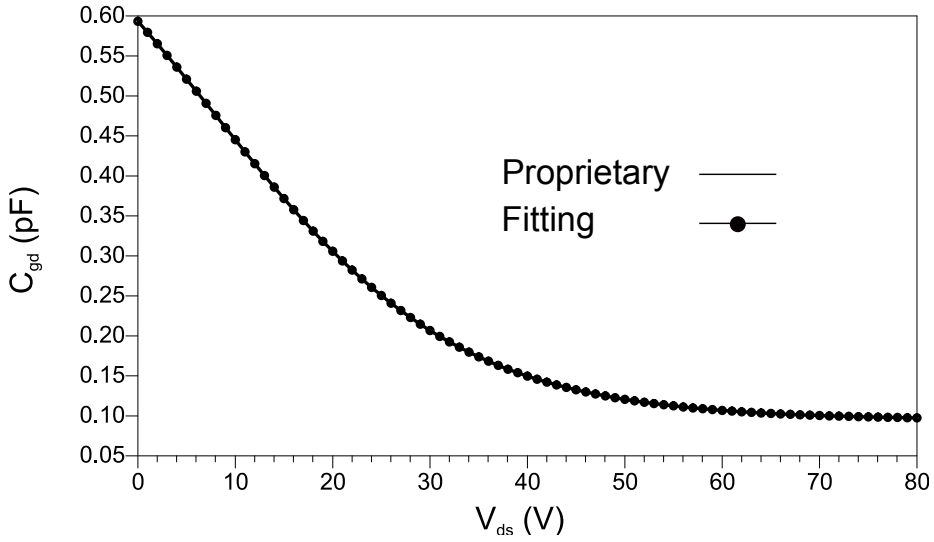


(b) IV response

Figure 6.5: Simplified model a) and IV response b) using both models



(a) Cgs vs Vgs



(b) Cgd vs Vds

Figure 6.6: Modeling the non-linear capacitances

Table 6.2: Parameters for drain current and voltage-dependent capacitances

Param.	$I_{ds}(V_{gs}, V_{ds})$	Param.	$C_{dg}(V_{ds})$	$C_{gs}(V_{gs})$
p	0.48520	a	0.8554	7.803
n	1.4	b	-0.3802	-1.836
λ	0.00163	c	0.0400	-2.977
q	0.3268	d	-0.4800	-8.926

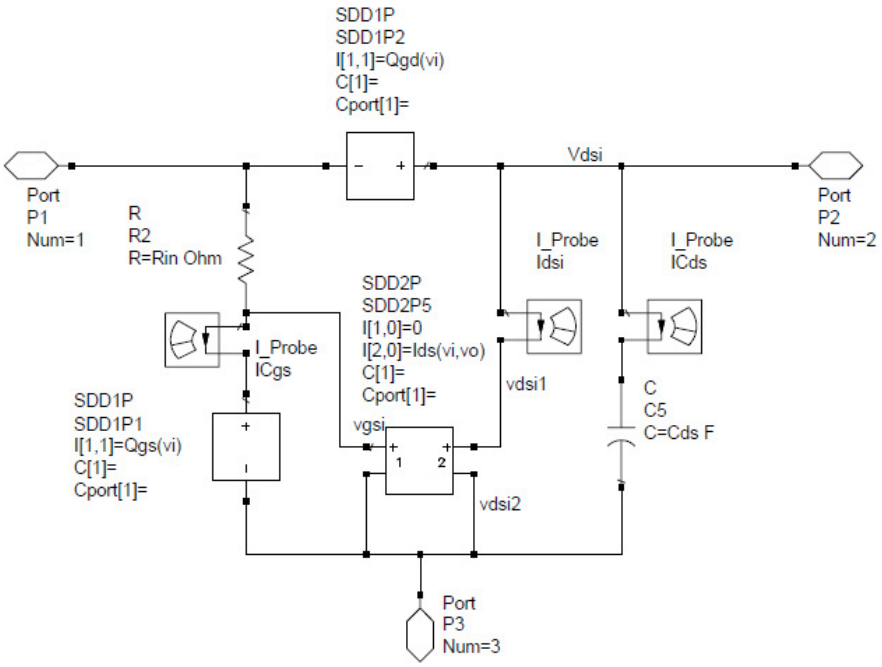


Figure 6.7: Transistor Model using SDD

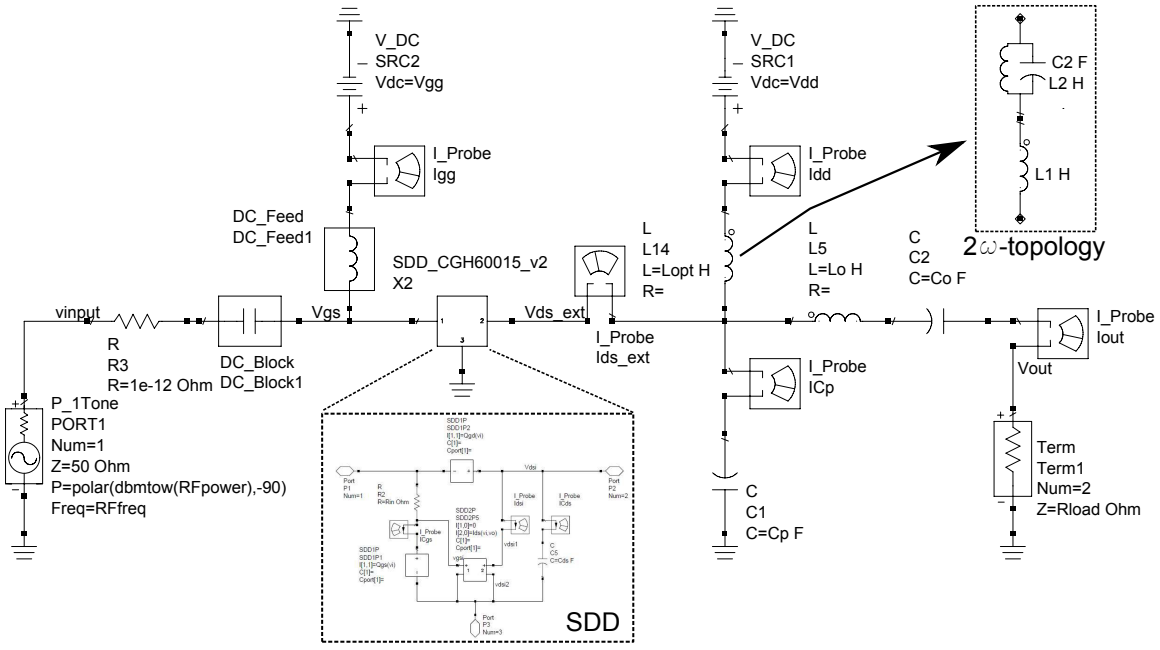


Figure 6.8: Class-E with SDD model in ADS

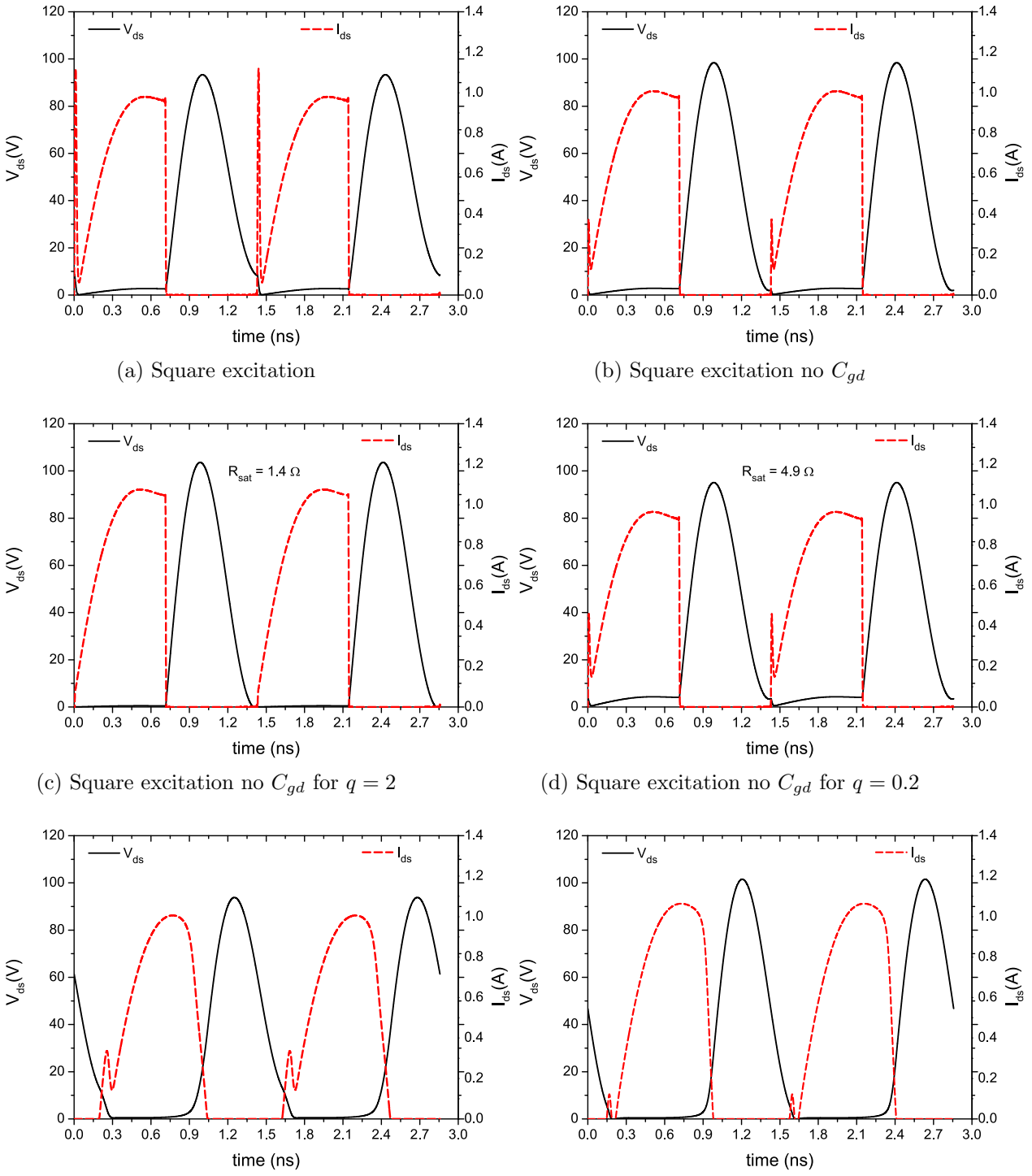
facilitate the reading of the current and voltages in each of them, as well as to be able to deactivate and activate the different circuit elements as required.

It is important to point out that the objective in this section is not to extract an extensive large-signal transistor model, but rather to generate a simplified model capable of describing transistor operation in a much better way as compared to an ideal switch. By doing so, it would be possible to gain a better insight into the active device operation in FDIC-class-E amplifiers.

6.2.2 Simulation of conventional Class-E using SDD Model

Figure 6.8 depicts the implementation of the class-E power amplifier in *Keysight Advanced Design Systems* (ADS) [99] using the SDD model. The equations for the parallel-circuit class-E [100] have been used to calculate the element values of the output network. The supply voltage $V_{dd} = 28\ V$ has been chosen in order to keep the drain peak voltage (approximately $3.5 \cdot V_{dd}$ for ideal class-E operation) well below the breakdown voltage of the CGH60015, given as $V_{BD(min)} = 120$ V. The targeted output power is $P_{out} = 10$ W and the maximum drain current is specified as $I_{DMAX} = 1.5$ A [94]. The maximum operation frequency of this topology f^E_{max} is around 1 GHz (see equations in [100]) and is 1.4 times larger than the one for the conventional class E [70].

Simulations using the SDD model were initially run at a frequency below f^E_{max} to verify proper class-E operation. Figure 6.9 shows the results at 700 MHz. Two cases were considered here, namely, when the device is driven by a square source (figures 6.9a to 6.9d) and secondly when a sinusoidal drive is used (figures 6.9e and 6.9f). Figure 6.9a depicts close-to-classical waveforms, although a large current spike is observed. According to Choi et al. [101] this current spike is caused by the feedback capacitance C_{gd}, which does not allow the drain voltage to reach zero before the transistor turns on. To verify this hypothesis, the feedback capacitance is removed from the model in figure 6.7. As can be seen in figure 6.9b, the amplitude of the spike has considerably decreased although it has not completely disappeared. Grebennikov et al. [100] has noted that a combination of non-ideal switching conditions and non-zero saturation resistance can cause a transient response of the current waveform as the one observed in figure 6.9b. In the SDD model it is possible to vary the saturation resistance by adjusting the parameter q. For $q = 0.3268$ (see table 6.2) the saturation resistance (r_{sat}) is approximately equal to 3 Ω. Figures 6.9c and 6.9d depicts the voltage and current waveforms for $r_{sat} \approx 1.4\ \Omega$ ($q = 2$) and for $r_{sat} \approx 4.9\ \Omega$ ($q = 0.2$) respectively. It is clearly seen that a low value of r_{sat} causes the spike to disappear whereas a higher value of r_{sat} enhances it. For a sinusoidal drive smoother waveforms are expected as shown by figure 6.9e. In this case the current spike, which now resemble a small bifurcation, is less pronounced and can be almost completely eliminated by removing the feedback capacitance C_{gd} as depicted in figure 6.9f. The efficiency degradation due to feedback capacitance is just about 3% points, whereas maximum efficiency of 95.7% is obtained with sinusoidal drive and no C_{gd} (for nominal $r_{sat} \approx 3\ \Omega$). The sinusoidal drive case also exhibited slightly higher output power compared to the square-signal drive, the highest being 40.5 dBm for a transistor without C_{gd}.



(a) Square excitation

(b) Square excitation no C_{gd}

(c) Square excitation no C_{gd} for $q = 2$

(d) Square excitation no C_{gd} for $q = 0.2$

(e) Sinusoidal excitation

(f) Sinusoidal excitation no C_{gd}

Figure 6.9: Current and voltages for class-E below f^E_{max} ($f = 700$ MHz)

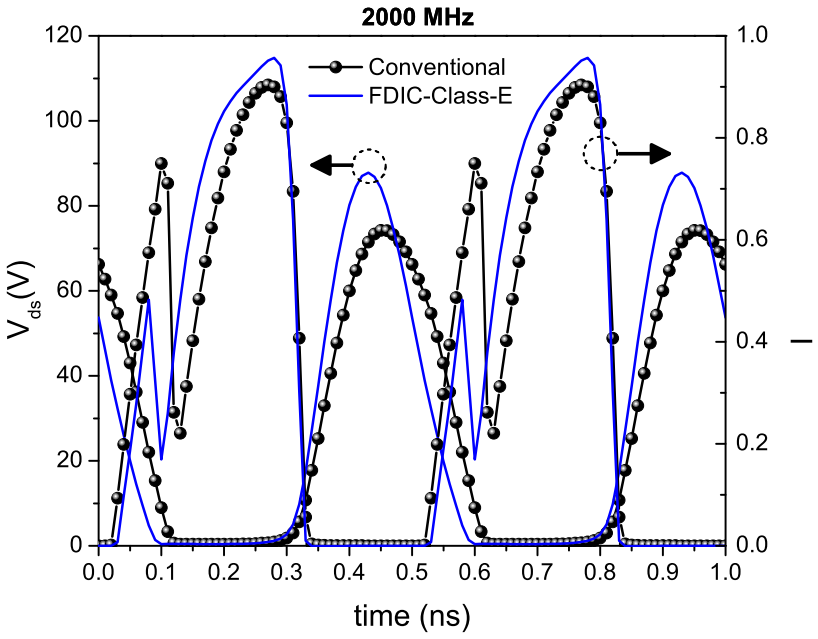
Table 6.3: Circuit parameters for 2 GHz and 3 GHz

Parameter	$F = 2$ GHz	$F = 3$ GHz
L	5.38 nH	3.58 nH
R	92.27 Ω	92.27 Ω
C	0.59 pF	0.39 pF
C_{EX}	0.33 pF	0.53 pF
α	0.56	1.35
L_1	3.08 nH	1.36 nH
L_2	0.56 nH	0.39 nH
C_2	5.70 pF	3.60 pF

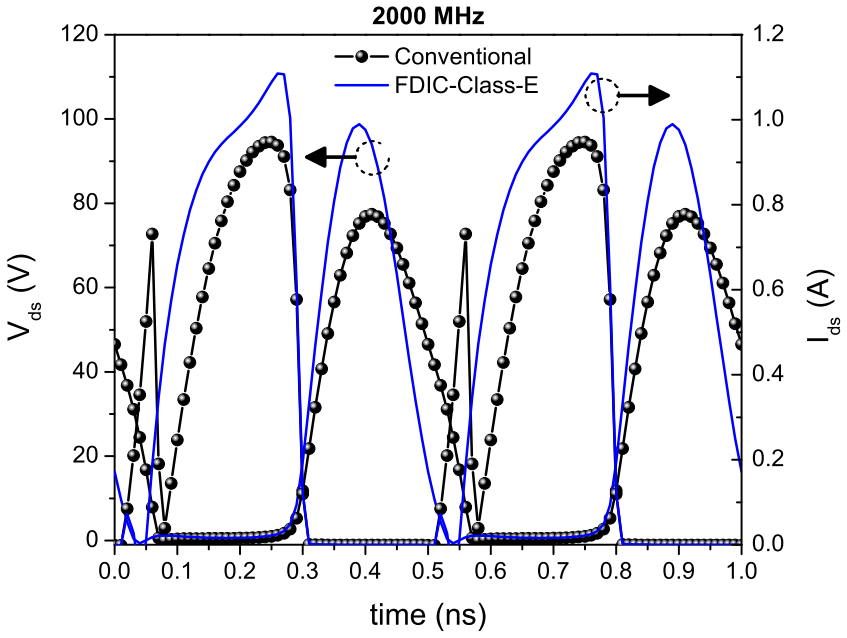
6.2.3 Simulation of FDIC-Class-E using SDD Model

In order to evaluate the performance of the FDIC-Class-E the fundamental frequency was increased as high as twice and three times f_{max}^{E}, i.e. to 2 GHz and 3 GHz respectively. The class-E topology in figure 6.8 was initially simulated using a single-valued inductor (which is calculated according to [70]) and after that using the one-resonator topology (calculated using equations (6.4) to (6.6) with $\gamma = 0.5$). Table 6.3 shows the parameter values for the selected frequencies. Inspection of the drain waveforms in figure 6.10a reveals higher peak voltage and current values for the compensated class-E. The phenomenon of drain current bifurcation as described in [97] is clearly depicted in both cases, although it is less pronounced in the FDIC-Class-E. In section 6.2.2 it was shown that a small current spike is observed in I_{ds} caused by the feedback capacitance for $f < f_{max}$. The drain current bifurcation can be seen as a magnified spike for $f > f_{max}$, caused this time not only by the feedback capacitance but also by the excess output capacitance. Simulations by Cipriani et al. [102] already display a soft-bifurcated I_{ds} but this effect is not discussed by the authors. Cripps [103] on the other hand, writes that this small peak of current prior to the main conduction corresponds to a condition where the device (acting as a switch) closes at a point of nonzero voltage. In addition to this, it seems that the spike in I_{ds} allows obtaining a better compromise between power and efficiency in class-E amplifiers [103]. As a matter of fact, the FDIC approach analyzed here is able to compensate for C_{out} minimizing the current bifurcation in class-E amplifiers operating above f_{max}. Nevertheless, switching at non-zero voltage is still observed as the effect of the feedback capacitance C_{gd} is not canceled out by the proposed FDIC approach. Figure 6.10b displays the current and voltage waveforms when removing C_{gd} from the SDD model, in this case bifurcation is not observed in the compensated PA any longer. In figure 6.11a the waveforms for 3 GHz are displayed. In this case the input power was increased from 26 dBm (used at 2 GHz) to 30 dBm, in order to be able to drive the device into saturation. This time the bifurcated current of the single-valued inductor Class-E exhibits a highly pronounced left-side "lobe". This side lobe together with a less symmetrical drain voltage (tilted toward the right), causes a higher overlap and as a consequence a higher power dissipation at the transistor drain.

Table 6.4 summarizes the performance of the conventional and of the FDIC-class-E in terms of drain efficiency and output power. The values for constant C_{gs} and C_{gd} are shown in parenthesis. A considerable improvement is obtained, especially when moving

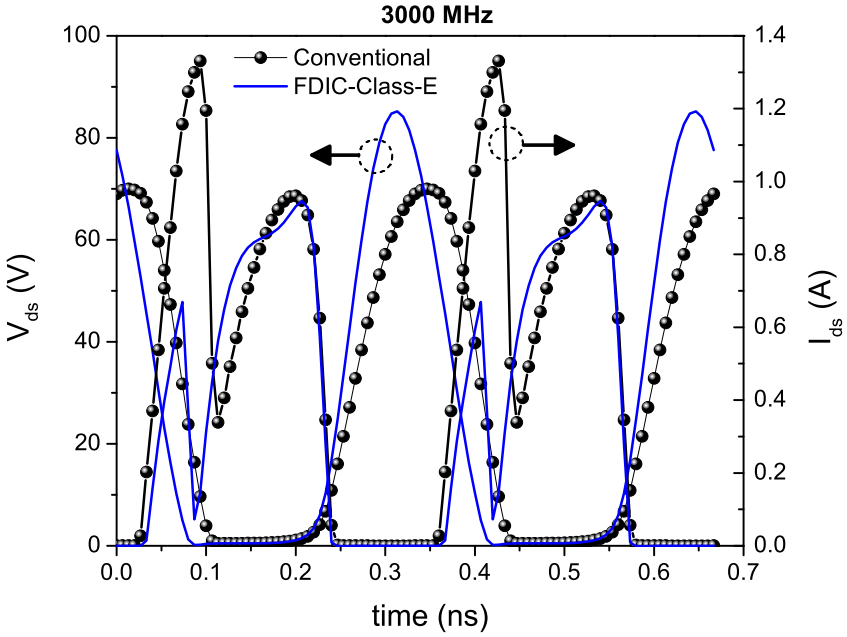


(a) Drain voltage and current

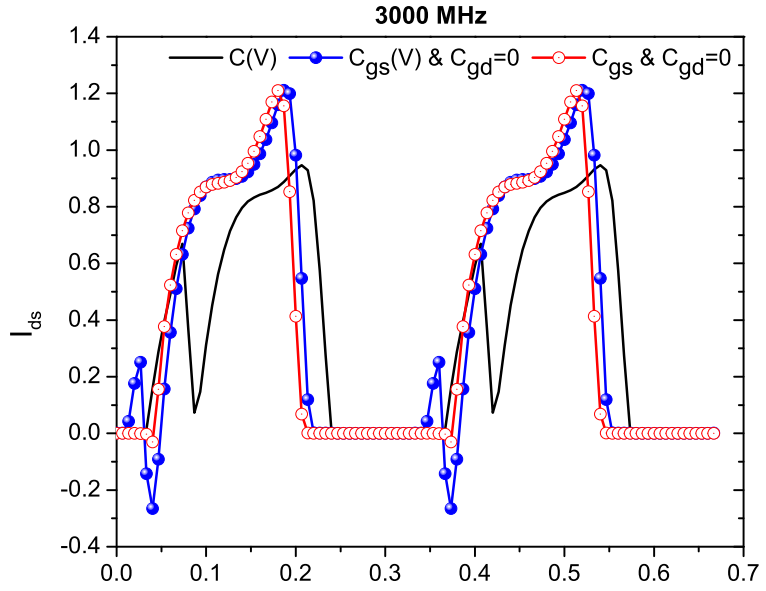


(b) Drain voltage and current for $C_{gd} = 0$

Figure 6.10: Waveforms of class-E with and without FDIC for $f = 2$ GHz



(a) Drain voltage and current



(b) [Influence of device capacitances on drain current

Figure 6.11: Waveforms of class-E with and without FDIC for $f = 3$ GHz

Table 6.4: Simulation results for 2 GHz and 3 GHz

$F = 2$ GHz	P_0 (dBm)	η (%)
Class-E	39.2(39.3[a])	82.3(90.8)
FDIC-Class-E	39.8(40.3)	95.9(96.3)
$F = 3$ GHz	**P_0 (dBm)**	**η (%)**
Class-E	38.8(38.9)	55.7(69.3)
FDIC-Class-E	39.8(40.3)	91.4(96.2)

[a] Values in parenthesis are for $C_{gd} = 0$

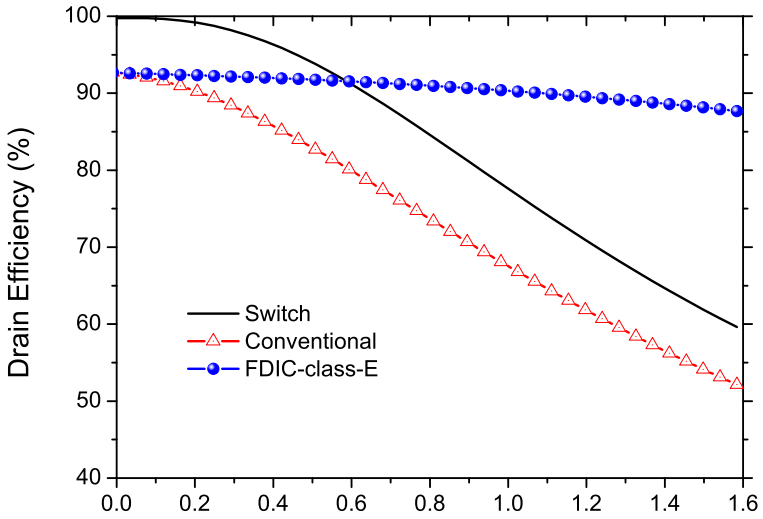
towards higher frequencies. In figure 6.11b the influence of the device capacitances is displayed. The black trace (without marks) represents the current for the FDIC-Class-E when having voltage-dependent capacitances, i.e $C_{gs}(V)$ and $C_{gd}(V)$. Removing C_{gd} from the FET equivalent circuit allows to eliminate the current bifurcation effect as depicted by the (blue) trace with filled circles, although this time a negative current jump is observed (in the classical class-E terminology this negative jump is caused by a negative voltage derivative at the turn-on time [49]). The small current jump still observed in I_{ds} can be completely removed by making C_{gs} constant.

Figure 6.12 presents the overall performance of the inductive compensation in relation to a conventional class-E operating above f_{max}. For the conventional class-E two cases are depicted, namely when using an ideal switch and when using the simplified large signal-model. It is clearly seen that the conventional class-E with the switch would predict outstanding efficiency levels, still above 80% for an excess factor of $\alpha = 0.9$, i.e. $C_{out} = 1.9 \cdot C_{opt}$. In addition to this, the output power is always above 9.4 W within the specified range for α. On the other hand, using the simplified large-signal model shows that efficiencies above 80% are only maintained up to $\alpha = 0.6$. The FDIC-Class-E on the other hand, exhibits improved efficiency and power far beyond f_{max} as compared to the conventional class-E.

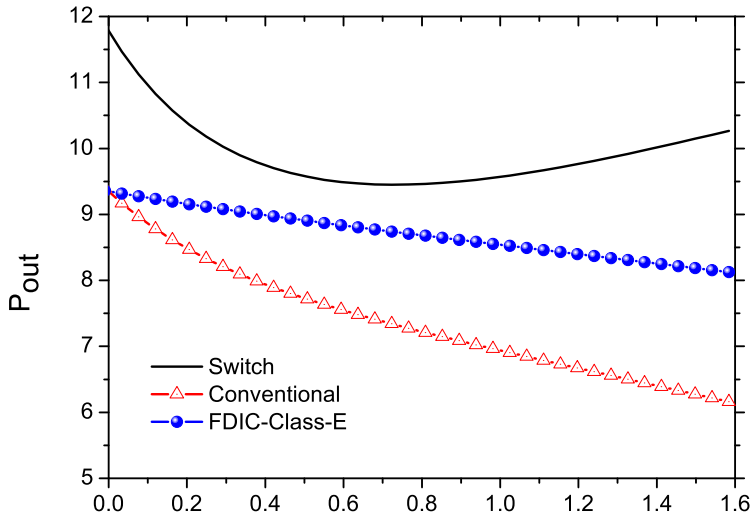
These efficiency and power plots are for fixed values of output resistance R, input impedance and input drive, whereas a square excitation was used to be able to compare with the ideal switch case. The efficiency and power of the FDIC-Class-E can be improved by increasing the output resistance R given in table 6.3 as well as by tuning the input impedance and by selecting an appropriate input power drive and biasing conditions. It is important to point out that only compensation up to the 2nd harmonic was presented in this section. This was done so since simulations performed using a double-resonator topology (C_{EX} compensation up to $3 \cdot f_0$) did not show significant improvement.

6.3 General Approach to Design FDIC-Class-E

In the previous sections a lumped element network and two equivalent transmission line topologies were presented, all of them used to implement the frequency-dependent inductor required to achieved FDIC in Class-E. In the first case the parasitics associated to discrete inductors and capacitors is the main factor limiting proper operation at microwaves. In the latter, the transmission lines of the equivalent circuit might become difficult to implement specially for an increasing excess factor α. A general design approach is evaluated in



(a) Efficiency vs. Excess Factor α



(b) Power vs. Excess Factor α

Figure 6.12: Comparison of PC Class-E with and without inductive compensation

this section, which offers the advantage of not relaying on the topologies presented previously and that is more suitable at microwave frequencies, where the implementation using transmission lines is a more common practice.

6.3.1 Impedances for FDIC and Class-E Network

The driving-point impedance seen from the switch-C_{out} combination as a function of the excess factor α is given by:

$$Z_{in}(\omega_0) = R \cdot \frac{1 + j1.366(1 + 0.5\alpha)}{1 + 1.866(1 + 0.5\alpha)^2} \tag{6.10}$$

and at the harmonics

$$\begin{aligned} Z_{in}(n\omega_0) &= j \cdot \frac{n\omega_0 L}{1 + 0.5\alpha n^2} \\ &= j \cdot X_n, \ n = 2, 3... \end{aligned} \tag{6.11}$$

These expressions were introduced in chapter 5 but were not further evaluated by the author. In this section these equations are used together with the simplified large-signal model to evaluate the general concept of FDIC-Class-E.

Since the goal has now been reduced to synthesize impedances according to equations (6.10) and (6.11) it is possible to use conventional class-E topologies as for instance the one in figure 6.13.

It is important to mention here that in previous approaches Fourier decomposition of the ideal current and voltage waveforms of the class-E amplifier have been used to calculate the required impedances seen from the switch plane [75] [102]. As has been presented here and also by others, class-E waveforms are far from classical at microwaves, rendering such an approach as unpractical.

The output network chosen here and depicted in figure 6.13 employs six transmission lines (another possible topology is the 4-line network described in [104] and [105]) three of them having a fixed electrical length at the fundamental frequency, namely, $\theta_3 = 90°$, $\theta_2 = 30°$ and $\theta_6 = 30°$. It is worth mentioning that for the sake of completeness, the topology selected here compensates the excess capacitance up to the third harmonic, even though the analysis of the FDIC in section 6.2.3 only considered compensation up to the 2nd harmonic.

At the fundamental frequency f_0 the line Z_3 connected to the DC supply does not contribute to the input impedance of the network since its length is $\lambda/4$, causing an open circuit to appear at its input. Further, at $f = 2 \cdot f_0$ this line becomes $\lambda/2$ therefore short circuiting the components to the right of the line with impedance Z_1. For $f = 3 \cdot f_0$ the open-circuited shunt line of impedance Z_6 is $\lambda/4$ long, causing a short circuit to appear at the input of this line. The short circuit is transformed into an open circuit by line Z_2, leaving only lines Z_1 and Z_4 as part of the equivalent circuit (the line Z_3 is $3\lambda/4$ and can be removed). The equivalent load networks seen by the device output at the fundamental and harmonics are shown in figure 6.14. For the sake of simplicity and without loss of generality it will be assumed that all open stubs have the same impedance, namely $Z_4 = Z_5 = Z_6 = Z_0$. The input impedances presented by the network at the harmonics, i.e. $Z_{in}(2\omega_0)$ and $Z_{in}(3\omega_0)$,

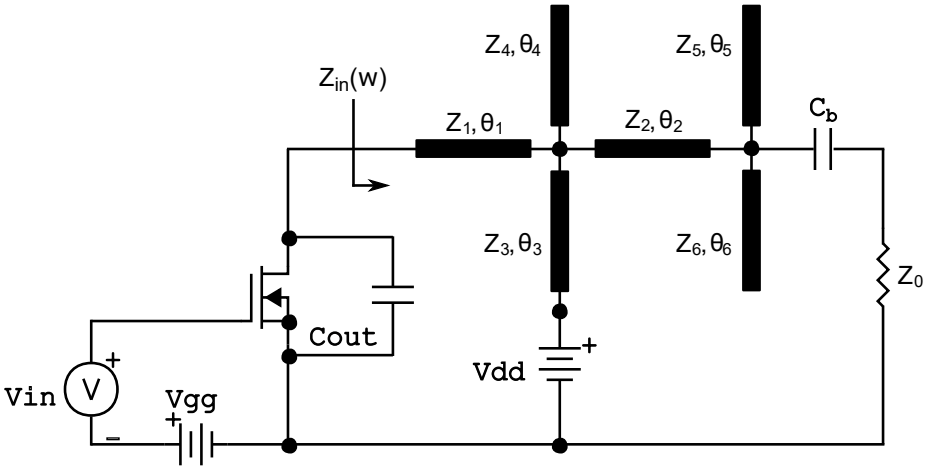


Figure 6.13: Generalized transmission Line Class-E PA

are given by equations (6.12) and (6.13) respectively. The expressions on the left side are equal to the reactance obtained from equation (6.11) for $n = 2$ and $n = 3$ respectively,

$$jZ_1\tan(2\theta_1) = jX_2 \tag{6.12}$$

$$-jZ_1 \cdot \frac{-Z_4\cot(3\theta_1) + Z_1\tan(3\theta_1)}{Z_1 + Z_4\cot(3\theta_4)\tan(3\theta_1)} = jX_3. \tag{6.13}$$

Hence, if for instance Z_1 is known, the electrical lengths θ_1 and θ_4 can be calculated from (6.12) and (6.13) respectively. In this case two quantities are yet to be determined, namely Z_2 and θ_5. The admittance seen at the fundamental frequency from plane g (see figure 6.14a) when terminating the left port of the network with $Z^*_{in}(\omega_0)$ (complex conjugate of $Z_{in}(\omega_0)$) is given by

$$Y_g = j\frac{\tan(\theta_5)}{Z_5} + j\frac{\tan(\theta_6)}{Z_6} + Y_d \tag{6.14}$$

with Y_d being the admittance seen from plane d towards the device and defined as follows

$$Y_d = \frac{1}{Z_2} \cdot \frac{Z_2 + jZ_c\tan(\theta_2)}{Z_c + jZ_2\tan(\theta_2)}. \tag{6.15}$$

In equation (6.15) Z_c represents once more the impedance seen from plane c.
The admittance Y_g must fulfill the following two conditions:

$$\mathrm{Re}(Y_g) = \frac{1}{Z_0} \tag{6.16}$$

$$\mathrm{Im}(Y_g) = 0. \tag{6.17}$$

Applying the first condition to (6.14) results in the following quadratic equation, which can be solved to obtain Z_2

$$\tan^2(\theta_2) \cdot Z_2^2 + 2b_c\tan(\theta_2) \cdot Z_2 + (\mid Z_c \mid^2 - Z_0 a_c \sec^2(\theta_2)) = 0, \tag{6.18}$$

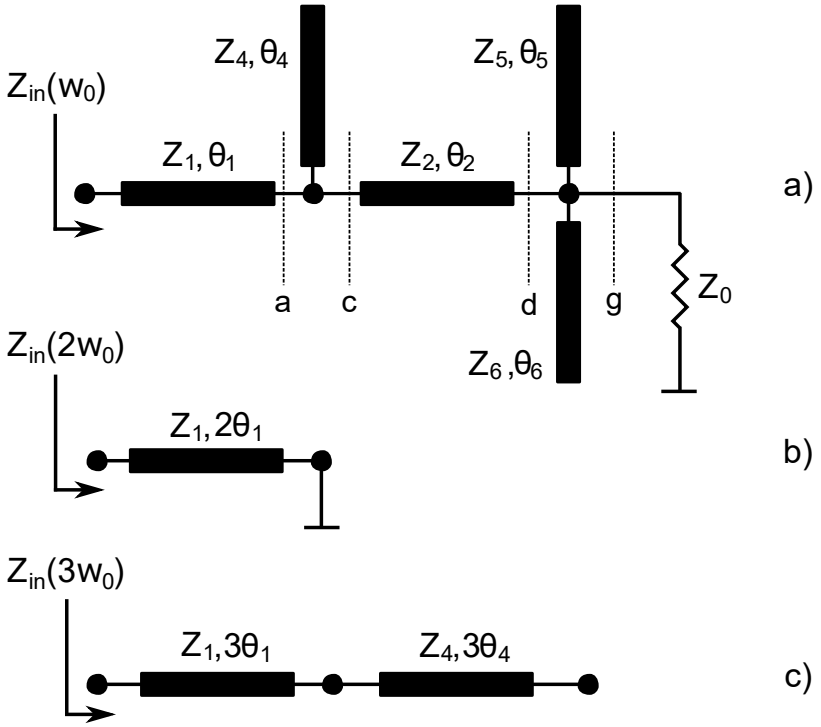


Figure 6.14: Load networks seen by device output at a) f_0 b) $2 \cdot f_0$ c) $3 \cdot f_0$

where a_c and b_c represent the real and imaginary parts of the impedance Z_c, i.e. $Z_c = a_c + jb_c$.

In addition to this, the $2nd$ condition can be applied to the admittance Y_g to obtain the electrical length θ_5 according to equation (6.19)

$$\tan(\theta_5) = -\tan(\theta_6) - Z_5 \cdot \mathrm{Im}(Y_d) \tag{6.19}$$

with

$$\mathrm{Im}(Y_d) = \frac{1}{Z_2} \cdot \frac{(\mid Z_c \mid^2 - Z_2^2)\tan(\theta_2) - Z_2 b_c(1 - \tan^2(\theta_2))}{\tan^2(\theta_2)Z_2^2 + 2b_c\tan(\theta_2)Z_2 + \mid Z_c \mid^2}. \tag{6.20}$$

The required impedances at the fundamental and harmonics can be calculated using equations (6.10) and (6.11) respectively. Those values are shown for 2 GHz in table 6.5. The excess factor used in the calculation is $\alpha = 0.56$ (refer to table 6.3).

Assuming the impedance Z_1 to be the independent variable and using equations (6.12) to (6.20), the values for the yet undetermined electrical lengths and line impedances can be obtained as a function of Z_1. The results are shown in figure 6.15. Table 6.5 summarizes the results for $Z_1 = 45\ \Omega$.

6.3.2 Simulations using SDD and Commercial Model

Simulations were now performed using the simplified large-signal model with the transmission line output network from the previous section. Figure 6.16a compares the drain waveforms for this case against the class-E using the one-resonator topology. As can be

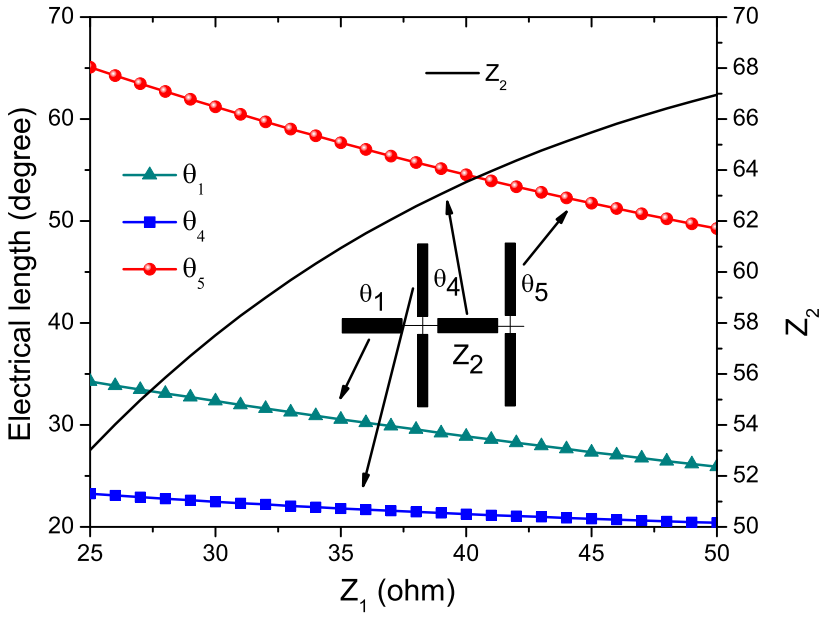


Figure 6.15: Network parameters as a function of Z_1

Table 6.5: Parameters Generalized Network

Parameter	$F = 2$ **GHz**
$Z_{in}(\omega_0)$	$(22.7 + j39.7)\ \Omega$
$Z_{in}(2\omega_0)$	$j63.5\ \Omega$
$Z_{in}(3\omega_0)$	$j57.3\ \Omega$
Z_1	$45\ \Omega$
Z_2	$65.5\ \Omega$
$Z_4 ... Z_6$	$50\ \Omega$
θ_1	$27.3°$
θ_2=θ_6	$30°$
θ_3	$90°$
θ_4	$20.8°$
θ_5	$51.7°$

seen from the figure the waveforms in both cases are quite similar although not identical. The small differences arise due to the different impedances seen by the device at the second and third harmonic in each of the cases. Responsible for this is equation (6.11), which was derived without taking into account the finite Q factor of the series resonator in the class-E circuit. Nevertheless, the efficiency of the transmission line FDIC-Class-E is still high achieving 91%, representing a 5.1% decrease relative to the lumped version's efficiency of 95.9%. In both cases the output power is 39.8 dBm.

Further, the simplified large-signal model was replaced by the proprietary GaN HEMT model of the CGH60015D. The proprietary model allows reading of the current and voltages only at the external terminals of the device. Figure 6.16b displays the drain voltage and current for the simplified (i.e. SDD) and for the proprietary model respectively. Good agreement is observed in this case. The output power of the class-E with transmission lines drops to 39.65 dBm whereas the efficiency obtained is now equal to 85.4%.

The next simulation step requires replacing the die model by the packaged device model. First of all the impedance provided by the output network need to be corrected by considering the characteristics of the package. For this purpose the ceramic housing of the device was removed and a laser scanning microscope used to obtain the dimensions and heights of different parts within the package. These parameters were then used to create the 3D model in figure 6.17a, which allowed performing electromagnetic (EM) simulations. The substrate used in the simulation was alumina, a widely used ceramic material in RF transistor packages [39]. The equivalent circuit of the package is shown in figure 6.17b.

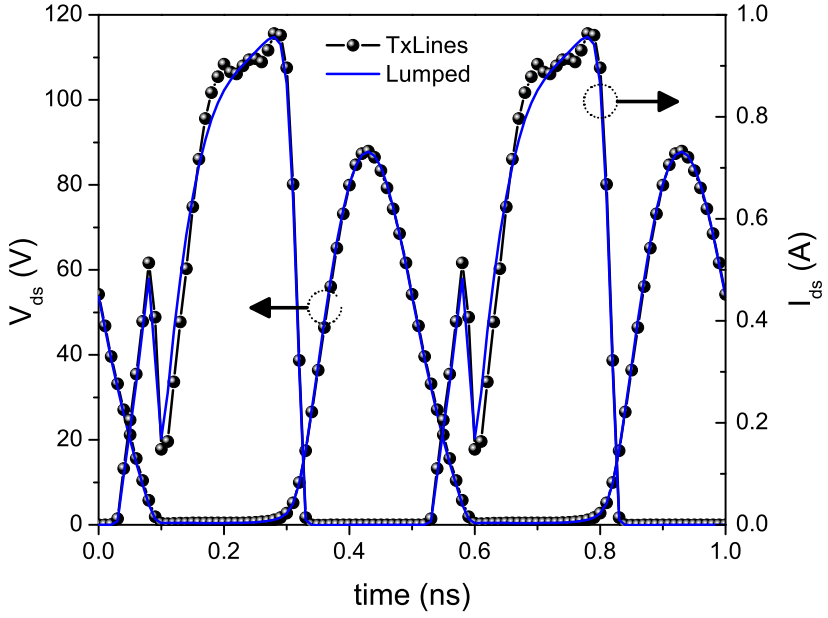
Equation (6.21) can now be used to re-calculate the impedance to be seen from the lead plane knowing the impedance at the C_{OUT} plane

$$\Gamma_{lead}(f) = \frac{S_{11}(f) - \Gamma_{out}(f)}{|S(f)| - \Gamma_{out}(f) \cdot S_{22}(f)} \tag{6.21}$$

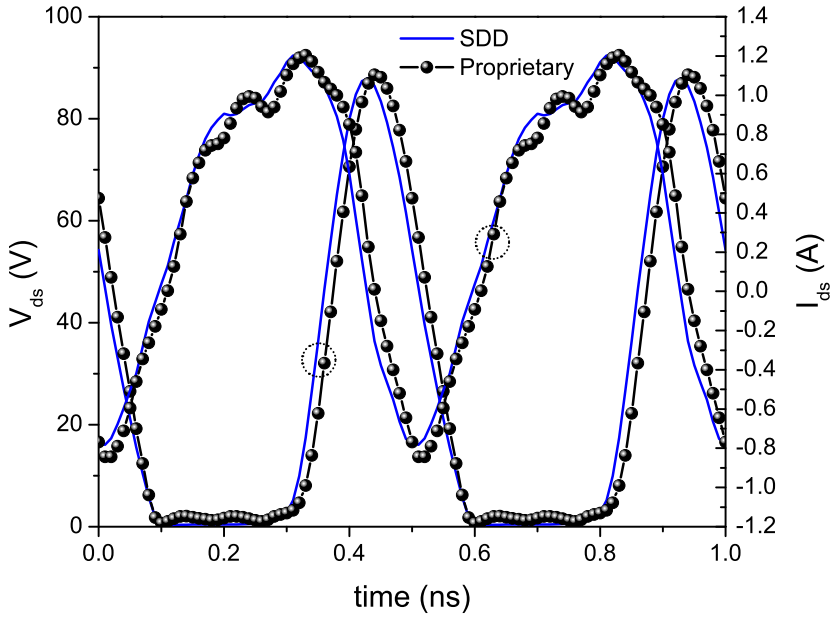
where S_{ij} denotes the S-parameters of the network between the C_{OUT} plane and the lead plane, $|S|$ is the determinant of the S-matrix, and Γ_{out} the desired reflection coefficient at the C_{OUT} plane. The impedances at both reference planes up to the 3rd harmonic are shown in table 6.6.

As explained previously, the impedance at the 3rd harmonic was also taken into account to provide a more general and complete solution, although this impedance was not originally considered in the theoretical considerations of the FDIC network. The impedance seen from the gate terminal was again obtained from S_{11}^*. Initial simulations using the packaged device show a drain efficiency of 81.6% and an output power of 39.8 dBm. In this case no additional optimization has been carried out in the simulation and the output network component values have been obtained solely by using the class-E formulas for FDIC. Nevertheless, very good efficiency performance is still displayed. The general design procedure for the class-E power amplifier is as follows:

1. Specify f_0, V_{DD} and P_{OUT},
2. Calculate the values of the parallel-circuit class-E output network elements using the equations in [100],



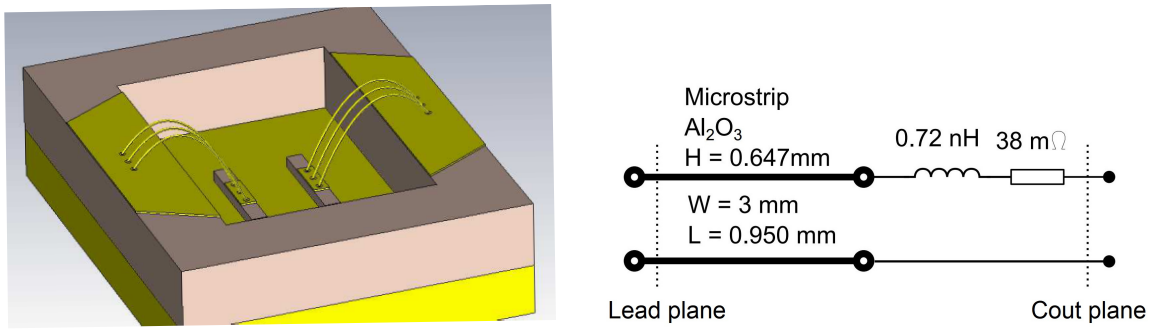
(a) Class-E waveforms using SDD and transmission lines



(b) External waveforms of simplified and of proprietary model

Figure 6.16: Waveforms of the FDIC-Class-E when using transmission lines

3. Calculate C_{EX} and α,
4. Use (6.10) to obtain $Z_{in}(\omega_0, \alpha)$,
5. Use (6.11) to obtain $Z_{in}(n\omega_0, \alpha)$,
6. Re-calculate $Z_{in}(\omega_0, \alpha)$ and $Z_{in}(n\omega_0, \alpha)$ using (6.21) to take into account the package effect,
7. Calculate the 6-line output network using (6.12) to (6.20),
8. Simulation-based optimization using transistor model.



(a) 3D model of transistor package

(b) Extracted package model for CGH40010F

Figure 6.17: Models of transistor package

Table 6.6: Impedances at C_{out} and Lead planes

Freq (GHz)	$\mathbf{Z_{Cout}}$ **(Ω)**	$\mathbf{Z_{lead}}$ **(Ω)**
2	$(22.7 + j39.7)$	$(16.37 + j26.11)$
4	$j63.5$	$j26.86$
6	$j57.3$	$j15.25$

6.4 Implementation and Experimental Results

In this section, a design example is given to verify the validity of the approach introduced in the preceding sections. An FDIC-Class-E prototype is implemented using the packaged GaN HEMT CGH40010F from Wolfspeed [106]. The selected operating frequency is 2 GHz and the targeted output power is 40 dBm using a drain supply voltage equal to 28 V. The calculated excess factor in this case is $\alpha \approx 0.6$ (i.e. the transistor output capacitance is approximately 60% higher than the optimum value). The predicted drain efficiency of the FDIC-Class-E in this case is around 96% according to table 6.4. It is important to remember that this prediction is based on a simplified transistor model without package and does not take into account losses in the circuit. The circuit is fabricated on Rogers

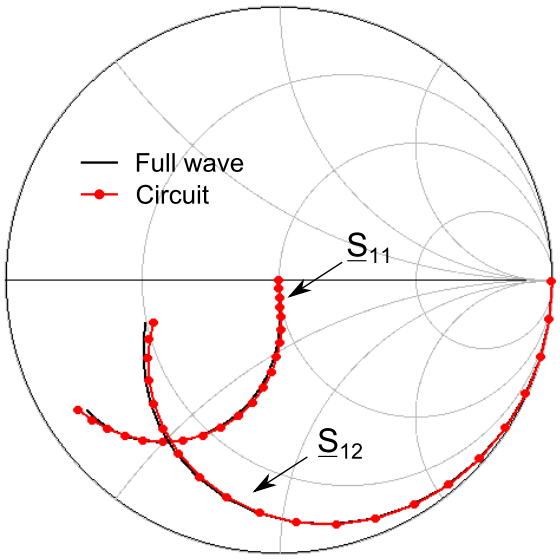


Figure 6.18: Full wave and equivalent circuit simulation of package

4350B [92] with a thickness of 20 mils and the dielectric constant of 3.66. A brass jig is used to mount the circuit board and SMA connectors used to interface the power amplifier. A cut out was made in the jig to introduce the transistor flange allowing the transistor leads to rest on top of the PCB traces for easy soldering. Multi-pin connectors were used at the gate and drain DC paths for connection to the power supply. The fabricated prototype can be seen in figure 6.19.

The six-line output matching network composed of lines Z_1 to Z_6 is shown at the right side of the packaged device. The input network was designed to provide a complex-conjugate matching at the frequency of operation as well as a low negative reactance termination at the second harmonic. The three transmission lines used to control the input harmonic termination are marked with 2nd HARM in figure 6.19. To guarantee stability two networks

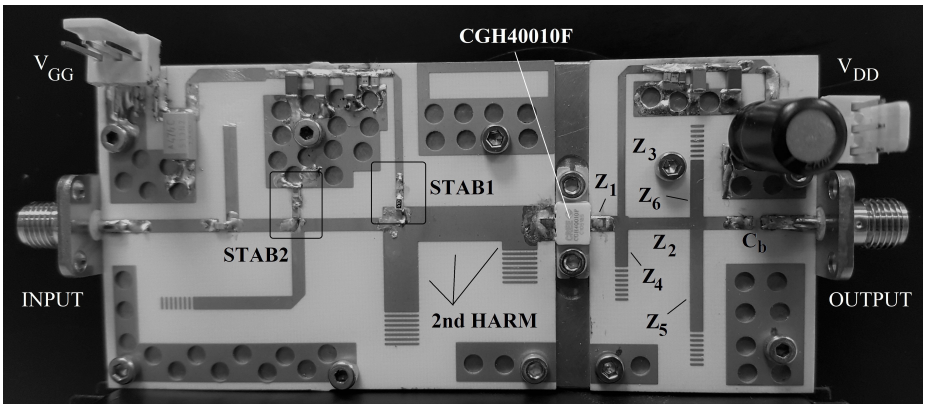


Figure 6.19: Implemented FDIC-Class-E Power Amplifier

were used. The first one is composed of a 47 Ω resistor close to the transistor gate and in series with the DC bias line. In addition to this, a shunt network composed of a 220 Ω resistor in series with a 6.8 pF capacitor was used. In figure 6.19 they have been designated as STAB1 and STAB2 respectively. The measured and simulated small-signal response of the proposed amplifier can be seen in figure 6.20.

Further the large-signal performance of the amplifier was characterized. The test setup consisted of the vector signal analyzer N5182A, an in-house designed broadband driver stage, a 30 dB attenuator, the signal analyzer N9020A and the 4-channel power supply HMP4040 from Rohde&Schwarz. The simulated results show that the PA delivers a peak power of 40.2 dBm, a peak drain efficiency of 82% and a peak PAE of 78.9% at 2 GHz. The output power, gain and efficiency of the prototype are shown in figure 6.21. The PA achieves an output power of 40.1 dBm with a drain efficiency of 77.4%, a PAE of 74.5% and a power gain of 14.3 dB at 2 GHz (figure 6.21a). On the other hand, the simulation results show a maximum drain efficiency of 82%, with PAE of 78.9% and output power of 40.2 dBm. Additional measurements revealed that higher efficiency can be obtained at a slightly lower frequency, namely, at 1.96 GHz.

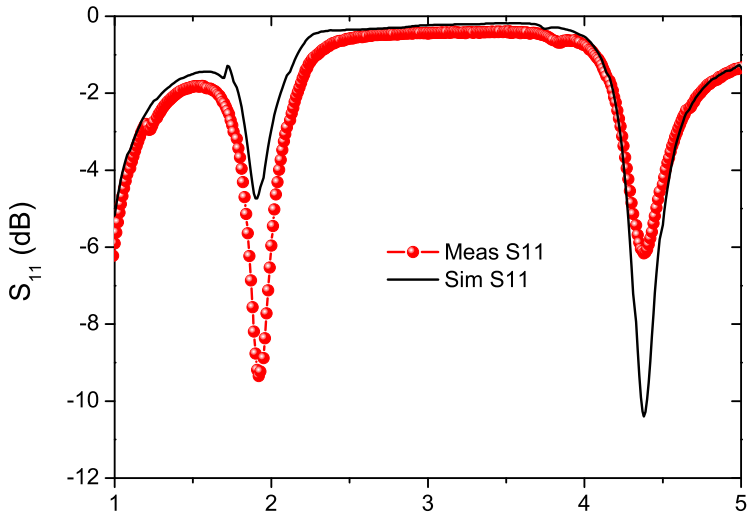
The results of the FDIC-Class-E PA shown in figure 6.21b demonstrate an output power of 40.1 dBm with a drain efficiency of 80.3%, a PAE of 76.3% and power gain of 13.1 dB at 1.96 GHz. In contrast, the simulation shows a maximum drain efficiency of 77.5 %.

Frequency deviations, which can be attributed to fabrication tolerances and large-signal model inaccuracy among others, are not rare and have been reported by other authors. Mustazar [107], for instance, observed a shift in the frequency for peak efficiency in his class-F PA design (using the same GaN HEMT device) from 2 GHz to 1.95 GHz. Mugisho et al. [108] reports even a larger deviation (close to 9%) in his class-E PA, namely from 1.5 GHz to 1.37 GHz. Although this issue was not further investigated, a combination of tolerances associated with the board as well as with the transistor and passive components, might be responsible for the observed deviation. As a matter of fact, a quick simulation shows that for instance, drain bypass capacitor placement inaccuracies of 0.5 mm, causes a shift of 10 MHz on the location of the efficiency maximum.

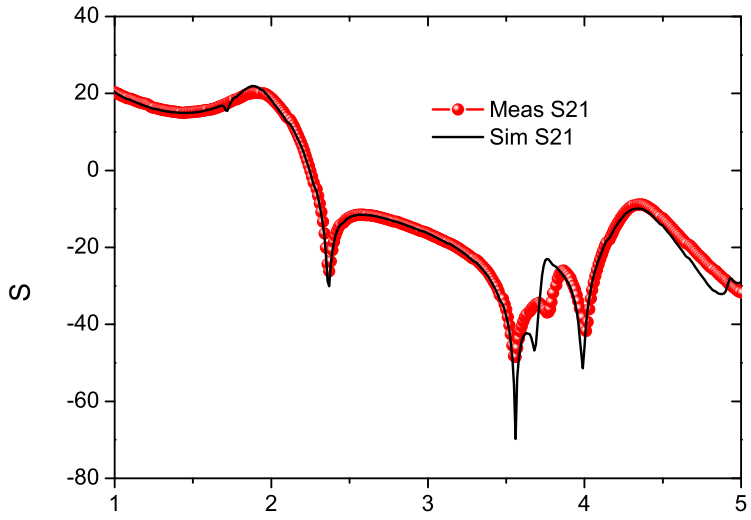
In table 6.7 a summary of selected highly efficiency power amplifiers is presented. Common to all of them is the use of the same GaN HEMT device and comparable operating frequency.

Table 6.7: Performance summary of various high-efficiency power amplifiers

PA Class	P_0 (dBm)	η (%)	f_0 (GHz)	V_{DD} (V)	Ref
Class E	40.1	77.5	2.80	28	[13]
Class E	40.2	77.5	2.90	28	[14]
PC-Class E/F_3	40.4	83.9	2.60	28	[91]
Class E/F_3	40.0	76.0	2.14	30	[105]
Class E	39.8	90.2	1.37	28	[108]
Class E	40.0	65.0	1.95	28	[109]
Saturated PA	41.0	78.0	2.66	30	[110]
Class F	40.8	77.8	2.50	25	[111]
FDIC-Class E	40.1	80.3	1.96	28	This work

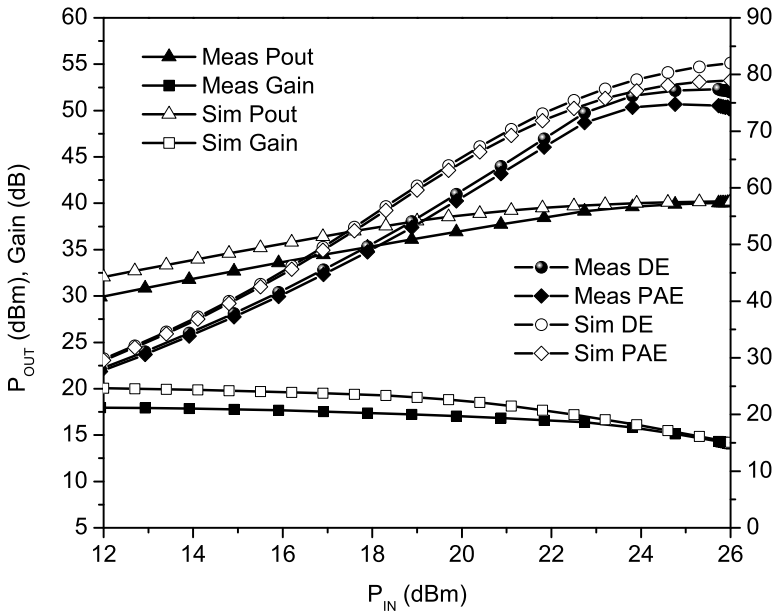


(a) Measured and simulated S_{11}

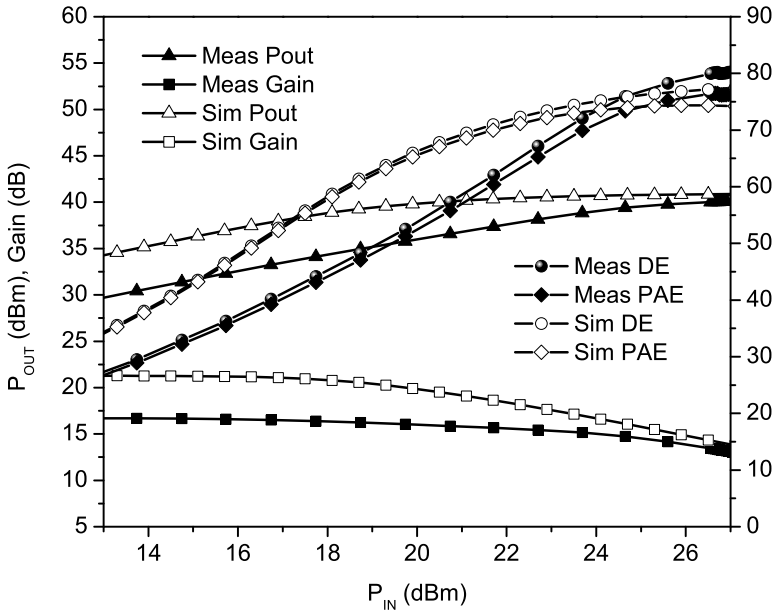


(b) Measured and Simulated S_{21}

Figure 6.20: Small-signal performance of power amplifier



(a) Measurements and simulations at 2 GHz



(b) Measurements and simulations at 1.96 GHz

Figure 6.21: Large-signal performance of power amplifier

7 Power Amplifiers for Hyperthermia Systems

This chapter reviews the topic of radio frequency hyperthermia and the requirements of power amplifiers used for this application. Existing literature is analyzed to understand the basic components of a hyperthermia system and few examples of commercially available systems are given to show typical operating parameters, such as frequency and output power. The design of a 100 W amplifier for regional hyperthermia operating at 70 MHz is presented. In this section, design considerations such as required drive power and gain, losses in the amplifying path, etc. are evaluated. The design of the 100 W module itself is of low novelty, but it allows a first contact with the hyperthermia world and to define requirements for the next design. The final section of this chapter presents the design of a 250 W amplifier as successor of the pre-designed 100 W module. The existence of a large-signal model for the high power device used in the $2nd$ amplifier, opens new possibilities for design exploration. In this respect, two design approaches are compared: the first one makes use of the classical class-E design equations to create a first design, which is evaluated via simulation. The second approach is based on load-pull simulations. Intrinsic waveforms (i.e., at the current source plane) are evaluated to understand the high-efficiency mode of operation of the PA. The implementation of the 250 W prototype is also presented. At the end, RF heating experiments using an agar phantom are performed to evaluate the capability of the PA to deliver enough power under close-to-real conditions.

7.1 Overview of Radio Frequency Hyperthermia

Radio frequency (RF) hyperthermia is a medical treatment in which cancerous tissue is exposed to high temperatures (typically 42°C to 43°C) to damage and kill cancer cells. The treatment is based on the fact that the healthy cells withstand temperatures up to 45°C while the cancer cells do not survive temperatures over 41°C [112].

The heating of tumor tissue has a cell killing (cytotoxic) effect. However, the cytotoxic effect is small at temperatures below 45°C. Therefore, hyperthermia is always clinically combined with either radiotherapy or chemotherapy. The application of hyperthermia has been proven to increase the therapeutic effect of both radiotherapy and chemotherapy. The effect of hyperthermia is strongly dependent on the achieved tumor temperatures and heating time. Preclinical research has shown that the cell-killing effect doubles every centigrade, e.g., 1 hour at 42°C is equivalent to half an hour at 43°C. Hypoxic tumors, i.e., tumors with a low level of oxygen, are more resistant to ionizing radiation than well-oxygenated tumors, while hyperthermia is particularly effective in hypoxic tumors [113]. RF and microwave hyperthermia can be classified in different clinical modes according to the medical indication. For instance, the term *Local Hyperthemia* is used when the treatment is used for super-

ficial malignant melanoma lessions and lymph node metastases of head and neck tumors. *Regional Hyperthemia* is indicated for cervical carcinoma, bladder carcinoma, prostate carcinome, etc. The way in which electromagnetic (EM) energy is applied might vary with the medical indication. In *Thermoablation* laser applicators or RF electrodes of few millimeters are employed. In *Interstitial Hyperthermia* an array of antennas or electrodes is implanted in inaccessible tumors, which might be located in deep or superficial tissues. A detailed discussion on the different clinical modes of RF thermotherapie can be found in [113].

An RF hypertermia system is usually composed of an RF source, a coaxial transmission lines capable of transporting the requested power, an applicator, thermometers and a control unit, which adjusts the output power of the source in order to obtain and keep constant the desired temperature in the treated tissue. The diagram of a general hyperthermia system can be seen in figure 7.1 [114]. A phased array of applicators or antennas can be used to steer and focus the EM energy towards the tumor. In addition to this, a water bolus is inserted between the patient and the applicator to obtain heat uniformity, cooling the tissue surface to minimize thermal hot spots as well as to achieve impedance matching between the RF source and the biological tissue [114, 115].

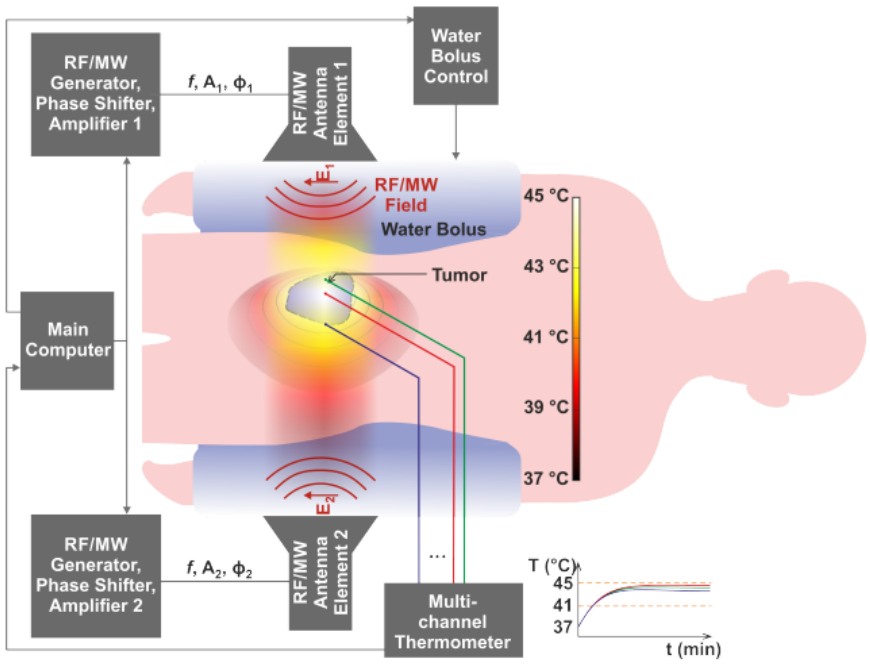


Figure 7.1: General block diagram of a hyperthermia system [114]

7.1.1 Power Amplifiers for RF Hyperthermia

One of the main blocks in the hyperthermia system is the RF source, which is composed of an RF generator or a frequency synthesizer that provides a clean (i.e. with low-level harmonic content) reference sinusoidal signal. The output of the generator (in the milliwatt range)

needs to be amplified to provide significant RF power to the applicators. A more detailed block diagram of a multi-channel hyperthermia system is depicted in figure 7.2. In multi-channel systems, the magnitude and phase of each path can be controlled and independently set by the system operator according to a specific treatment planning. As shown in the figure the system includes directional couplers to measure the power out of the amplifiers as well as the reflected power from the applicators, phase shifters, data acquisition units (DAQ), etc. Although a divider unit after the pre-amplifier can be used to provide N paths as indicated in figure 7.2, an alternative approach might use a generator with N outputs, each of the outputs providing magnitude and phase adjustable signals, connected to path pre-amplifiers and path power amplifiers (see for instance [116]).

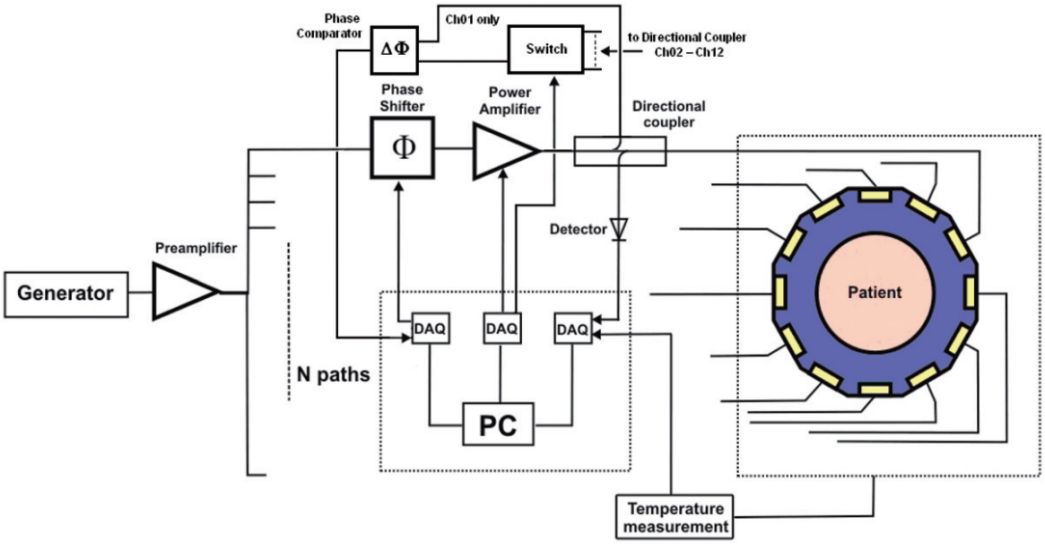


Figure 7.2: Block diagram of HT system showing power amplifier according to [15]

Wust et. al [117] mention some of the requirements to be fulfilled by power amplifiers used in RF hyperthermia systems, namely: sufficient output power level (> 100 W), broadband operation, high efficiency, high linearity, high stability, low cost and long-term reliability. The output power will depend not only on the clinical mode (type and location of tumor) but also on the number of channels. Available systems deliver as low as 60 W up to a maximum of 500 W per channel. The application dictates once more the frequency of operation, superficial tumors are heated with microwave antennas in the range of $(443 - 2450)$ MHz and deep-seated tumors with RF antennas in the range of $(70 - 150)$ MHz [118]. The PA can be designed to operate at a single frequency or to cover a pre-defined range. Table 7.1 presents a summary of few commerial hyperthermia systems.

7.2 Design of 100 W Amplifier for Regional Hyperthermia

This section presents the design of a power amplifier to be used in *regional* hyperthermia experiments, i.e., for the case of deep seated tumors, extending to more than 4 cm from the skin surface [118]. The power amplifier is required to operate at 70 MHz and to deliver an

Table 7.1: Commercial RF/MW Hyperthermia Systems

System	Channels	P_{out}/channel	$Freq$(MHz)	Vendor	Ref
BSD-500	8	60	915	Pyrexar	[119]
BSD-2000B	4	325	75 – 140	Pyrexar	[119]
BSD-2000-3D	12	135	75 – 140	Pyrexar	[119]
BSD-2000-3D/MR	12	135	100	Pyrexar	[119]
ALBA 4D	4	500	70	Alba	[120]
ALBA ON 4000D	12[a]	200	434	Alba	[121]

[a] This customized solution with 12 channels was designed to support the HYPERcollar system [122]

output power between (50 – 100) W, to a load composed of an applicator connected to an agar phantom (emulating a 1-channel system). Details on the experiments performed with this power amplifier at the Institute of Biomedical Engineering in Kladno can be found in [114].

7.2.1 Design considerations and Driver requirements

The amplifier for the initial experiments should deliver at least 50 W operating at 70 MHz [114]. In addition to this, high gain is required to amplify the output signal of the direct digital synthesizer[1] (DDS) circuit. Figure 7.3 shows the spreadsheet for the calculation of power and gain for the 100 W use case. Following assumptions were made in the calculation: a) the length of the coaxial cable between the coupler and the applicator is equal to 3 m, b) there is no additional component (e.g. a Balun) between the cable and the applicator, c) the applicator has a return loss (RL) equal to 15 dB and d) the mismatch loss between the driver and the high-power amplifier (HPA) is negligible.

	RF Generator	Driver	HPA	Coupler	Cable	Balun	Antenna	
Power (W)	2,00E-04	1	100	99,31	91,62	91,62	88,72	Total
Power (dBm)	-7	30,00	50,00	49,97	49,62	49,62	49,48	49,48
Gain (dB)		37	20	-0,03	-0,35	0	-0,14	56,48
P/N	AD9959	NPTB00004	MRF101AN	Pulsar C40-21-481	H+S Enviroflex 400, 50 Ohm		Applicator	
Pmax (W)		4	100					

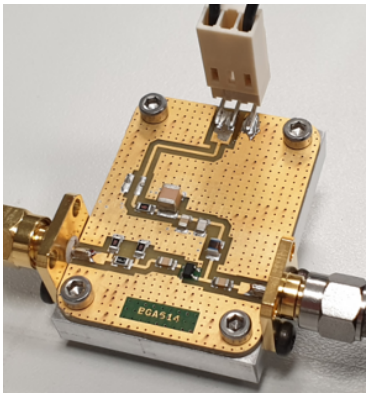
Figure 7.3: Spreadsheet to calculate power and gain of 100 W use case

The "Power (W)" row shows the power at the output of each component with the exception of the antenna or applicator, in which case, the power reading must be interpreted as the input power to the antenna minus the mismatch loss. As can be seen in the spreadsheet, the output of the DDS is −7 dBm [124], which needs to be amplified by the driver and finally by the PA. The 20 dB gain of the HPA is a conservative assumption based on

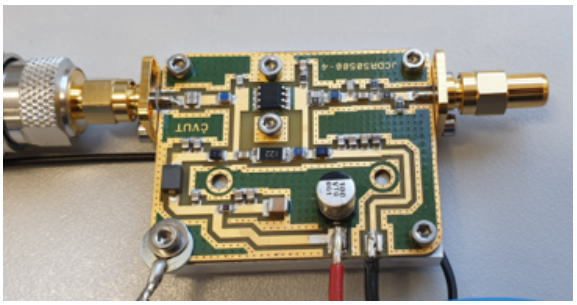
[1] DDS is a method of producing an analog waveform by generating a time-varying signal in digital form and then performing digital-to-analog conversion [123]

the transistor datasheet [125]. To obtain 50 dBm (100 W) from the HPA, a driver with a gain of 37 dB is required (for a total gain of 57 dB for the amplifying stage). Every dB of gain reduction on the HPA (e.g. due to mismatch) needs to be compensated by the driver. Finally, as can be seen in figure 7.3, the power reaching the applicator is less than 90 W.

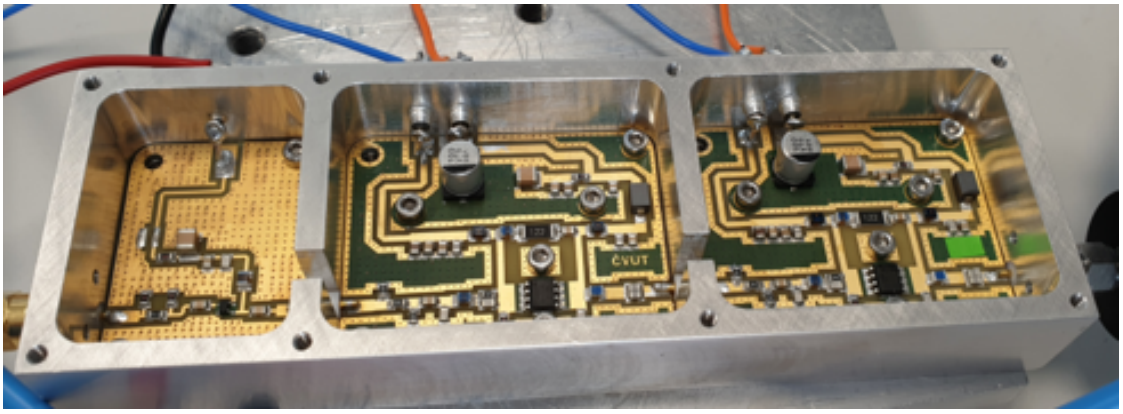
In order to meet the gain requirements of the driver and to provide a minimum of 1 W (see figure 7.3) to drive the HPA, a 3-stage configuration was selected. In this case the driver is composed of a gain stage employing the general purpose MMIC[2] amplifier BGA614 [126] and two identical pre-drivers built around the GaN HEMT[3] NPTB00004 [127]. The pictures of the built driver can be seen in figure 7.4.



(a) Gain state



(b) Pre-driver



(c) Driver

Figure 7.4: Driver composed of 3 amplifying stages

The driver was designed to operate over a broadband frequency range, going all the way from 70 MHz to approximately 450 MHz. To accomplish this, negative feedback combined with lossy matching was used for the pre-driver. The design of feedback amplifiers is out of the scope of this chapter and the interested reader is referred to the existing literature [128]. The small-signal performance of the driver shows that the gain is equal to 44.7 dB

[2]Monolithic Microwave Integrated Circuit
[3]Gallium Nitride High-Electron-Mobility Transistor

Table 7.2: Small-signal performance of driver amplifier

Frequency (MHz)	$\lvert\underline{S}_{21}\rvert$ (dB)	$\lvert\underline{S}_{11}\rvert$ (dB)	$\lvert\underline{S}_{22}\rvert$ (dB)
70	44.7	−34.9	−16.3
250	43.3	−36.8	−14.0
450	40.9	−31.6	−12.7

at 70 MHz and goes down by 1.4 dB at 250 MHz. The output return loss is better than 12 dB in the range of $(70 - 450)$ MHz and the input return loss better than 30 dB in that frequency range. The small-signal performance of the driver is summarized in table 7.2. The large-signal performance of the driver will be shown later in this section.

7.2.2 Power Amplifier Implementation and Measurements

The final stage or HPA was built using the LDMOS device MRF101AN [125]. In this case, the company NXP[4] offers a design kit composed of a small printed circuit board (PCB), a custom base plate, two transistors and additional parts like screws and SMA[5] connectors. This allows the designer to concentrate on the circuit design, selecting the appropriate passive components and do the assembly of the small-footprint PA. The picture of the assembled amplifier can be seen in figure 7.5.

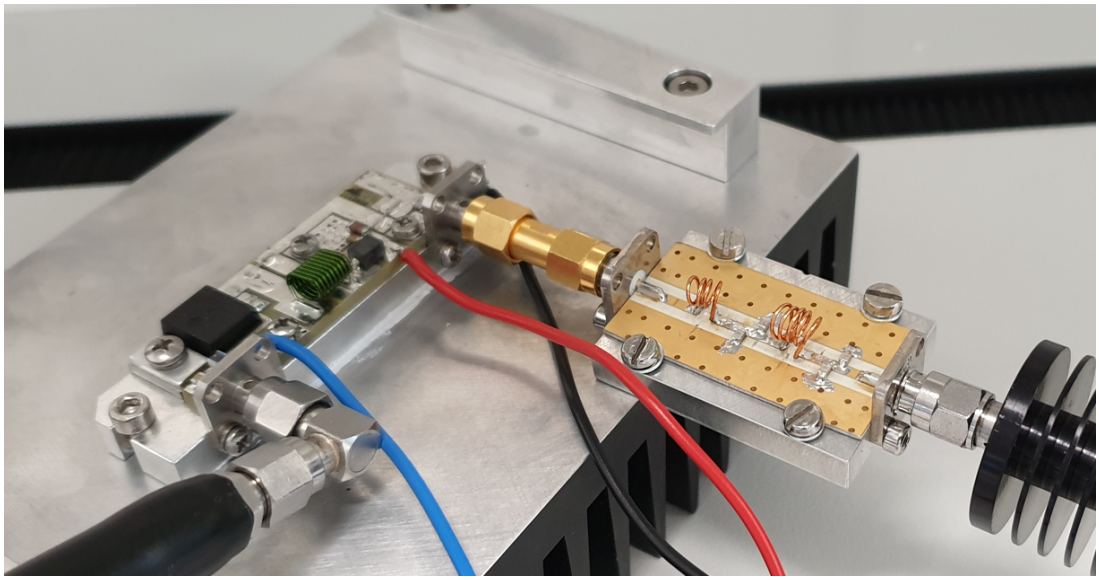


Figure 7.5: Picture of 100 W amplifier

As there is no large-signal model available for the MRF101AN, the S-parameter data provided by the manufacturer was used to design the input matching network of the PA. For the output matching network an alternative approach was used, which allows designing

[4]https://www.nxp.com/
[5]SMA: SubMiniature version A coaxial connector

and optimizing the output impedance presented to the transistor drain. In this respect, an additional PCB contains the output matching circuit, which consists of a 4-element low-pass network. The impedance to be presented to the transistor drain was obtained by interpolation of the impedance data given in the datasheet for the reference circuits [125]. The element values of the output matching network (OMN) were initially obtained via simulation and subsequently tuned to obtain the desired impedance value. Figure 7.6 shows the small-signal measurements of the PA. The OMN transforms the 50 Ω load impedance to a value of $(12.4+j2.9)$ Ω as can be seen in figure 7.6a. A good input return loss (RL) is observed (close to 20 dB at 70 MHz) but the output RL is apparently insufficient, exhibiting a value of 1.8 dB at 70 MHz (see figure 7.6c). The poor output RL observed in the measurement is a normal behavior. The device is biased in deep class-AB with a quiescent drain current of only 100 mA. The output impedance is highly dependent on the output voltage swing at the transistor output and will improve as the device is driven to operate at high output power levels.

The whole amplifying chain was assembled and measured. The measurement setup can be seen in figure 7.7. The additional 4th-order low-pass filter connected at the output of the driver allows reducing the 2nd harmonic component (at 140 MHz) by 30 dB in order to inject a clean signal into the PA. The performance of the driver and of the output stage is shown in figure 7.8. The power of the generator was swept from −24 dBm to −10 dBm allowing to obtain 112 W from the PA. This required approximately 3 W from the driver (or 35 dBm as shown by the black trace in figure 7.8a). The gain of the driver stage was better than 45 dB. Figure 7.8b indicates that the output stage is saturated with a gain of 15.4 dB at maximum power. At this point, the PA reaches a drain efficiency close to 78%. The bill-of-materials (BOM) for the gain block, pre-driver and HPA can be found in Appendix D.

Although the amplifier displays a good performance, the experiments in [114] showed that the power provided by this amplifier was not enough to produce the desired heating of the phantom and for that reason a new power amplifier with higher output capability was required. The next section presents the design of a 250 W power amplifier.

7.3 Power Amplifier with $P_0 = 250$ W

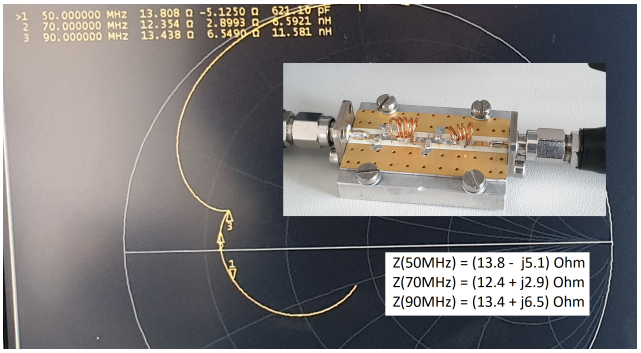
For the design of the new amplifier the transistor MRF300AN from NXP was selected [129]. The device is specified for $P_{out} = 300$ W and for operation up to 250 MHz. In addition to this, it comes in an low-cost over-molded plastic package, which makes it an attractive option in terms of price[6] and expected performance.

The design process described in this section start by evaluating two approaches:

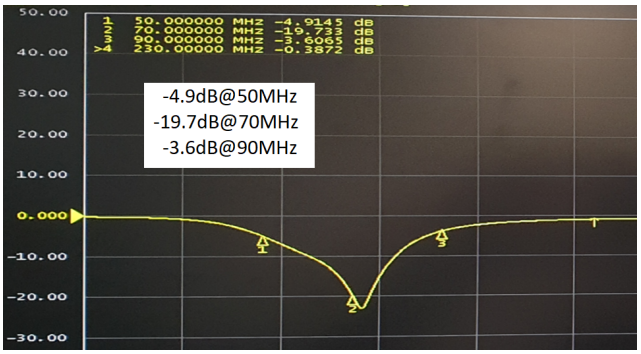
1. Approach 1: using the parallel-circuit class-E design equations from previous chapters to create an initial PA design

2. Approach 2: using load-pull simulations to determine the appropriate loading for high-efficiency operation

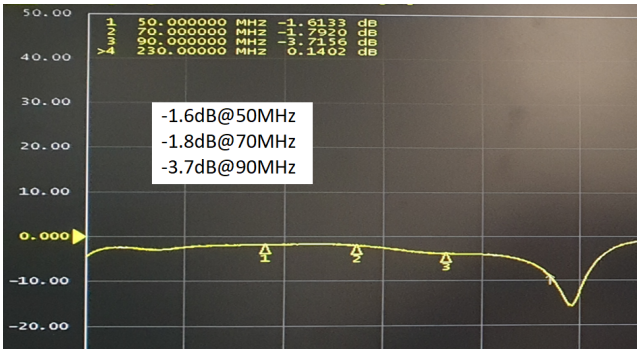
[6]The cost-per-watt of the MRF300AN at 0.18 $/W is less than half of a comparable devide at 0.47 $/W employing a ceramic housing



(a) Impedance presented to the drain



(b) Input return loss



(c) Output return loss

(d) Gain

Figure 7.6: S-parameters of PA using MRF101AN

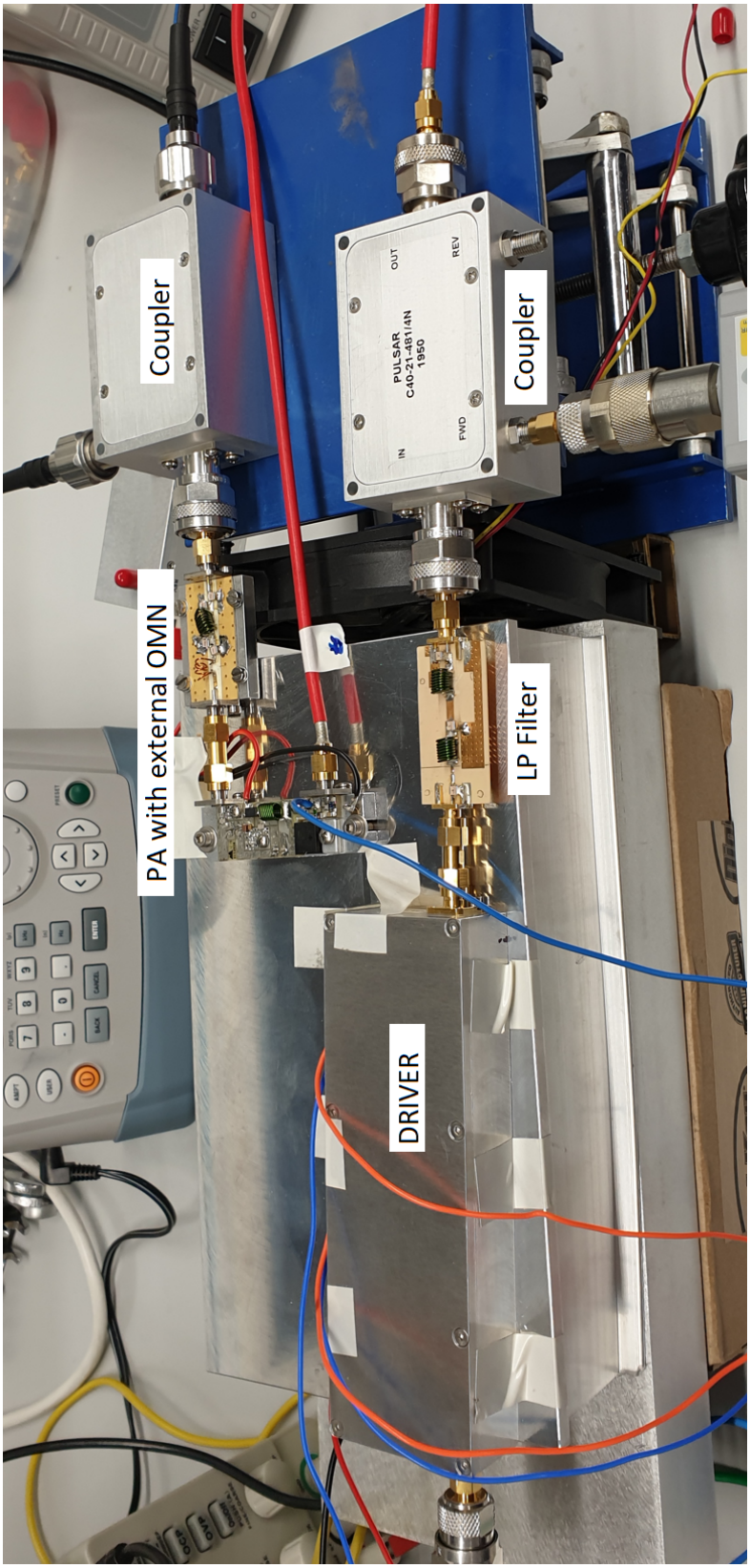
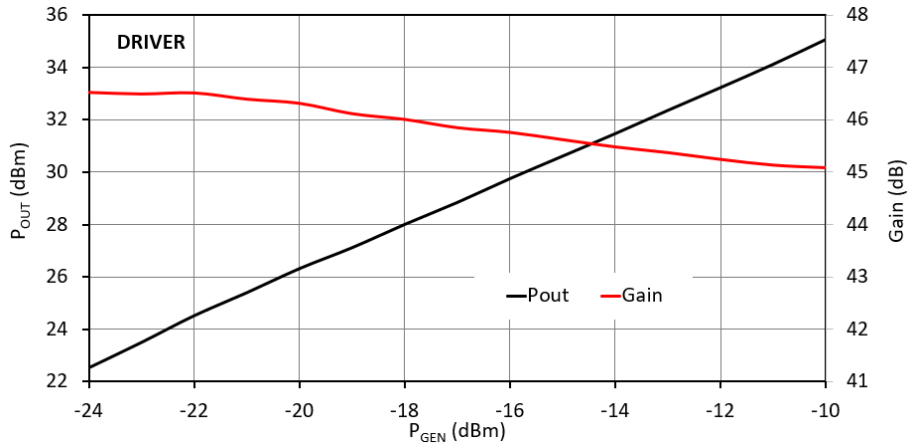
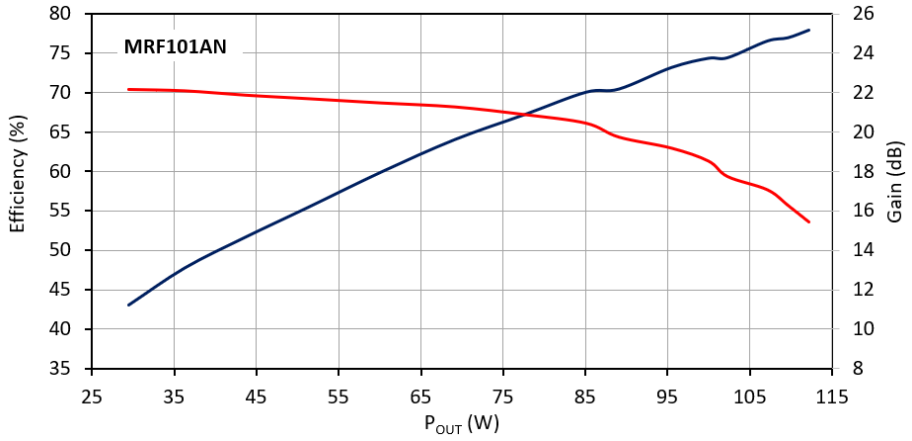


Figure 7.7: Test setup showing the driver, PA and additional components



(a) Output power and gain of driver



(b) Gain and drain efficiency of PA vs output power

Figure 7.8: Large-signal performance of driver and PA

7.3.1 Evaluation of PC Class-E Topology via Simulations

To proceed with approach 1, the equations (5.11) to (5.13) in subsection 5.1.2 were used to determine the values of the lumped elements in the parallel-circuit class-E topology. The input to those equations are: $V_{dd} = 50$ V, $P_{out} = 300$ W and $f_0 = 70$ MHz. In addition to this, the knee voltage is set to $V_{knee} = 3$ V, which is taken from the IV curves generated using the large-signal model. The knee voltage needs to be subtracted from V_{dd} in equation (5.11). The resulting circuit can be seen in figure 7.9

The input matching network was designed by conjugately matching the input impedance of the transistor, which was obtained from $\underline{S}_{11}$ at the deep class-AB biasing condition of $V_{gs} = 2.368$ V and $V_{ds} = 50$ V. A shunt R-C circuit in series with the transistor gate was used to provide unconditional stability, although in later designs, only a resistor in the gate bias path is enough to serve this purpose. The output capacitance C_{ds}^{out} of the transistor is

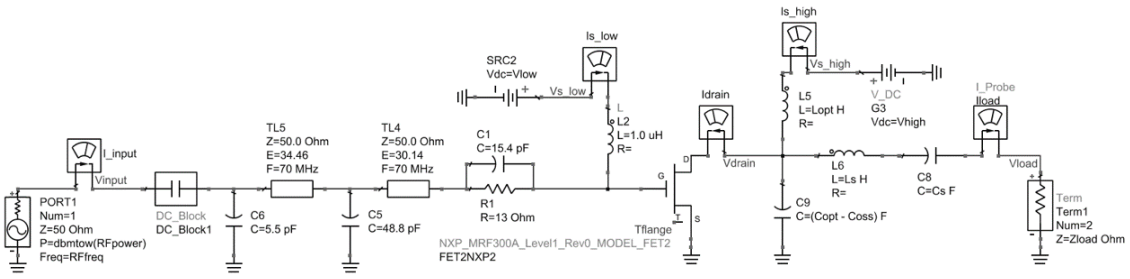


Figure 7.9: Circuit diagram of PC class-E amplifier

bias dependent and the value used here is $C_{ds}^{out}(50V) = 105$ pF[7].

The simulated performance of the circuit is shown in figure 7.10. The power sweep in 7.10b shows a good efficiency level of 88.5% and an output power of 53.5 dBm for an input power of 33 dBm. To verify class-E operation, the intrinsic waveforms (at the current generator or switch plane) are also shown[8]. These waveforms resemble those of a class-E amplifier, in which the current waveform has been smoothed. Some overlap between the voltage and current is observed, as expected for an non-ideal switching behavior. The current waveform also displays negative values (trace in red color), something that in the classical class-E theory is usually attributed to a non-fully discharged output capacitance during switch on [49]. In figure 7.10a the waveforms for two different values of input power are given. At $P_{in} = 28.5$ dBm the peak drain voltage reaches 133 V, which is the value for the breakdown voltage V_{BR} given in the datasheet of the device [129]. At this input power level, the PA delivers $P_{out} = 51.6$ dBm (below 150 W) at 72.3% efficiency, which is significantly lower than the values for $P_{in} = 33$ dBm. The peak drain voltage at this higher P_{in} is 156 V and therefore 17% higher than V_{BR}.

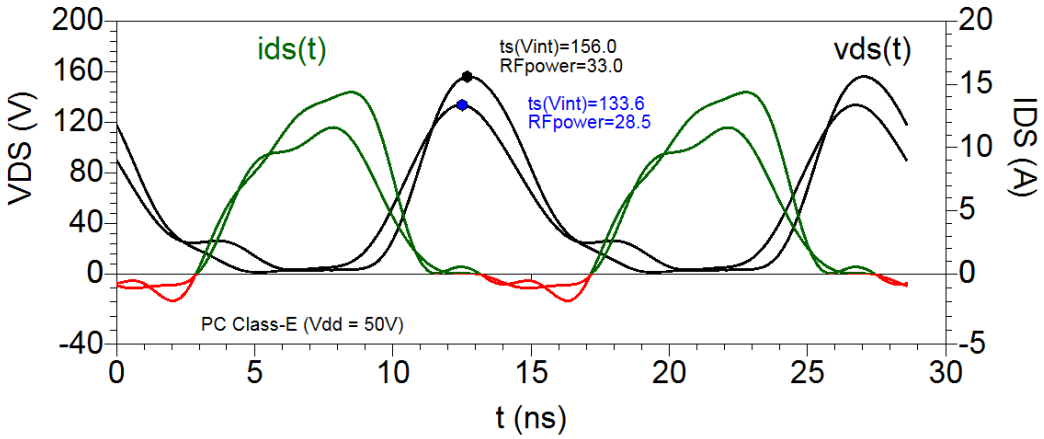
According to the literature, the peak drain voltage in the PC class-E topology can reach up to $\approx 3.6 \cdot V_{dd}$ [100]. On the other hand, the observed peak voltage in figure 7.10a is rather close to $3 \cdot V_{dd}$, therefore, a second simulation at reduced drain voltage was performed. In this case $V_{dd} = 40$ V was selected, which is about 3.3 lower than the transitor V_{BR}. Before running the simulation, the element values of the circuit were re-calculated and a slightly higher value for the output capacitance used, i.e., $C_{ds}^{out} = 113$ pF[9]. To be able to recover the output power level the sweep is performed up to $P_{in} = 36$ dBm. As can be seen in figure 7.11b, the output power is 53.6 dBm at an efficiency level of 85.9%, while keeping the peak voltage below 133 V. The current has been increased and now has a peak value of 18.7 A (with an acceptable DC level of 6.5 A). The RF swing at the gate displays a peak value of 9 V, which is still below the 10 V maximum rating for V_{gs}. This result seems to indicate that reducing the drain voltage to 40 V and driving the device with 4 W would allow to ideally obtain close to 230 W at 85.9% efficiency[10].

[7] Please note that in the schematic the wrong notation C_{oss} was used. C_{oss} refers to the short circuit ouput capacitance and is equal to $C_{ds}^{out} + C_{gd}$. For the used device $C_{gd} \approx 2$ pF and therefore $C_{oss} \approx C_{ds}^{out}$

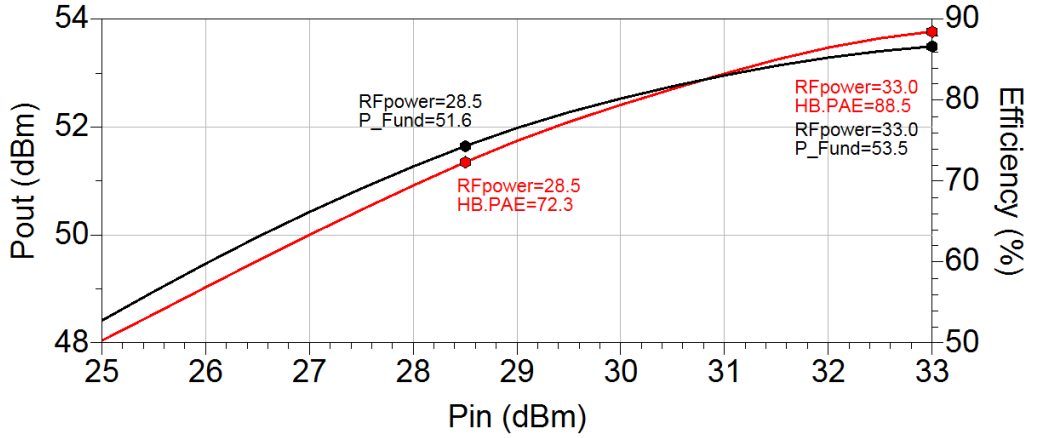
[8] See Appendix E to see how to calculate the intrinsic waveforms

[9] The value for $C_{ds}^{out}(V_{dd})$ is obtained from the simulated output admittance $\underline{y}_{22}$ at $f_0 = 1$ MHz when biasing the device below threshold, in this case $V_{gs} = 0$ V and setting the corresponding V_{dd} (see Appendix E)

[10] Please note that losses in passive components and thermal effects will negatively affect this outcome



(a) Intrinsic drain voltage and current waveforms



(b) Output power and efficiency

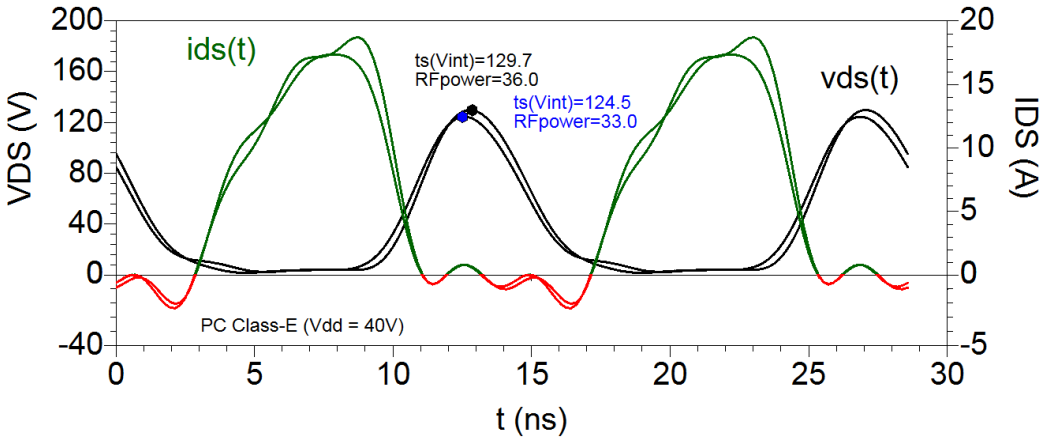
Figure 7.10: Simulation results of PC class E for $V_{dd} = 50$ V

7.3.2 General Approach via Load-Pull Simulations

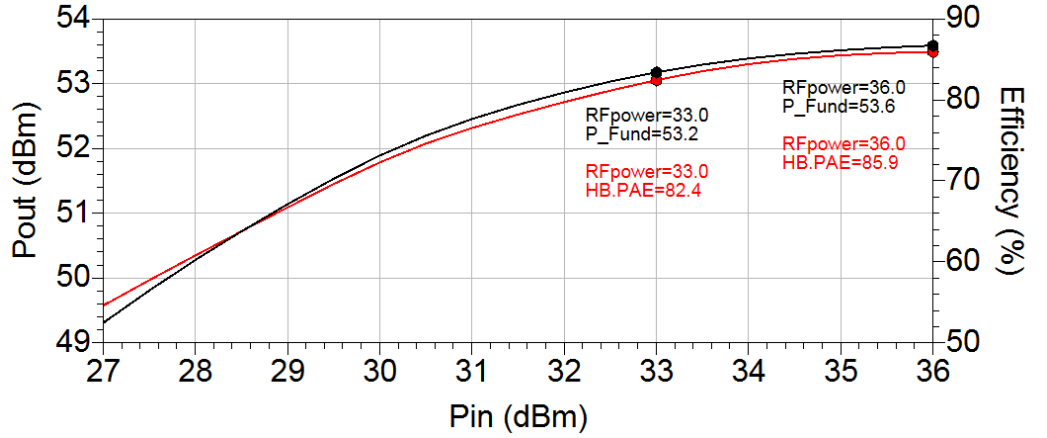
As a second approach, load-pull simulations were performed using the large-signal model of the transistor. The parameters used to run the setup can be found in table 7.3. Besides the input power level, frequency and biasing condition, the impedance terminations at the harmonic frequencies have to be specified. In this case, the default value of 500 Ω was used, which is practically an open circuit when compared to the optimum impedance required by the device at the fundamental frequency. As with previous simulations, the case temperature T_{case} of the device was set to 100°C. The obtained impedances as well as output power and power-added efficiency (PAE[11]) after few iterations of load and source-pull can be seen in the lower part of table 7.3. An output power of 275 W at an efficiency level of ≈ 89% is obtained.

The high efficiency obtained from the load-pull optimization suggests that some kind of

[11] $PAE = (P_{out} - P_{in})/P_{DC}$



(a) Intrinsic drain voltage and current waveforms for $V_{dd} = 40$ V



(b) Output power and efficiency for $V_{dd} = 40$ V

Figure 7.11: Simulation results of PC class E for $V_{dd} = 40$ V

waveform shaping is happening within the circuit with the set of impedances presented to the device. To evaluate this, the drain voltage and current signals at the intrinsic plane of the transistor are shown in figure 7.12. These waveforms remarkably resemble those of another member of the high-efficiency PA family, namely, the *class-J* power amplifier. Wright et al. [130] present measurements of typical class-J waveforms on a 10 W GaN HEMT. Both current and voltage waveforms are quasi half sinusoidal in shape and the current also passes through small negative values in the same wave as observed in figure 7.12a. The power sweep was performed up to $P_{in} = 30$ dBm and therefore 3 dB lower than the value used in the load-pull setup. As can be seen in figure 7.12b, the peak drain voltage exceeds V_{BR} for input power levels beyond 25.5 dBm. Exceeding the manufacturer's DC breakdown voltage rating of the device seems to be a major practical issue in high-efficiency modes of operation, which might require trading output power for efficiency. For instance, Cripps [32] has theoretically shown that a peak voltage ratio of nearly 3 is obtained in class-E PAs, when choosing a conduction angle to provide the same output power level as

Table 7.3: Parameters and results of Load-Pull simulation

Parameter	Value
P_{in} (dBm)	33
f_0 (MHz)	70
V_{dd} (V)	50
V_{gsq} (V)	2.368
(I_{dsq} (mA))	(100)
$Z_{S,L}^{nf_0}$ (Ω)	500
Z_S (Ω)	$3.0 + j8.3$
Z_L (Ω)	$3.1 + j4.3$
P_{out} (dBm)	54.4
PAE (%)	88.9

Table 7.4: Simulation-based comparison of two design approaches ($V_{dd} = 50$ V)

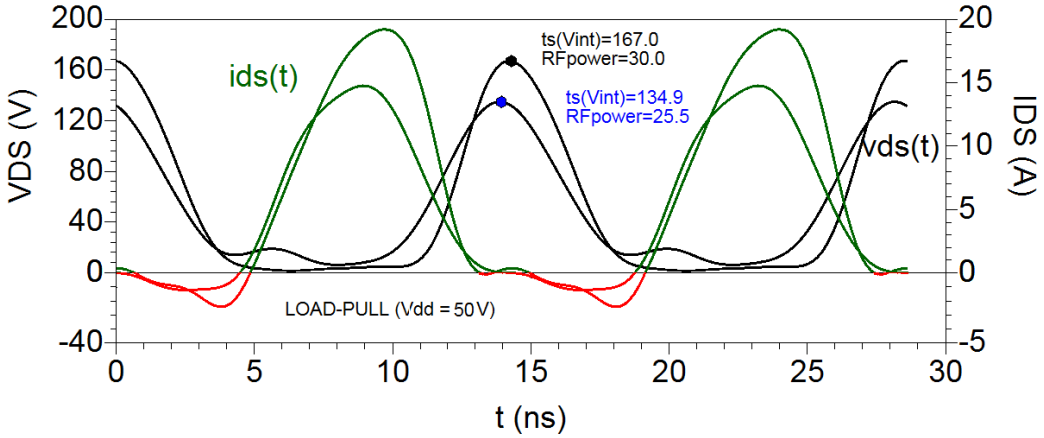
No.	Approach	P_{in} (dBm)	P_{out} (dBm)	Eff. (%)	V_{ds}^{peak}
(1)	PC Class-E	33	53.5 (224 W)	88.5	$1.17V_{BR}$
		36	53.7 (234 W)	89.6	$1.20V_{BR}$
(2)	Load Pull	30	54.2 (263 W)	86.1	$1.26V_{BR}$

in class-A operation (having a peak voltage ratio of 2). Brounley [17] brings some insights into this topic. In his experiments with high-efficiency power amplifiers, he has registered drain peak voltages above breakdown. For instance, in a design operating at 40.68 MHz with $P_{out} = 544$ W and with efficiency of 85%, the peak voltage was 150 V, which is 36% higher than the specified $V_{BR} = 110$ V. In this case, the measured excursions were on the order of 2 ns long during the time the DC breakdown is exceeded. Brounley concludes that the RF breakdown is higher than the DC value specified by the manufacturer. An additional observation concerns the data provided by NXP on the MRF300AN. According to the datasheet, the device is able to deliver 300 W of power even at efficiency levels reaching the 80% when operating at $V_{dd} = 50$ V [129]. This seems to be a clear indication that the device is operating with peak voltages pass its DC breakdown voltage. For the purpose of this work, it will be considered that peak voltages exceeding the DC breakdown by about 36% (as measured by Broundley [17]) are still acceptable.

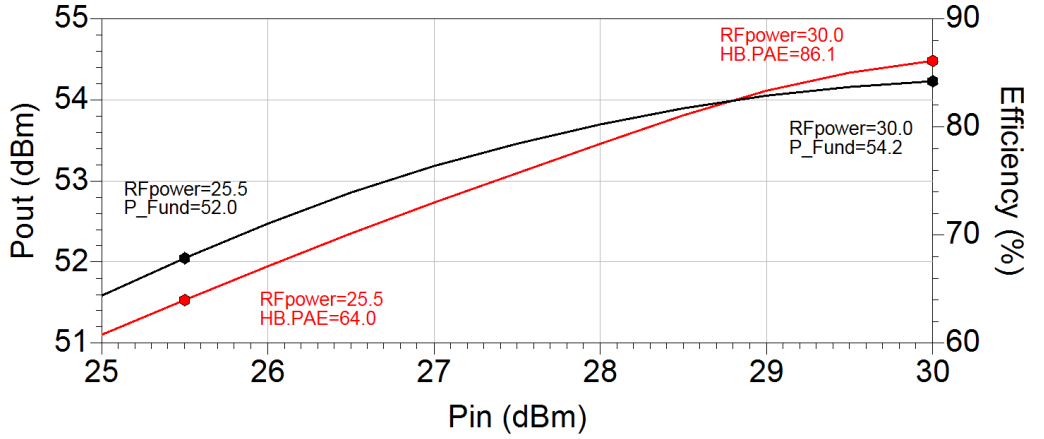
Table 7.4 summarizes the results of the studied approaches when using a supply voltage of $V_{dd} = 50$ V. As can be seen here, approach no. 2 offers a good compromise between output power and efficiency at an acceptable peak voltage factor (peak drain voltage exceeds DC breakdown by 26%, which is below the 36% previously mentioned).

7.3.3 Power Amplifier Implementation

Using the impedance values from the Load-Pull simulation, the input matching network (IMN) and output matching network (OMN) were synthesized. The corresponding circuit diagram is shown in figure 7.13. Both matching networks are composed of two cascaded



(a) Intrinsic drain voltage and current waveforms



(b) Output power and efficiency

Figure 7.12: Simulation results of Load-Pull setup E for $V_{dd} = 50$ V

low-pass L-type transformers. This topology is quite general and can be employed in either broadband amplifier matching [131] or for instance in output networks for class-E amplifiers at gigaherz frequencies by replacing the lumped elements by transmission lines [45].

The simulated response of the amplifier using ideal components is shown in figure 7.14. The power sweep shows an output power of 54.6 dBm (288 W) at an efficiency level of 79.3%. The peak voltage is exceeding V_{BR} by more than 36%. In this case the input power needs to be reduced to compensate for this. The differences with the previous results using the load-pull data, are caused by the output matching circuit, which presents different impedances at the $2nd$ and $3rd$ harmonic components. In this case, the circuit elements in the matching network need to be adjusted to recover the performance.

The company NXP provides once more a design kit for the MRF300AN. The kit contains a PCB, a small aluminum plate and the transistor. For the sake of symplicity, the provided PCB was used. The DXF files of the board were imported into ADS [99] and planar EM simulations run. The layout of the PA in the simulation environment can be seen in figure

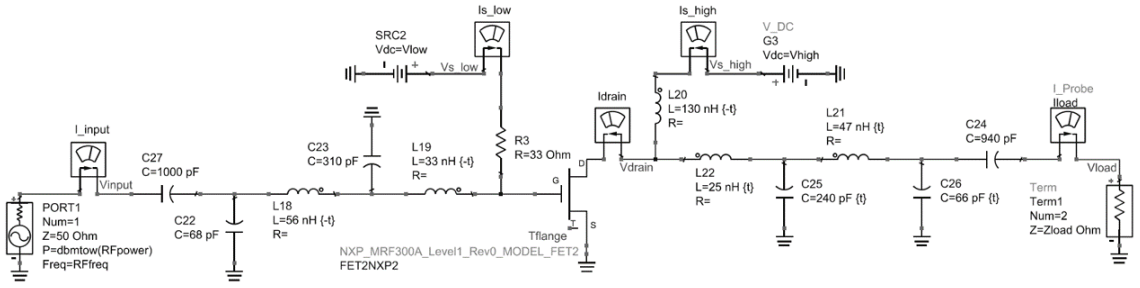


Figure 7.13: Circuit diagram of amplifier with synthesized IMN and OMN

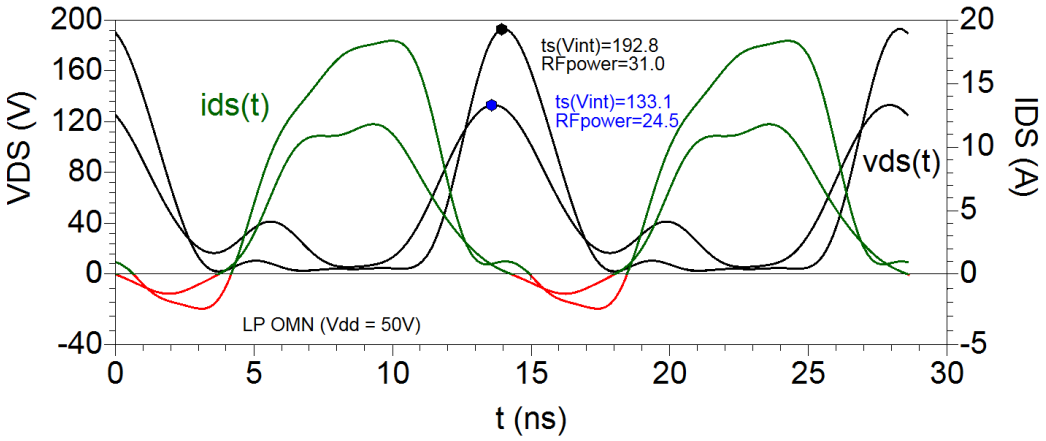
7.15. At the fundamental frequency of 70 MHz EM simulations of the layout are not really required, but the parasitic components of the board become important at the harmonics. Figure 7.15 also shows the impedance seen from the drain side of the device towards the OMN for two cases, i.e., when using an OMN with ideal components as in figure 7.13 and when using the layout of the OMN as shown in figure 7.15. In both cases the same ideal lumped components were used, so that the main difference lies in the interconnects (traces) between those components. At the fundamental frequency the real part of the input impedance in both cases is quite similar, with differences below 1 Ω. As the frequency increases the differences in the imaginary part become aparent.

The power amplifier employing the layout was simulated. Ideal lumped components were replaced by the manufacturer S-parameters. For the initial implementation commercialy available inductors are used, therefore the value of the two inductors in the OMN (25 nH and 47 nH respectively) were adjusted to meet existing components (22 nH and 42 nH), something that will slightly affect the performance. The power sweep and waveforms of the simulated amplifier can be seen in figure 7.16. At $P_{in} = 32$ dBm (peak factor of $1.36V_{BR}$) the output power is 53.4 dBm and the efficiency 78.1%. If the 42 nH inductor is replaced by two 22 nH in series[12], the efficiency can be increased to 82.5% while no real change in output power is obtained (an small increase in 0.1 dB is observed). Further, a reduction in the capacitor values at the OMN would allow obtaining 54.2 dBm output power at 84.3% efficiency. To achieve that, a 1 dB increase in input power is required with the added benefit of slightly reducing the peak factor to $1.31V_{BR}$.

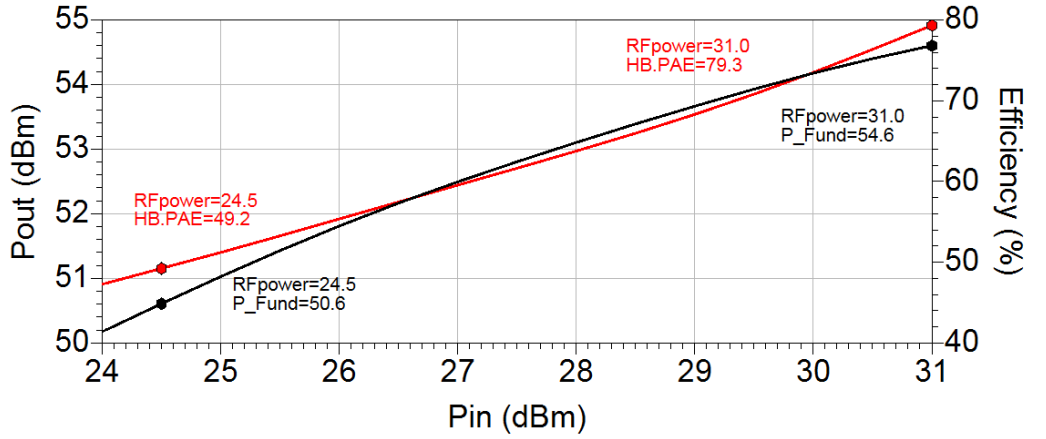
The picture of the assembled PCB is shown in figure 7.17. As can be seen in the figure, the transistor is still not soldered, since the idea here is to first measure the impedances presented by the matching networks to the gate and drain of the device. In the setup shown, a semirigid coaxial cable is used to interface the coaxial port of the network analyzer to the gate and drain traces on the PCB. Before soldering the cable, a one-port calibration was performed to reference the measurement to the un-connectorized side of the cable. The standards used during the SOL[13] calibration were the following:

- Load: a 51 Ω SMD[14] resistor soldered between the inner conductor and the cable shield

[12] For the selected high current inductors, there are no values between 42 nH and 66 nH
[13] Short-Open-Load
[14] Surface-Mounted Device



(a) Intrinsic drain voltage and current waveforms



(b) Output power and efficiency

Figure 7.14: Simulation results of amplifier circuit for $V_{dd} = 50$ V

- Short: a short length of wire soldered between the inner conductor and the cable shield
- Open: no connection at all

Figure 7.18 presents the results of the impedance measurement together with the simulated data. As can be appreciated in the figure, there is a good agreement between the measured and simulated data. For the case of the OMN the markers show the values for the fundamental as well as for the harmonics.

The S-parameters of the fully assembled PA are shown in figure 7.19. The red traces corresponds to the simulated data and those in black to the measurement. As can be appreciated, there is a good correspondence between the measured and simulated data. The measured curve for $\underline{S}_{11}$ displays 20 dB of input return loss at 70 MHz. This level of matching is not predicted by the simulation. Regarding the gain it can be said that both curves exhibit similar behavior. The measured small-signal gain of the amplifier is 18.7 dB

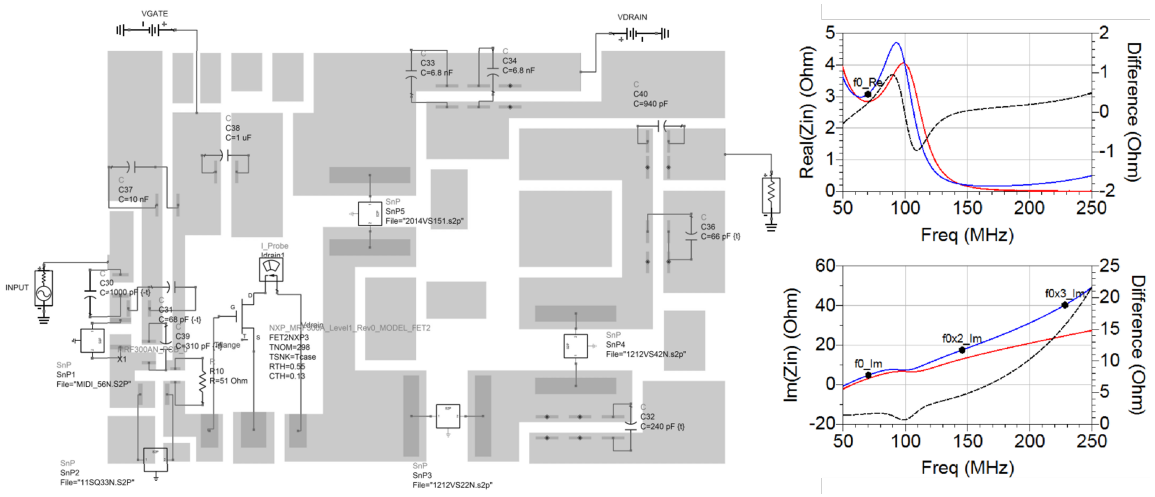
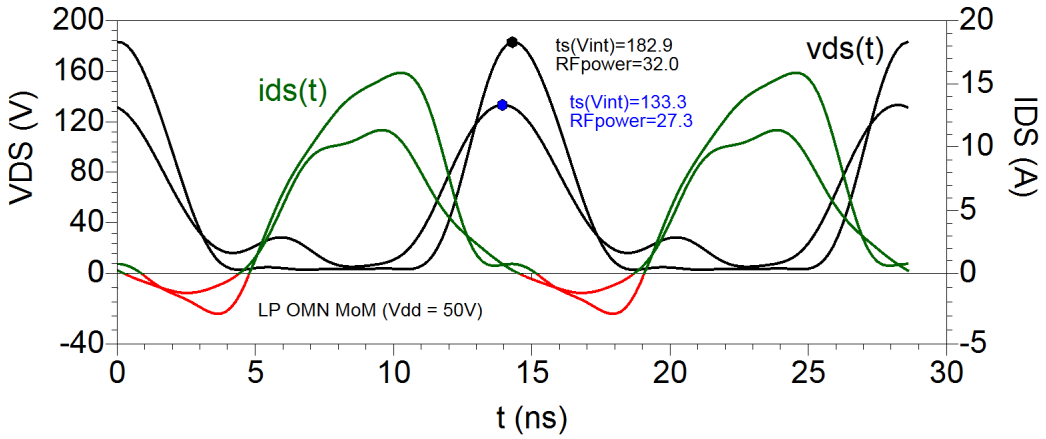


Figure 7.15: Layout of amplifier and input impedance presented by the OMN in the ideal circuit and when using the EM-simulated layout

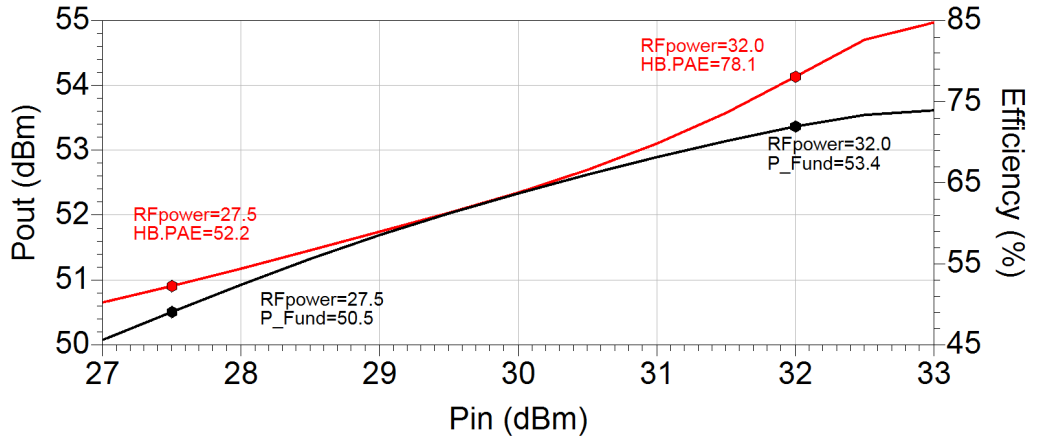
for the design frequency, whereas the simulated value is 4 dB lower. It is important to mention that for both cases, i.e., for the measurement as well as for the simulation a gate voltage was individually selected to obtain about 110mA of drain quiescent current (deep class-AB biasing). The case temperature in the model was also set back to 25°C (otherwise a higher drain current would flow using the same gate voltage). These settings allow to have similar operating conditions. Nevertheless, it is important to remember that model inaccuracies are possible. The output return loss looks quite similar in both cases. This poor level of small-signal output matching was also observed in the 100 W amplifier. As previously stated, the output impedance is highly dependent on the voltage swing at the transistor output and will change as the device is driven to operate at high output power levels. A proof that the output impedance matching improves is the significant gain increase exhibited by the PA during large-signal operation, as will be shown later.

The initial large-signal testing phase of the PA was not quite successful. The PA did not reach 200 W and exhibited poor efficiency, which caused the measured case temperature to reach the 100°C mark after 4 mins of operation. To avoid damage of the device, the PA was switched off when the case temperature reached 120°C. Care was taken to provide enough cooling by placing the transistor directly onto a bigger heatsink (using a thin layer of silicon grease) and by using cooling fans. Slight modifications of the biasing point (quiescent current) and of the drain voltage did not show significant deviation of the observed performance. This first experimental round apparently shows that the transistor large-signal model prediction capabilities are not as expected. A more detailed study is required to understand the usability range of the manufacturer's transistor model.

In order to optimize the performance of the designed power amplifier, following methodology was used: a) using the large-signal simulation as a guidance tool to understand how to change (increase/decrease) a certain component in the OMN (to improve P_{out} and efficiency) and b) implement those changes into the PC board of the PA. For instance, as mentioned early in this section, increasing the value of the second inductor (42 nH in the



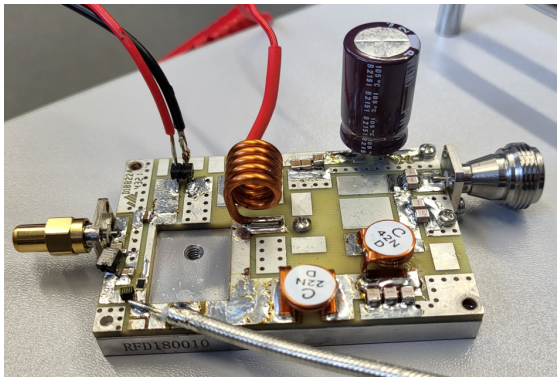
(a) Intrinsic drain voltage and current waveforms



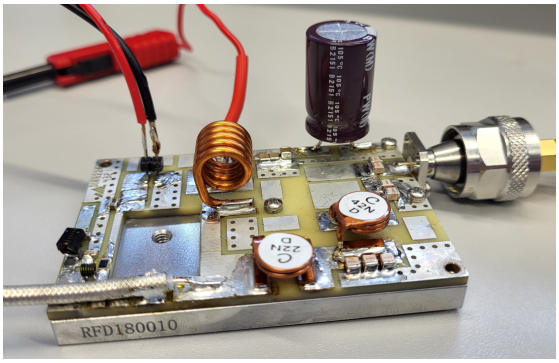
(b) Output power and efficiency

Figure 7.16: Simulation results of PA using layout with $V_{dd} = 50$ V

board and L_{21} in figure 7.13) has a positive effect on the amplifier efficiency. After making those changes, Z_{drain} (please refer to figure 7.18b) can be observed by simulation to understand what kind of loading is required by the PA. The low-pass OMN is composed of the elements L_{22}, C_{25}, L_{21} and C_{26} according to figure 7.13 (an additional degree of freedom offers the bias inductor L_{20}). Modifying the value of L_{21} allows the fundamental impedance $Z_{drain}(f_0)$ to move on a line of almost constant reactance (without significantly changing the harmonic impedances). Or in another words, this allows adjusting the real part of the fundamental impedance presented to the device. On the other hand, the inductor L_{22} would cause all impedances (fundamental and harmonics) to move on a line of almost constant resistance. A possibility to only move the harmonic impedances would be to firstly use L_{22} and then the two capacitors to move back the component at f_0. Capacitor C_{26} would exclusively affect the impedance at f_0 in its real and imaginary part. Although all those changes are theoretically possible, in practice, applying those to our PC board would be cumbersome (e.g. de-soldering and re-soldering capacitor combinations on a PCB mounted



(a) Setup for measuring Z_{gate}



(b) Setup for measuring Z_{drain}

Figure 7.17: Setup for measuring impedances presented to LDMOS device

on a heatsink is a challenging task), therefore, changes were only applied to the inductors to optimize the PA performance as much as possible.

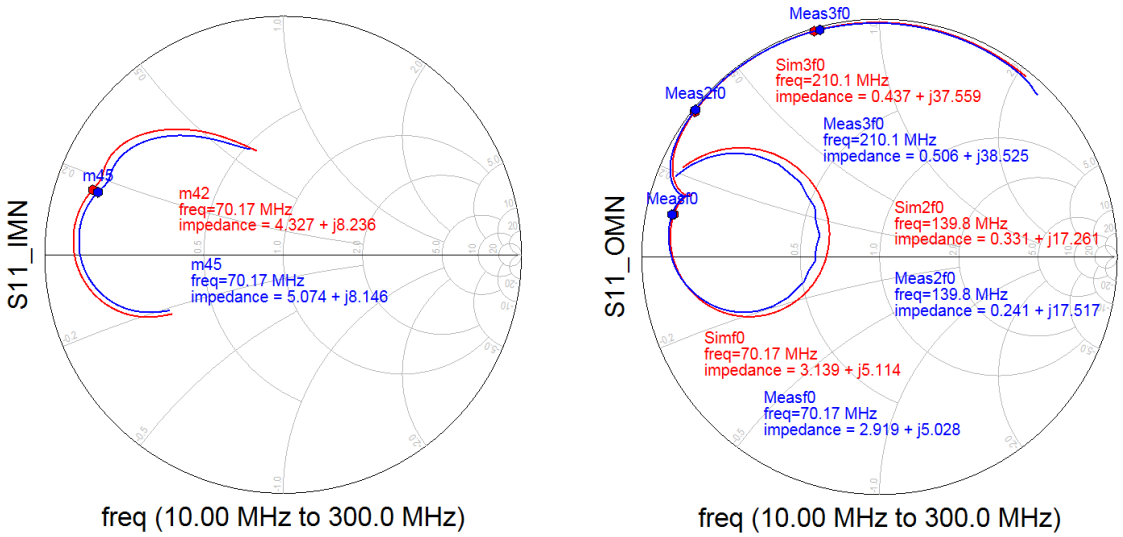
The final performance of the optimized power amplifier is shown in figure 7.20. The output power for $P_{in} = 31.7$ dBm (or close to 1.5 W) is equal to 54.2 dBm or 263 W. The efficiency achieved at this power level is equal to 76.9 % and the power dissipated in the device is $P_{diss} = 79$ W. The operation of the power amplifier was stable and the case temperature did not exceed the 90°C. Figure 7.21a shows the picture of the improved PA using hand made coils for L_{21} and L_{22} and figure 7.21b a thermal image of the PA after 30 min of continuous operation at a constant $P_{out} = 242$ W. Rising the gate voltage from 2.56 V to 2.68 V allows an additional increase of the output power up to ≈ 275 W at an efficiency of 77.5%. As previously clarified, the capacitors in the output matching network were not changed, therefore limiting the optimization of the PA module.

7.3.4 Experiments using Agar Phantom

In order to evaluate the performance of the power amplifier in a close-to-real environment, the test setup in figure 7.22 was prepared. The difference of this arrangement in comparison with previous measurements is that the power amplifier is not connected to a high-power 50 Ω load but to an applicator loaded with a phantom. Power meters connected to the coupling ports of coupler #2 measure the incoming power to the applicator and the reflected power. The RF generator is a commercial amplifier system from the company ALBA. This systems was adjusted to operate at reduced power levels. Coupler #1 was initially used to register the input power of the amplifier under optimum loading (50Ω termination) in order to create an input power reference table. Once this process was completed, the two available sensors were connected to coupler #2.

The applicator used in the experiments is a patch antenna element operating at 70 MHz and part of a regional hyperthermia system, which is currently being developed at FBMI[15] for the treatment of cancer in the pelvic region [132]. A picture of the applicator is shown in figure 7.23a. This 2-layer structure (ground plane and upper layer) forms a microstrip

[15]Institute of Biomedical Engineering in Kladno



(a) Measured and simulated Z_{gate}

(b) Measured and simulated Z_{drain}

Figure 7.18: Impedances presented to LDMOS device

line using water as the substrate. The height of the substrate is 25 mm and on top of this an additional 75 mm water layer represents the bolus which, as previously explained, provides heat uniformity, cools down the tissue surface to minimizes hot spots and improves matching between the RF source and the tissue [115]. A plexiglass enclosure holds the whole structure in place.

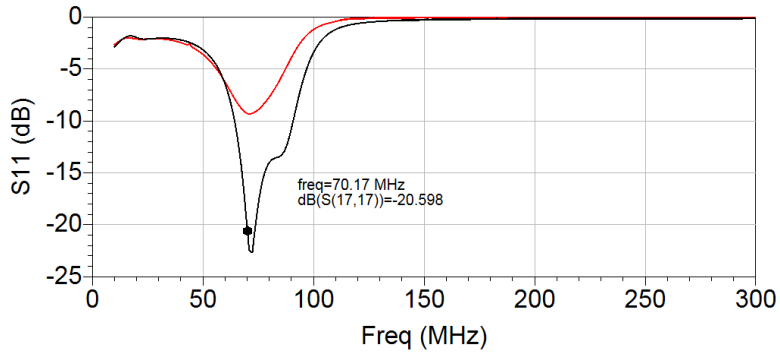
An agar phantom representing human muscle tissue was used in the experiments. It consists of distilled water, gelatin agar and sodium chloride[16]. The manufactured phantom was divided into four sections or layers that could be separated from one another. After RF energy exposure, the temperature in each layer would be measured with a thermal imaging camera. A picture of the agar phantom on top of the patch antenna can be seen in figure 7.23b. The first step in setting the antenna-phantom arrangement is:

1. filling the plexiglass enclosure with distilled water
2. measuring the temperature on each of the four layers
3. placing the layers one by one on top of the patch antenna
4. measuring the reflection coefficient of the arrangement (the reference plane is at the input of the 1 m coaxial cable connected to coupler #2 in figure 7.22)

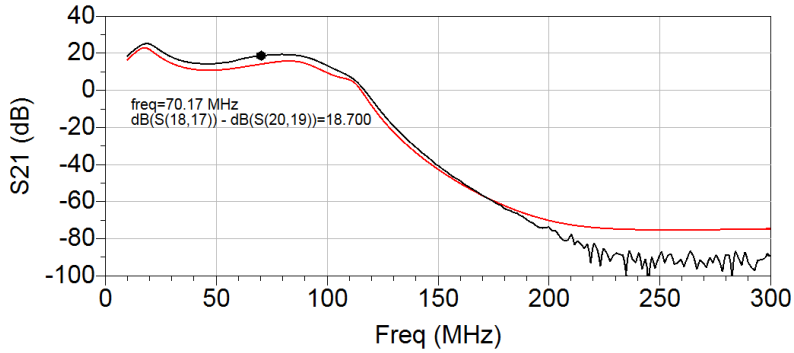
Markings on the foil holding each layer allows to identify the layer number.

The results for two rounds of experiments are shown in table 7.5. The first experiment was run for 6 min, whereas the second for 3 min. Once an RF heating round is completed, the temperature on each layer is measured once more. This requires removing each layer one by one and measuring its corresponding temperature. As can be seen, this also implies that

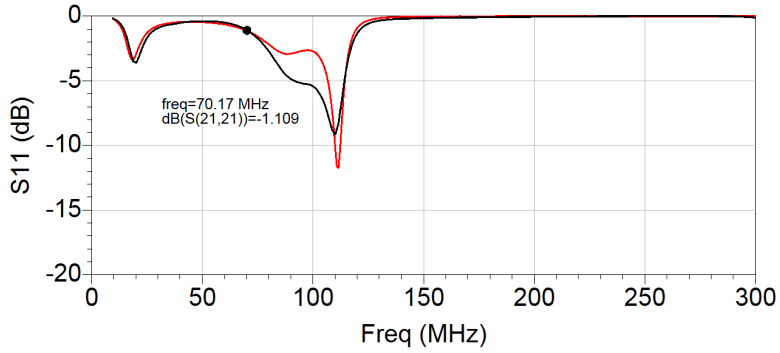
[16]More details on the phantom preparation can be found in [132]



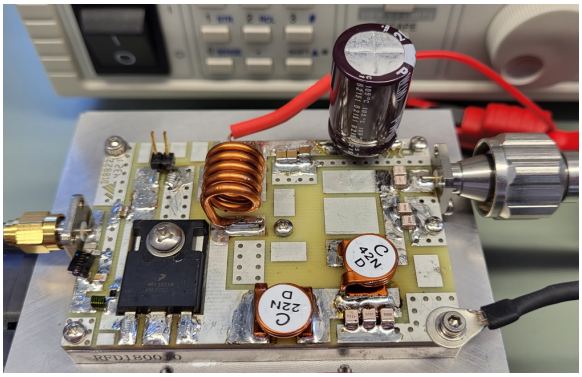
(a) Input reflection coefficient



(b) Amplifier gain

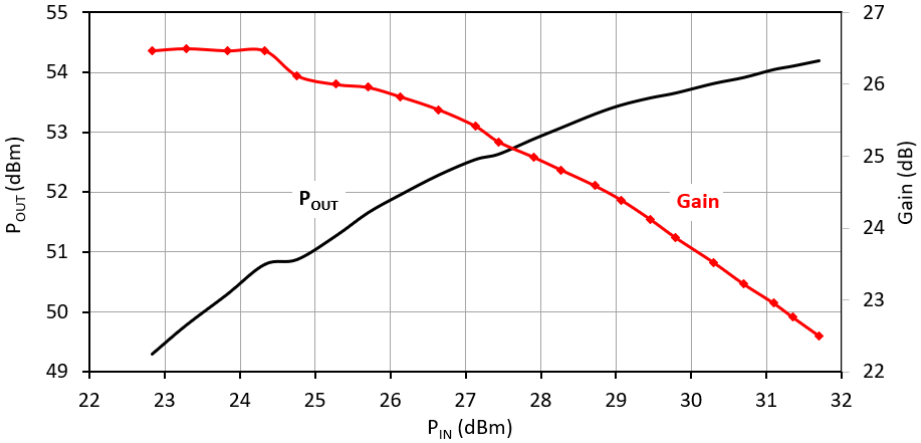


(c) Output reflection coefficient

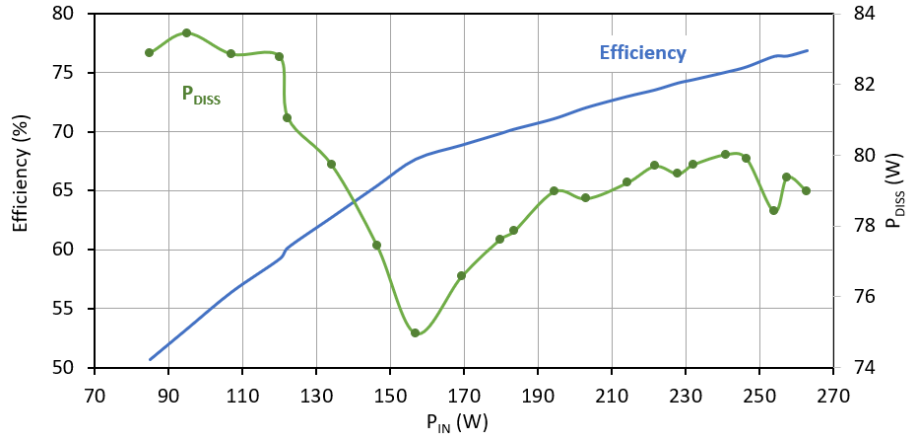


(d) Assembled PA

Figure 7.19: S-parameter measurements of power amplifier (red: simulation, black: measurement)

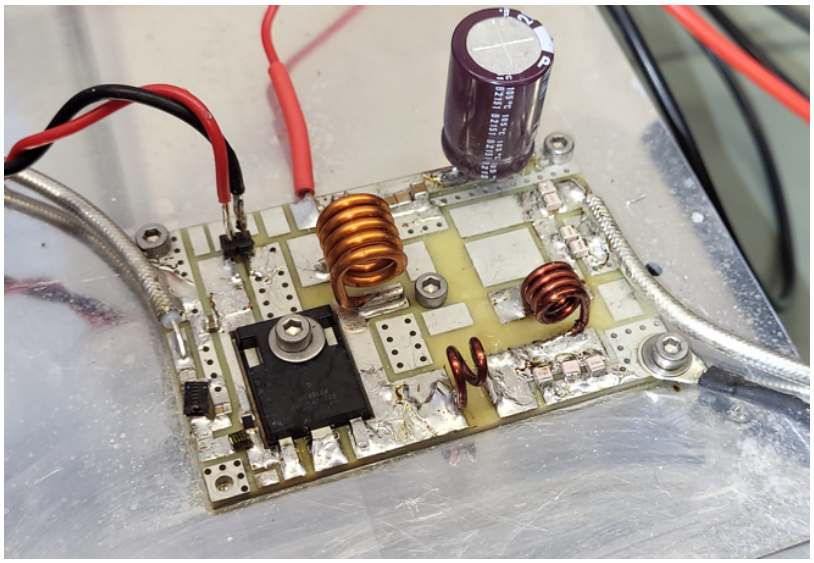


(a) Output power and gain of PA

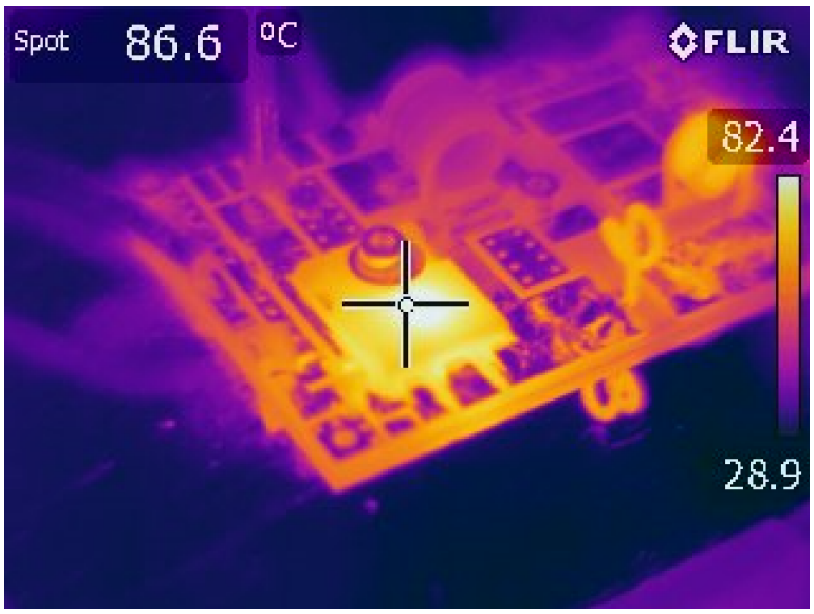


(b) Efficiency and power dissipation of PA

Figure 7.20: Large-signal performance of 250 W power amplifier



(a) Power amplifier with new L_{21} and L_{22} coils



(b) Thermal image after 30 min of continuous operation

Figure 7.21: Pictures of improved PA and measurement of case temperature

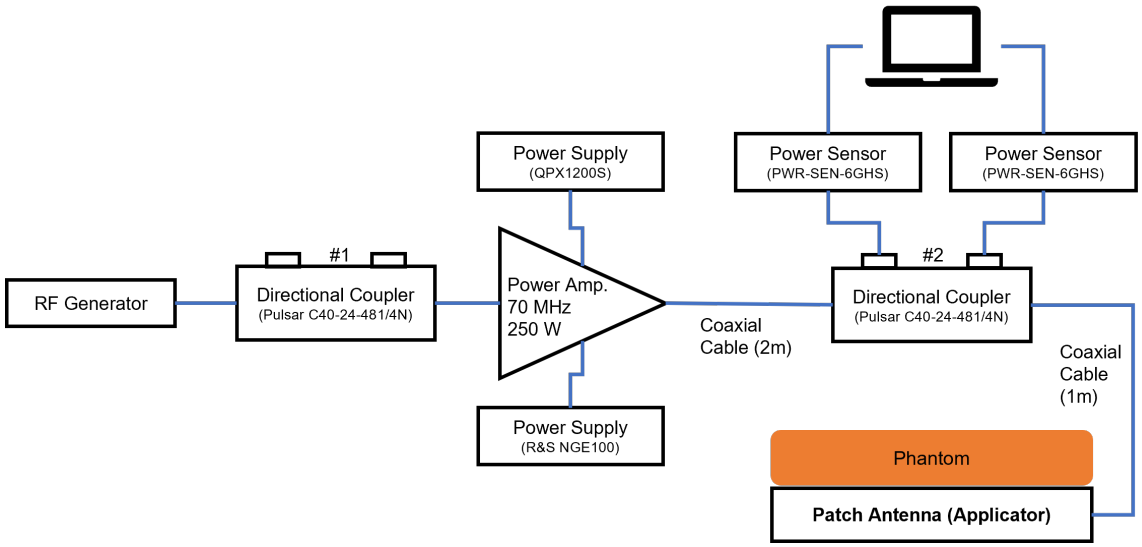


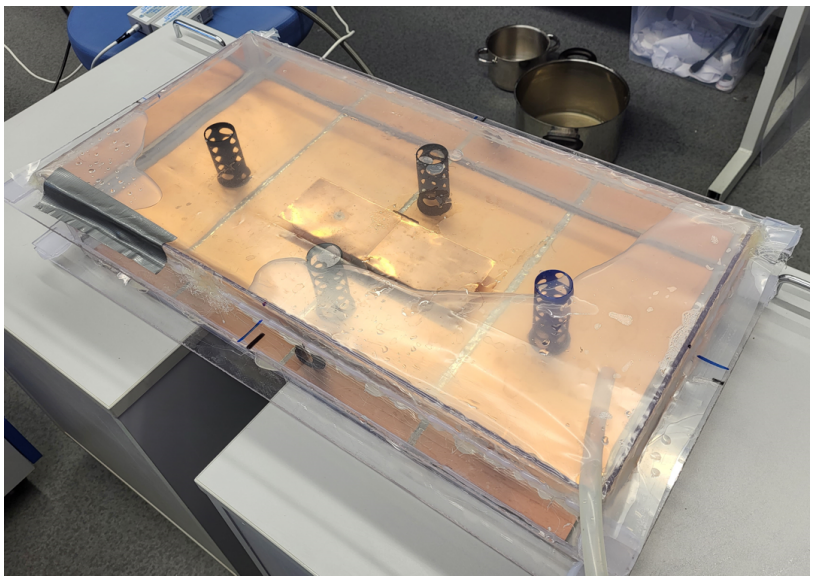
Figure 7.22: Block diagram for test setup with phantom

Table 7.5: Results of experiments using agar phantom

Round 1	t (min)	$T_{phantom}$ (°C)	P_{out} (W)	P_{ref} (W)	T_{case} (°C)	Eff. (%)
t_0	0	25	248.7	37.2	81.8	67.6
t_f	6	29	257.0	37.0	102.0	69.0
Round 2	t (min)	$T_{phantom}$ (°C)	P_{out} (W)	P_{ref} (W)	T_{case} (°C)	Eff. (%)
t_0	0	25	257.4	45.4	108	68.2
t_f	3	27	260.4	45.6	116	68.6

the antenna-phantom arrangement needs to be re-assembled before the next round. The measured return loss for experiment number 1 was 8.5 dB, whereas for experiment number 2 was 7.5 dB, which would translate into a 14% and 18% reflected power respectively. This difference in input reflection coefficient can be explained by the water refilling process and re-positioning of the phantom layers for each experiment, which causes variations on the antenna-phantom arrangement. Images of the temperature measurement of the phantom layer closest to the applicator are shown in figure 7.24. A reference metallic frame (320 mm x 230 mm) is positioned on the phantom every time before performing the temperature reading, so that the measurement is always performed at the center. This $4°C$ increase is observed after a heating time of 6 min.

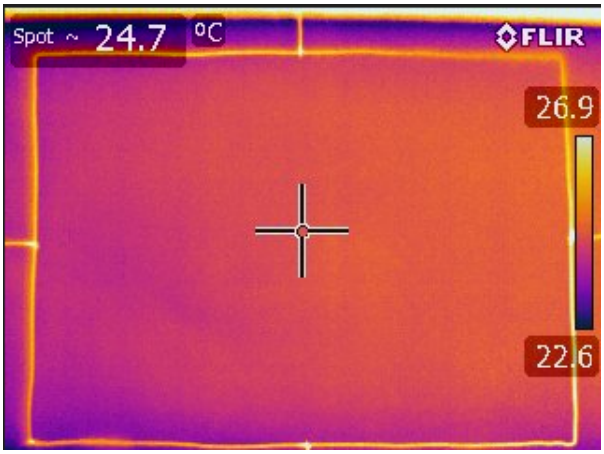
In each round following is measured: the initial and final incident and reflected power, the transistor case temperature and the drain current (to determine the drain efficiency). Two obvious observations regarding the power amplifier are: 1) the operating case temperature reaches and goes above 100°C and 2) the efficiency degrades ($\approx$ 9% points degradation). As previously shown, under much better loading conditions the amplifier reaches close to 77% efficiency and the temperature never exceeds the 90°C for an output power of about



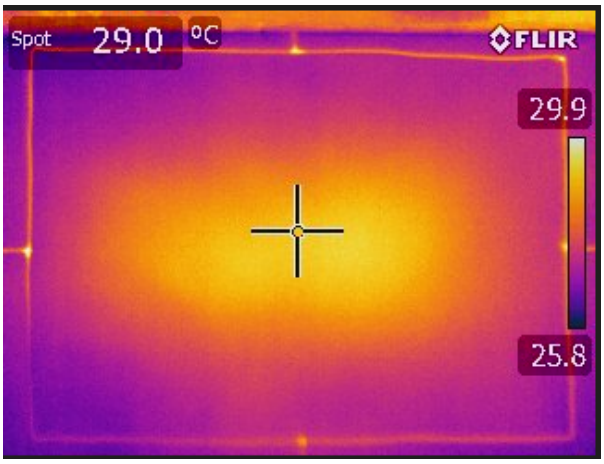
(a) Picture of patch antenna

(b) Picture of phantom

Figure 7.23: Patch antenna with and without phantom



(a) Thermal image before heating



(b) Thermal image after heating

Figure 7.24: Thermal images taken during experiments with phantom

260 W. On the other side, the experiments showed the capability of the PA to deliver enough power to heat the phantom.

8 Conclusions and Outlook

In this work the topic of highly efficient power amplification is studied. Emphasis is given to the class-E power amplifier, a well established concept, which after so many years of its invention in the mid seventies, is still considered a topic of importance within the research and industry community. The advances in semiconductor technology and more specifically the development of GaN HEMT devices, offering higher power density, higher breakdown voltage and higher thermal conductivity, have opened new possibilities for this power amplifier concept. In this thesis work, theoretical aspects in relation to class-E amplifiers are reviewed and power amplifier demonstrators have been simulated, fabricated and measured to validate the proposed concepts. The contributions of this work can be summarized as follows:

- Performing analysis to evaluate the maximum operating frequency of a class-E power amplifier as a function of the design parameter q and of the output capacitance (C_{out}) of the transistor. This allows the designer to understand the design space for class-E power amplifiers and to for instance, determine the maximum acceptable output capacitance for a specific value of the parameter q given the frequency of operation, desired output power and supply voltage.

- Further, a simplified analysis of the class-E amplifier in the frequency domain has been carried out, to evaluate the possibility of compensating excessive output capacitance. This analysis has shown that a frequency-dependent inductor is required to compensate excessive capacitance not only at the fundamental frequency but also at the harmonic components. A so-called *excess factor* (α) is introduced and equations to calculate the required driving-point impedance seen at the C_{out} plane are derived as a function of this new parameter. Moreover, in order to model the response of the frequency-dependent inductor an equivalent circuit composed of an inductor in series with two parallel LC resonators is proposed here. Equations to determine the values of these components as a function of α and of the resonance frequency of the resonators are derived. The number of resonators defines up to which harmonic the capacitance compensation will occur and therefore equations for a single and for a dual-resonator topology are derived. In this work, the classical class-E amplifier topology is extended by introducing those equivalent circuits.

- Exploring excess capacitance compensation at microwave frequencies. In this respect, performed a computer-aided analysis of class-E amplifiers using *Frequency Dependent Inductive Compensation* (FDIC), a term introduced in this work, to refer to a class-E PA having a frequency-dependent excess capacitance compensation mechanism. The analytical approach to solve the class-E amplifier circuit, although very useful, requires a lot of simplifications for it to be tractable. One of the main assumptions is that the transistor behaves like a switch. To make the analysis more

realistic, in this work a simplified large-signal model for a GaN HEMT device is extracted. The model uses a voltage-controlled current source and non-linear models for the gate-source and gate-drain capacitances. The different components in the model are implemented by using so-called *Symbolically-Defined Devices* (SDD), which are blocks containing the equations for each component. Using this model allows us to account for non-ideal switching behavior, saturation resistance, feedback capacitance and capacitance voltage-dependency. The waveforms of the class-E amplifier below and above the maximum operating frequency are studied and the limitations of FDIC discussed. This study reveals, that not only the output capacitance but also the feedback capacitance, which can not be compensated by FDIC, limits class-E optimum operation. Design equations for designing an FDIC-Class-E using a generalized transmission line network are derived in this thesis.

- Investigating power amplifiers for hyperthermia systems. This thesis also studied more practical aspects related to the requirements of power amplifiers for this specific medical application. The design of a 100 W amplifier for regional hyperthermia operating at 70 MHz is presented. The emphasis here is on system design considerations, such as required drive power and gain, losses in the amplifying path, etc. This power amplifier module was used in initial RF hyperthermia experiments. Following this, the design of a 250 W amplifier as successor of the pre-designed 100 W module is discussed. Two design approaches are compared: the first one makes use of the classical class-E design equations to create a first design, which is evaluated via simulation. The second approach is based on load-pull simulations. Intrinsic waveforms are evaluated to understand the high-efficiency mode of operation and to guide the design process. One of the main design considerations to be taken into account is the DC drain breakdown voltage. High-efficiency operating modes are characterized by high peak voltages, going beyond the conventional $2 \cdot V_{suppy}$. Literature suggests that the RF breakdown voltage is higher than the corresponding DC one and inspection of the device manufacturer data seems to indicate that devices might be driven at peak voltages beyond the DC breakdown rating. Manufactures of RF transistors do not publish data on RF breakdown voltage, and further investigation is required to understand the limits of operation of the device. In the final section of this work, RF heating experiments using an agar phantom are performed to evaluate the capability of the PA to deliver enough power under close-to-real conditions.

Class-E power amplifiers are still an attractive concept for microwaves but require the use of GaN HEMTs for the reasons previously discussed. The classical time-domain analysis is of limited use at microwaves but still relevant at low frequencies. Good large-signal models are a need to predict PA performance and to be able to study generated waveforms to help guiding the design process. At low frequency (sub-GHz) classical class-E design equations might help to get initial design values, which can be optimized via simulation. A transistor not behaving like a switch can not generate the classical class-E waveforms, nevertheless, smoothed waveforms resembling the classical case can be obtained. The non-switched operation also implies that a pure class-E is not obtained and therefore hybrid modes will occur. In the work presented in this thesis, it was observed that driving conditions and loading can shape the current in such a way that a quasi-class-E response shifts to a class-J

power amplifier response.

Additional research is required to understand transistor maximum RF breakdown voltage, specially in LDMOS, in which a highly-efficient PA design causes peak voltages beyond the DC breakdown rating. Non-optimum matching of the PA, as for instance when driving a loaded hyperthermia applicator, causes reflections which might rise the peak voltage of the device even further. Operation under non-matched conditions was not addressed in this thesis and needs to be investigated in future works streams. The design of high-efficiency power amplifiers involves designing the appropriate harmonics terminations to obtain the desired waveform shaping. In this respect, the designer needs to take into account the harmonic terminations provided by the load and create a design less susceptible to these impedances. The input impedance of the patch antenna applicator used in the hyperthermia experiments was highly reflective at $2f_0 = 140$ MHz and $3f_0 = 210$ MHz, but the designed low-pass output matching network was insensitive to these impedance terminations, therefore the efficiency of the power amplifier did not decay dramatically. An interesting approach for future research, is the possibility of including the highly reactive harmonic impedances of the applicator in the PA design. This requires a better understanding of the applicator design in order to perform a co-design of the PA-Applicator pair. This might open the possibility of integrating the PA and the applicator into a single unit.

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Appendix A

.1 Efficiency in class-B PA with resistive load

Let the following simplified circuit represent a device operating under class-B conditions

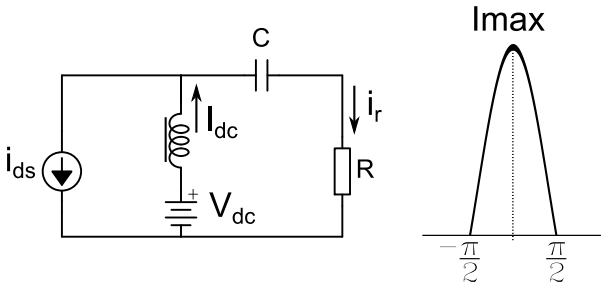


Figure .1: current source representing class-B amplifier

The efficiency can be calculated as follows:

$$\eta = \frac{P_{out}}{P_{dc}} = \frac{i_{r(rms)}^2 \cdot R}{V_{dc} \cdot I_{dc}} \tag{.1}$$

where $i_r(\theta) = I_{dc} - i_{ds}(\theta)$, and the expression for the half sinusoidal drain current is given by

$$i_{ds}(\theta) = \begin{cases} I_{max} \cdot cos(\theta) & if\ |\theta| \leq \Phi/2 \\ 0 & otherwise \end{cases} \tag{.2}$$

and the current through R can be written as

$$i_r(\theta) = \begin{cases} I_{dc} - I_{max} \cdot cos(\theta) & if\ |\theta| \leq \Phi/2 \\ I_{dc} & otherwise \end{cases} \tag{.3}$$

the DC and fundamental component of the drain current $i_{ds}(\theta)$ are obtained by Fourier decomposition [27]

$$I_{dc} = \frac{I_{max}}{\pi} \tag{.4}$$

$$I_1 = \frac{I_{max}}{2} \tag{.5}$$

Now calculating the root mean square value of the resistor current

$$\begin{aligned} i_{r(rms)}^2 &= \frac{1}{2\pi}\int_{-\pi/2}^{\pi/2} i_r^2(\theta)\cdot d\theta \\ &= \frac{1}{2\pi}\left[\int_{-\pi/2}^{\pi/2}\left(\frac{I_{max}}{\pi} - I_{max}\cdot cos(\theta)\right)\cdot d\theta + \int_{\pi/2}^{3\pi/2}\left(\frac{I_{max}}{\pi}\right)^2\cdot d\theta\right] \\ &= \frac{1}{2\pi}\left[\left(-3\frac{I_{max}^2}{\pi} + \pi\frac{I_{max}^2}{2}\right) + \left(\frac{I_{max}^2}{\pi}\right)\right] \\ &= (\pi^2-4)\left(\frac{I_{max}}{2\pi}\right)^2 \end{aligned} \tag{.6}$$

The optimum load resistance is the quotient of the fundamental components of the drain voltage and current, i.e.

$$R = \frac{V_1}{I_1} = \frac{V_{dc}}{I_{max}}\left(\frac{\pi}{\pi-1}\right) \tag{.7}$$

where the following expression for the fundamental component of the drain voltage (for zero knee voltage) has been used [27]

$$V_1 = \frac{V_{dc}}{2}\cdot\left(\frac{\pi}{\pi-1}\right) \tag{.8}$$

Now using equation .1 together with .6 and .7 to evaluate the efficiency

$$\begin{aligned} \eta &= \frac{(\pi^2-4)\left(\frac{I_{max}}{2\pi}\right)^2\cdot\frac{V_{dc}}{I_{max}}\left(\frac{\pi}{\pi-1}\right)}{V_{dc}\cdot\frac{I_{max}}{\pi}} \\ &= \frac{1}{4}\cdot\left(\frac{\pi^2-4}{\pi-1}\right) = 0.685 \end{aligned} \tag{.9}$$

Please note the this value of efficiency ($\eta = 68.5\%$) differs from the 58% (knee voltage neglected) encontered in [27]. This results from using only the fundamental components for the calculation, as opposed here where the rms value of real current waveform (non sinusoidal) at the load side have been used instead.

Appendix B

.1 System of Equations for Finite Feed Class E

Let us define the following variables

$$
\begin{aligned}
x_1 &= sin(q \cdot \pi) && (.10)\\
x_2 &= cos(q \cdot \pi) && (.11)\\
x_3 &= -sin(q \cdot \pi) + \pi \cdot q \cdot cos(q \cdot \pi) && (.12)\\
x_4 &= \frac{q}{q^2 - 1} && (.13)\\
x_5 &= 2q^2 - 1 && (.14)\\
x_6 &= -cos(q \cdot \pi) - \pi \cdot sin(q \cdot \pi) && (.15)\\
x_7 &= cos(2 \cdot q \cdot \pi) && (.16)\\
x_8 &= sin(2 \cdot q \cdot \pi) && (.17)
\end{aligned}
$$

The coefficients A_i and B_i of the two equations required to determine p and φ are given as follows

$$
\begin{aligned}
A_1 &= 1 + x_6 \cdot x_7 + x_3 \cdot x_8 && (.18)\\
A_2 &= q \cdot x_4 \cdot (x_2 \cdot x_7 + x_1 \cdot x_8 + 1) && (.19)\\
A_3 &= x_4 x_5 (x_1 \cdot x_7 - x_2 \cdot x_8) && (.20)\\
B_1 &= q \cdot (x_3 \cdot x_7 - x_6 \cdot x_8) && (.21)\\
B_2 &= q^2 \cdot x_4 \cdot (x_1 \cdot x_7 - x_2 \cdot x_8) && (.22)\\
B_3 &= -q \cdot x_4 \cdot (x_1 \cdot x_5 \cdot x_8 + x_2 \cdot x_5 \cdot x_7 + 1) && (.23)
\end{aligned}
$$

and the system of equations is given by

$$
\begin{aligned}
A_1 + A_2 \cdot p \cdot cos(\varphi) + A_3 \cdot p \cdot sin(\varphi) &= 0 && (.24)\\
B_1 + B_2 \cdot p \cdot cos(\varphi) + B_3 \cdot p \cdot sin(\varphi) &= 0 && (.25)
\end{aligned}
$$

This system is solved for $p \cdot sin(\varphi)$ and $p \cdot cos(\varphi)$ to obtain

$$
\begin{aligned}
p \cdot sin(\varphi) &= \frac{B_1 \cdot A_2 - A_1 \cdot B_2}{B_2 \cdot A_3 - A_2 \cdot B_3} = Ps && (.26)\\
p \cdot cos(\varphi) &= \frac{A_3 \cdot B_1 - A_1 \cdot B_3}{A_2 \cdot B_3 - A_3 \cdot B_2} = Pc && (.27)
\end{aligned}
$$

therefore

$$\varphi = atan(\frac{Ps}{Pc}) \tag{.28}$$

$$p = \frac{Ps}{sin(\varphi)} = \frac{Pc}{cos(\varphi)} \tag{.29}$$

Appendix C

.1 Equations for two-resonator network

$$L_1 = \frac{L(\alpha^2 + 2\alpha(\gamma_2 + \gamma_3) + 4\gamma_2\gamma_3)}{\gamma_2\gamma_3(18\alpha^3 + 49\alpha^2 + 28\alpha + 4)} \tag{.30}$$

$$L_2 = \frac{\alpha L(\alpha + 2\gamma_3)(-36\gamma_2^3 + 49\gamma_2^2 - 14\gamma_2 + 1)}{\gamma_2(\gamma_2 - \gamma_3)(18\alpha^3 + 49\alpha^2 + 28\alpha + 4)} \tag{.31}$$

$$L_3 = \frac{\alpha L(\alpha + 2\gamma_2)(36\gamma_3^3 - 49\gamma_3^2 + 14\gamma_3 - 1)}{\gamma_3(\gamma_2 - \gamma_3)(18\alpha^3 + 49\alpha^2 + 28\alpha + 4)} \tag{.32}$$

$$C_2 = \frac{\gamma_2}{\omega_0^2 L_2} \tag{.33}$$

$$C_3 = \frac{\gamma_3}{\omega_0^2 L_3} \tag{.34}$$

with L representing the optimum value of inductor in the classical PC-Class-E obtained from (5.12) and the following two parameters:

$$\gamma_2 = \left(\frac{\omega_0}{\omega_2}\right)^2 \tag{.35}$$

$$\gamma_3 = \left(\frac{\omega_0}{\omega_3}\right)^2 \tag{.36}$$

whereby γ_2 and γ_3 are limited to the following range:

$$\frac{1}{4} < \gamma_2 < 1 \text{ and } \frac{1}{9} < \gamma_3 < \frac{1}{4} \tag{.37}$$

.2 Equations for $L_1L_2C_2$ network for variable q

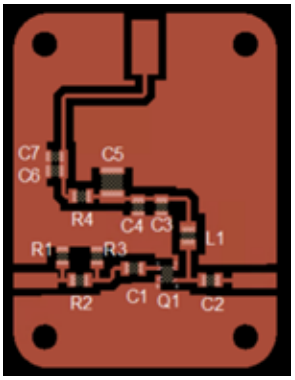
$$L_1 = \frac{q^2 L(q^2\gamma + \alpha)}{\gamma(4\alpha^2 + 5\alpha q^2 + q^4)} \tag{.38}$$

$$L_2 = -\frac{q^2\alpha L(4\gamma^2 - 5\gamma + 1)}{\gamma(4\alpha^2 + 5\alpha q^2 + q^4)} \tag{.39}$$

$$C_2 = \frac{\gamma}{\omega_o^2 L_2} \tag{.40}$$

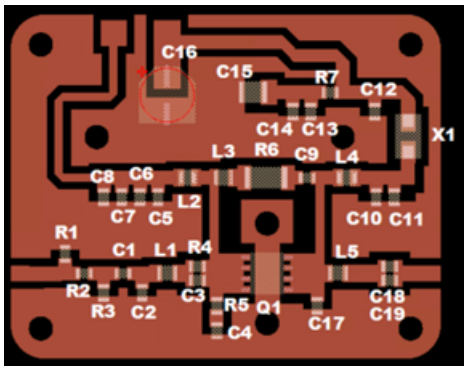
Appendix D

.1 BOM Gain block



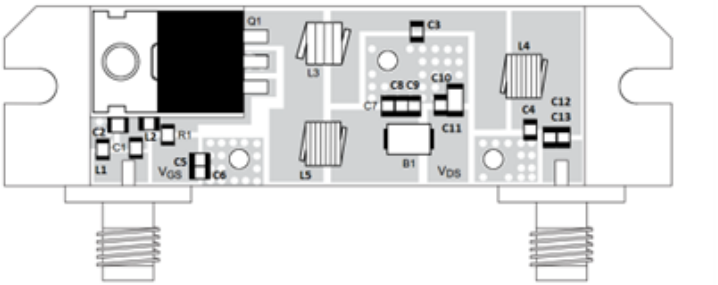
Part	Description	Part Number	Manufacturer	Ordering
R1, R3	100 Ohm resistor, 0805	ERJ-U06J101V	Panasonic	667-ERJ-U06J101V
R2	66.5 Ohm resistor, 0805	ERJ-6ENF66R5V	Panasonic	667-ERJ-6ENF66R5V
R4	68 Ohm resistor, 0805	ERJ-U06J680V	Panasonic	667-ERJ-U06J680V
C1, C2	8.2 nF chip capacitor, 0805	08053C822KAT2A	AVX	581-08053C822KAT2A
C3	100 pF chip capacitor, 25V, 0805	08052A101KAT2A	AVX	581-08052A101KAT2A
C4	1000 pF chip capacitor, 0805	08052C102M4T2A	AVX	581-08052C102M4T2A
C5	2.2 uF chip capacitor, 1210	12101C225KAT4A	AVX	581-12101C225KAT4A
C6, C7	NU			
L1	270 nH chip inductor, 0.42A, 0805	805HP-271XGRB	Coilcraft	994-0805HP-271XGRB
Q1	Broadband MMIC Amplifier, SOT343	BGA614H6327XTSA1	Infineon Technologies	726-BGA614H6327XTSA1

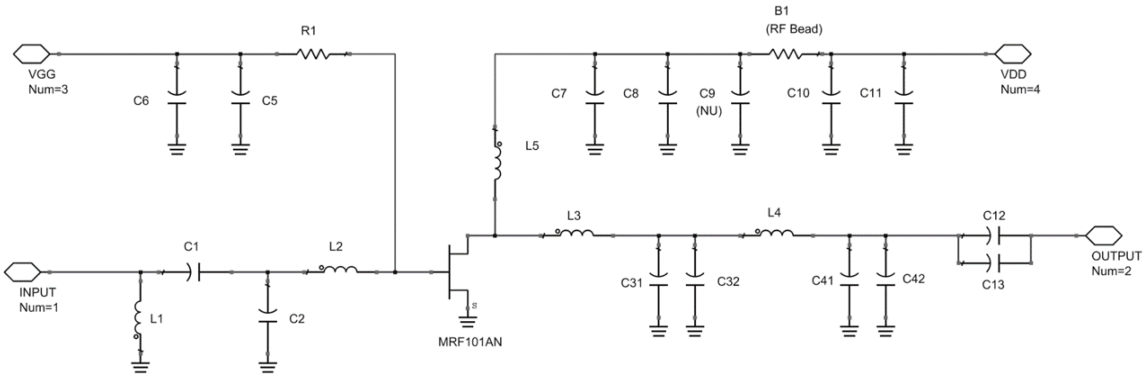
.2 BOM Pre-Driver



Part	Description	Part Number	Manufacturer	Mouser P/N
R1, R3	430 Ohm resistor, 0805	ERJ-6ENF4300V	Panasonic	667-ERJ-6ENF4300V
R2	12 Ohm resistor, 0805	ERJ-6GEYJ120V	Panasonic	667-ERJ-6GEYJ120V
R4	16 Ohm resistor, 0805	ERJ-6GEYJ160V	Panasonic	667-ERJ-6GEYJ160V
R5	100 Ohm resistor, 0805	ERJ-U06J101V	Panasonic	667-ERJ-U06J101V
R6	1.2 kOhm resistor, 1W, 2010	CRGH2010J1K2	TE Connectivity / Holsworthy	279-CRGH2010J1K2
R7a	0.33 Ohm resistor, 0.25W, 0805	ERJ-U6QFR33V	Panasonic	667-ERJ-U6QFR33V
R7b	0 Ohm resistor, 0805	ERJ-6GEY0R00V	Panasonic	667-ERJ-6GEY0R00V
C1	820 pF chip capacitor, 0805	08051C821J4T2A	AVX	581-08051C821J4T2A
C2	2.2 pF chip capacitor, 0805	08051A2R2DAT2A	AVX	581-08051A2R2DAT2A
C3	15 pF chip capacitor, 0805	08052A150JAT2A	AVX	581-08052A150JAT2A
C4, C9	330 pF chip capacitor, 0805	08055C331K4Z2A	AVX	581-08055C331K4Z2A
C5, C10, C18, C19	470 pF chip capacitor, 1210	08051A471K4T4H	AVX	581-08051A471K4T4H
C6, C13	0.01 uF chip capacitor, 0805	FS051C103K4Z2A	AVX	581-FS051C103K4Z2A
C7, C14	0.1 uF chip capacitor, 0805	08051C104J4T4A	AVX	581-08051C104J4T4A
C8	1 uF chip capacitor, 0805	08051C105K4T2A	AVX	581-08051C105K4T2A
C11, C12	1000 pF chip capacitor, 0805	08052C102M4T2A	AVX	581-08052C102M4T2A
C15	1 uF chip capacitor, 1210	12101C105KAT2A	AVX	581-12101C105KAT2A
C16	100 uF, Al electrolytic capacitor, SMD 35V, 6.3x7.7mm	EEE-TQV101XAP	Panasonic	667-EEE-TQV101XAP
C17	1.8 pF chip capacitor, 0805	08051A1R8DAT2A	AVX	581-08051A1R8DAT2A
L1	18 nH chip inductor, 1.2A, 0805	0805HP-18NXGRB	Coilcraft	994-0805HP-18NXGRB
L2	680 nH chip inductor, 0.6A, 0805	0805AF-681XJRB	Coilcraft	994-0805AF-681XJRB
L3	33 nH, chip inductor, 1.1A, 0805	0805HP-33NXGRB	Coilcraft	994-0805HP-33NXGRB
L4	680 nH, chip inductor, 590mA, 0805	0805LS-681XJLC	Coilcraft	994-0805LS-681XJLC
L5	6.8 nH, chip inductor, 1.3A, 0805	0805HP-6N8XJRB	Coilcraft	994-0805HP-6N8XJRB
X1	Ferrite 43 SM, 47Ohm@100Mhz	2743019447	Fair-Rite	623-2743019447LF
Q1	GaN HEMT, DC-6GHz	NPTB00004A	MACOM	937-NPTB00004A

.3 BOM Final Stage





Part	Description	Part Number	Manufacturer	Ordering
L1	39 nH inductor, 1.1A, 0805	0805HQ-39NXJLB	Coilcraft	994-0805HQ-39NXJLB
L2	82 nH inductor, 0.82A, 0805	0805HP-82NXJRB	Coilcraft	994-0805HP-82NXJRB
L3	handmade, Dwire = 0.6 mm, Dcoil = 4.1 mm (outer), N = 4, L = 7.3 mm			
L4	130 nH inductor, 5.4A, 2222 (coil stretched, L = 9.4 mm)	2222SQ-131GEC	Coilcraft	994-2222SQ-131GEC
L5	130 nH inductor, 5.4A, 2222	2222SQ-131GEC	Coilcraft	994-2222SQ-131GEC
C1	390 pF chip capacitor, 25V, 0805	08053A391JAT2A	AVX	581-08053A391JAT2A
C2	270 pF chip capacitor, 50V, 0805	08055C271K4T2A	AVX	581-08055C271K4T2A
C3=C31||C32	56pF||56 pF chip capacitor, 1111	1111C560JP501	PPI	
C4=C41||C42	20pF||22pF chip capacitor, 1111	1111C200JP501 1111C220JP501	PPI	
C5, C7, C8, C12, C13	510 pF chip capacitor, 100V, 0805	GRM2165C2A511JA01D	Murata	81-GRM2165C2A511JA1D
C6	1 uF chip capacitor, 100V, 0805	08051C105K4Z2A	AVX	581-08051C105K4Z2A
C9	NU			
C10	0.01 uF chip capacitor, 100V, 0805	FS051C103K4Z2A	AVX	581- FS051C103K4Z2A
C11	1 uF chip capacitor, 100V, 1206	C3216X7R2A105K160AA	TDK	810-C3216X7R2A105K
R1	75 Ohm chip resistor, 0.5W, 0805	SG73P2ATTD75R0F	KOA Speer	660-SG73P2ATTD75R0F
B1	43 SM Bead, Z=47Ohm@100MHz, 10A, 5.1mmx3.05mmx2.85mm (LxWxH)	2743019447	Fair.Rite	623-2743019447LF
Q1	RF Power LDMOS Transistor	MRF101AN	NXP	771-MRF101AN
PCB	FR4 0.09 in., er=4.8, 2 oz. Copper			

Appendix E

.1 Equivalent output circuit of MRF300AN and intrinsic waveforms

An L network composed of a shunt capacitor and a series lossy inductor can be used to represent the output of the transistor. The capacitor represents the voltage-dependent drain-source capacitance of the device and the lossy inductor the bond wires connecting the transistor chip to the package lead. To obtain the values of this lumped-element components, following procedure was performed:

1. S-parameter simulations using the large-signal model of the device are performed (see figure .3a). The maximum simulation frequency is set to 1 MHz and the gate voltage equal to zero[1] ($V_{gs} = 0$ V). Biasing below threshold ensures that the output current source is off and the transistor is behaving as a passive network. Frequencies below 1 MHz guarantee that the transistor capacitances dominate the input impedance over inductive and resistive components.

2. Calculate the admittances $\underline{y}_{11}$, $\underline{y}_{12}$, and $\underline{y}_{22}$ from the S-parameters.

3. Calculate the capacitances as follows ($\omega = 2\pi f_0$, with $f_0 = 1$ MHz):

$$C_{gd} = -\Im(\underline{y}_{12})/(\omega) \tag{.41}$$
$$C_{gs} = \Im(\underline{y}_{11})/(\omega) - C_{gd} \tag{.42}$$
$$C_{ds} = \Im(\underline{y}_{22})/(\omega) - C_{gd} \tag{.43}$$

4. Sweep the drain voltage V_{ds} to obtain $C_{ds}(V_{ds})$. The red trace in figure .4 shows $C_{ds}(V_{ds})$ for the MRF300AN. The black dots show the result of a curve fitting.

5. Now bias the device under *cold-fet* conditions, i.e., $V_{gs} = 0$ V and $V_{ds} = 0$ V and run again the S-parameter simulation (same circuit from figure .3a) .

6. To understand the next step, let's review the behavior of the transistor when biased in the cold-fet condition. Figure .5a shows the equivalent circuit for this biasing condition[2]. In the previous steps the capacitances were determined, now the remaining components will be obtained.

7. The equivalent circuit to calculate $\underline{z}_{22}$ (open-circuit output impedance) is now shown in figure .5b. This series inductance can be obtained from the resonance frequency of the circuit and the series resistor from the impedance value at resonance.

[1] The thershold voltage of the MRF300AN is larger than 2 V

[2] As a first order approximation, the resistances in series with C_{gs} and C_{gd} are neglected here

8. Use the simulated S-parameters in cold-fet condition to calculate the impedances $\underline{z}_{11}$ and $\underline{z}_{22}$ and to plot their magnitude and phase.

9. The circuit in figure .3b shows the simulation environment including the equivalent resonant circuits for the gate and for the drain side.

10. Figure .6 shows $\underline{z}_{22}$ extracted from the S-parameters using the transistor model and from the equivalent $L - C$ circuit.

11. The equivalent bondwire inductance for the drain side is approximately $L_b = 1.2$ nH. The series resistance seems to be negligible.

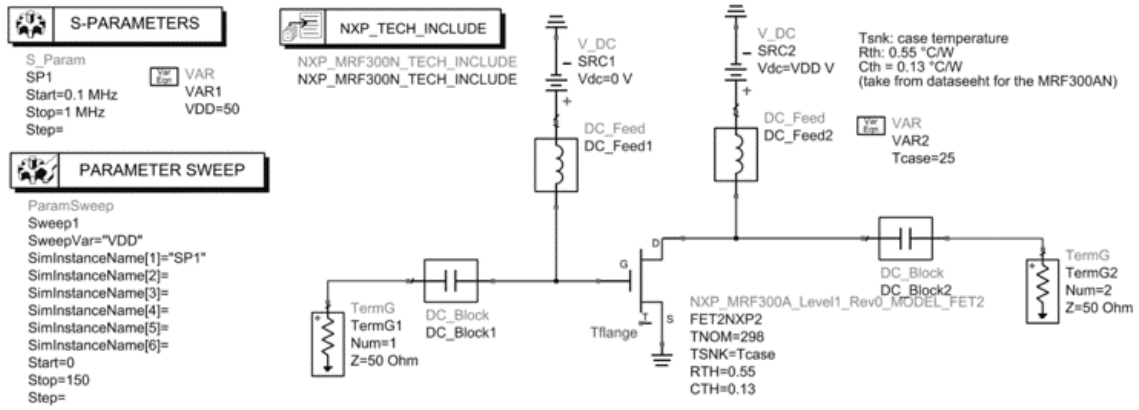
When running a large-signal simulation, following equations can be used to calculate the intrinsic voltage and current waveforms:

$$v_{drain}^{int}(\omega t) = v_{drain}(\omega t) - j\omega L_b \cdot i_{drain}(\omega t) \tag{.44}$$
$$i_{drain}^{int}(\omega t) = i_{drain}(\omega t) - j\omega C_{ds} \cdot v_{ds}^{int}(\omega t) \tag{.45}$$

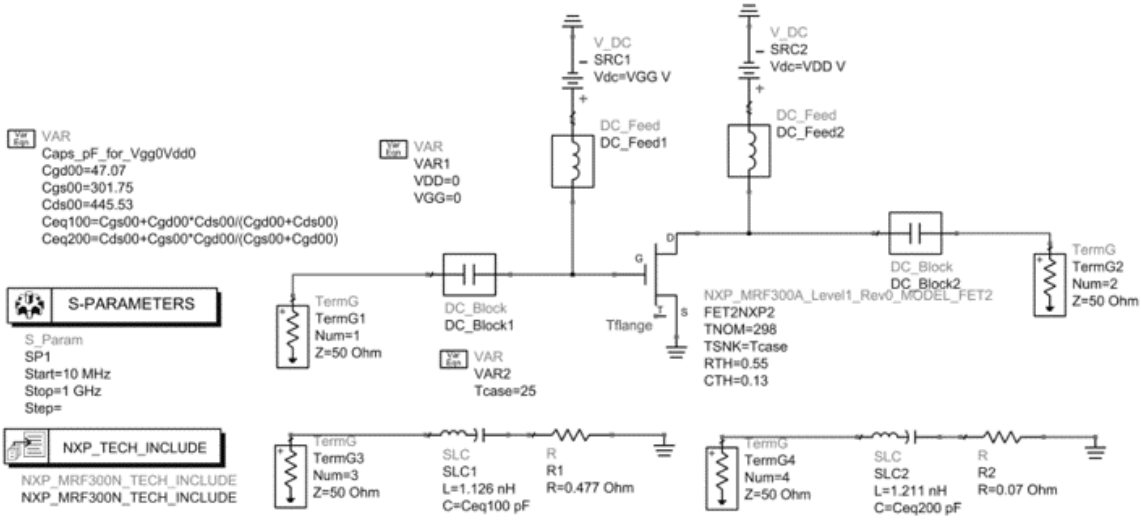
For more complex output networks, the ABCD matrix of the 2-port can be calculated within the simulation environment and used to calculate the intrinsic waveforms. To do so, include the circuit in figure .7 within the harmonic balance (large-signal) simulation environment in ADS, place the output network between the "Cds-plane" and the "Lead plane" and use following equations (refer to figure .7 for the variables below)[3]:

$$A = \frac{V_{1O}}{V_{2O}} \tag{.46}$$
$$B = \frac{V_{1S}}{I_{2S}} \tag{.47}$$
$$C = \frac{I_{1O}}{V_{2O}} \tag{.48}$$
$$D = \frac{I_{1S}}{I_{2S}} \tag{.49}$$
$$V_{int} = A \cdot V_{drain} - B \cdot I_{drain} \tag{.50}$$
$$I_{int} = C \cdot V_{drain} - D \cdot I_{drain} \tag{.51}$$

[3] C_{ds} in the output network is voltage dependent: $C_{ds}(V) = (10^{-12})(C + A/\sqrt{D \cdot V + B})$ with $A = 1325$, $B = 12.637$, $C = 28$ and $D = 5.77$



(a) Circuit for obtaining transistor capacitanes



(b) Circuit for obtaining transistor inductances

Figure .3: Circuits to obtain the intrinsic capacitors and inductors

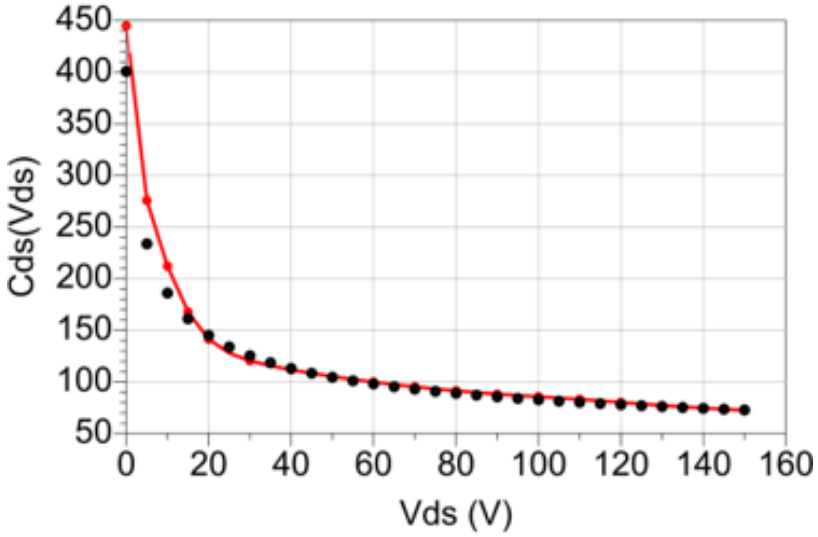
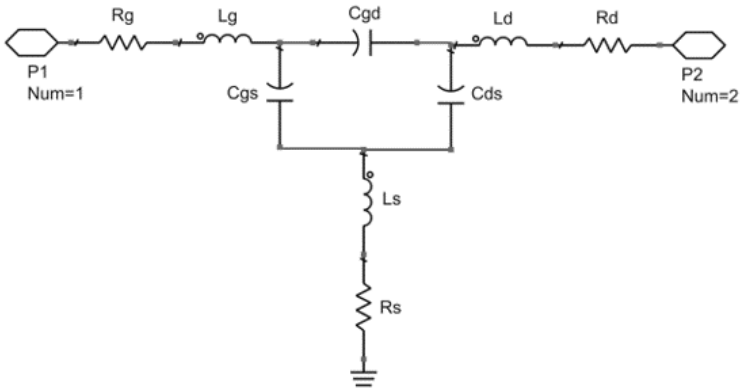
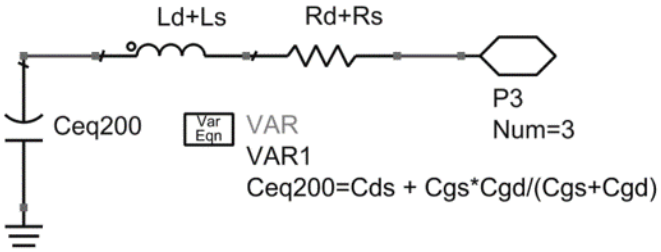


Figure .4: Drain-source capacitance vs. voltage

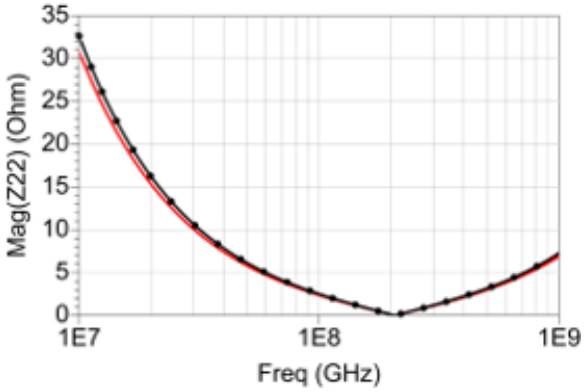


(a) Cold-Fet equivalent circuit

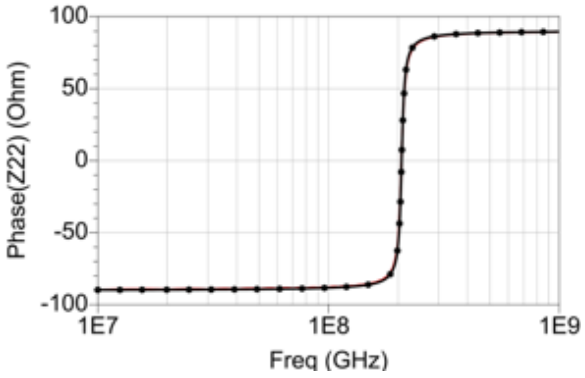


(b) Equivalent circuit to calculate z_{22}

Figure .5: Circuits for the cold-fet condition



(a) $|\underline{z}_{22}|$



(b) $\angle \underline{z}_{22}$

Figure .6: Magnitude and phase of $\underline{z}_{22}$

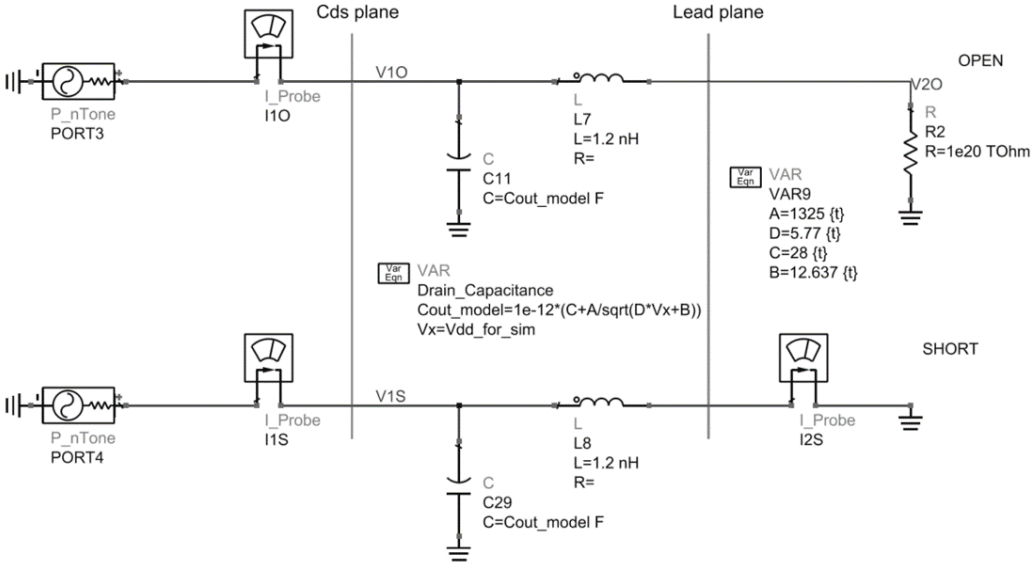


Figure .7: Circuit to calculate the ABCD matrix in the simulation

Appendix F

.1 Publications in Impacted Journals

Related to thesis topic

1. Cumana J., Vrba J. Jr., Vrba J.: *Computer-aided design methodology for inductive compensated microwave class-E power amplifier.* In: International Journal of RF and Microwave Computer-Aided Engineering, 2021, 31. DOI: 10.1002/mmce.22910

2. Cumana, J., Grebennikov, A., Sun G., Kumar N, Jansen R. H.: *An Extended Topology of Parallel-Circuit Class-E Power Amplifier to Account for Larger Output Capacitances.* In: IEEE Transactions on Microwave Theory and Techniques, 2011, 59, 3174-3183. DOI: 10.1109/TMTT.2011.2168971

Not related to thesis topic

1. Matters-Kammerer, M., Tripodi, L., van Langevelde R.: Cumana J., Jansen R. H.: *RF Characterization of Schottky Diodes in 65-nm CMOS.* In: IEEE Transactions on Electron Devices, 2010, 57, 1063-1068. DOI: 10.1109/TED.2010.2043402

.2 Conference Publications

Related to thesis topic

1. J. Cumana, J., Narendra, A., Mediano, H,: *Voltage and Current Waveforms Analysis in C-LC Broadband High Efficiency Class-E Amplifier.* In: 2009 IEEE International Conference on Antennas, Propagation and Systems, December 2009

2. Cumana J., Lautensack C., Eickelkamp M., Goliasch J., Noculak A., Vescan A, Jansen R. H.: *Advanced Modeling of MISHFET Devices and their Performance in Current-Mode Class-D Power Amplifiers.* In: Microwave Integrated Circuit Conference, 2008. EuMIC 2008. 179-182. DOI: 10.1109/EMICC.2008.4772258

Not related to thesis topic

1. Cumana, J., Coupechoux, M., Cordero-Fuentes, J.: *Metasurface for Enhanced Millimeter-Wave Communications under Imperfect Beam Alignment.* In: IEEE International Mediterranean Conference on Communications and Networking, 2023. (**accepted for publication**)

2. Schierhorn, O., Cumana, J., Heinrich, W.: *Design of a Low-cost Broadband Dual-polarized Aperture-coupled Stacked Patch Antenna.* In: Progress in Electromagnetics Research Symposium. Institute of Electrical and Electronics Engineers, Inc., 2023. (**accepted for publication**)

3. Vrba, J., Kubeš, J., Třebický, F., Vrba, J., Vrba, D., Merunka, I., Cumana, J., Fišer, O.: *Lens Applicator for Deep-local Treatment of Cancer by Microwave Hyperthermia.* In: Progress in Electromagnetics Research Symposium. Institute of Electrical and Electronics Engineers, Inc., 2019. p. 2547-2550. ISSN 1559-9450. ISBN 9781728134031.

4. Vrba, J., Merunka, I., Cumana, J., Kubeš, J., Třebický, F., Vožech, F., Barcal, J., Vannucci,L.: *Research of Biological Effects of EM Field in Microwave Frequency Band.* In: Progress in Electromagnetics Research Symposium. Institute of Electrical and Electronics Engineers, Inc., 2019. p. 1449-1451. ISSN 1559-9450. ISBN 9781728134031.

5. Merunka, I., Vrba, D., Fišer, O., Cumana, J., Vrba, J.: *2D Microwave System for Testing of Brain Stroke Imaging Algorithms.* In: 1st European Microwave Conference in Central Europe, 2019. p. 508-511. ISBN 978-2-87487-066-8.

6. Vrba, D., Vrba, J., Fišer, O., Merunka, I., Cumana, J., Vrba, J.: *Perspective applications of microwaves in medicine.* In: 28th International Conference Radioelektronika. IEEE (Institute of Electrical and Electronics Engineers), 2018. p. 1-4. ISBN 978-1-5386-2485-2.

7. Vrba, J., Vrba, D., Fišer, O., Merunka, I., Vrba, J., Cumana, J.: *Microwave based medical imaging.* In: 32nd General Assembly and Scientific Symposium of the International Union of Radio Science, URSI GASS 2017, Montreal; Canada; Category number CFP1705I-ART; Code 132402. Institute of Electrical and Electronics Engineers, Inc., 2017. p. 1-4. Volume 2017-January. ISBN 9789082598704.