Czech Technical University in Prague
Faculty of Nuclear Sciences and Physical Engineering
Department of Physical Electronics

Master thesis

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Faculty of Nuclear Sciences and Physical Engineering
Department of Physical Electronics

Control circuit of single photon detector for space projects with improved temperature stability

Master thesis

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Consultant: **Ing. Roberta Bimbová**
Academic year: **2022/2023**

ČESKÉ VYSOKÉ UČENÍ TECHNICKÉ V PRAZE
FAKULTA JADERNÁ A FYZIKÁLNĚ INŽENÝRSKÁ
Katedra fyzikální elektroniky

ZADÁNÍ DIPLOMOVÉ PRÁCE

Student:	**Bc. Matěj S t a v i n o h a**
Studijní program:	**Fyzikální elektronika**
Specializace:	**Laserová fyzika a technika**
Akademický rok:	**2022/2023**
Název práce: (česky)	**Řídicí obvod detektoru jednotlivých fotonů pro kosmické projekty se zvýšenou teplotní stabilitou**
Název práce: (anglicky)	**Control circuit of single photon detector for space projects with improved temperature stability**
Jazyk práce:	**Angličtina**

Cíl práce:

Zlepšení parametrů stávajícího elektronického řídícího obvodu detektoru jednotlivých fotonů vedoucí ke snížení teplotní závislosti zpoždění detekce na teplotě a k možnému snížení vlastního šumu za tmy. Detektor bude navržen pro možné budoucí použití v kosmickém projektu.

Pokyny pro vypracování:

1. Seznamte se s principem a konstrukcí řídícího elektronického obvodu s pasivní teplotní kompenzací zpoždění detekce.
2. Najděte vhodný typ rychlého komparátoru pro snížení teplotní závislosti celého obvodu.
3. Navrhněte úpravu obvodu – výměnu rychlého komparátoru tak, aby bylo dosaženo teplotní závislosti menší v absolutní hodnotě než 0,25 ps/K v celém rozsahu pracovních teplot.
4. Najděte vhodný obvod pro konverzi úrovní signálů a logický obvod typu D pro dosažení vyšší rychlosti aktivního zhášení.
5. Navrhněte úpravy obvodu, zapojení a plošný spoj pro nový obvod.
6. Prověřte činnost nového řídícího obvodu společně s detekčním čipem na bázi křemíku.

Doporučená literatura:

1. Procházka I., Hamal K., Sopko B., Recent Achievements in Single Photon Detectors and Their Applications, Journal of Modern Optics 51, 9-10, 1289-1313, 2004.
2. Schreiber K. U., Procházka I, Lauber P., Hugentobler U., Schäfer W, Cacciapuoti L, Nasca R., Ground-based demonstration of the European Laser Timing (ELT) experiment, IEEE Transactions on Ultrasonics, Ferroelectrics and Frequency Control 57(3), 728-737, 2010.
3. Saleh B. E. A., Teich M. C., Základy fotoniky, svazek 3, Matfyzpress, Praha, 1995, ISBN 80-85863-05-7.
4. Cova S., Ghioni M., Lacaita A., Samori C., Zappa F., Avalanche photodiodes and quenching circuits for single-photon detection, Applied Optics 35(12), 1956-1976, 1996.
5. Procházka I., Blažej J., Fleková T., Kodet J., Silicon Based Photon Counting Detector Providing Femtosecond Detection Delay Stability, IEEE Journal of Selected Topics in Quantum Electronics, 26(2), 3900205, 2020.

Jméno a pracoviště vedoucího práce:

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Datum zadání: 17. říjen 2022

Datum odevzdání: 3. květen 2023

Doba platnosti zadání je dva roky od data zadání.

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Garant programu

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Vedoucí katedry

.....

Děkan

ČESKÉ VYSOKÉ UČENÍ TECHNICKÉ V PRAZE Fakulta jaderná a fyzikálně inženýrská

V Praze dne 17.10.2022

Declaration of Authorship

I declare that I have written the submitted work independently and that I have listed all the used literature.

In Prague, date 25.4.2023 Bc. Matěj Stavinoha

Acknowledgment

I would like to express my sincere gratitude to my supervisor, Prof. Ing. Ivan Procházka, DrSc., for his invaluable guidance and support throughout my master's program. His expertise and encouragement helped me to complete this research and write this thesis.

Bc. Matěj Stavinoha

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Abstrakt

Tato diplomová práce se zabývá optimalizací polovodičových jednofotonových detektorů, tyto typy detektorů mohou dosáhnout časového rozlišení lepšího než 20 ps a stability zpoždění výrazně lepší než 1 ps. Používají se v mnoha oblastech vědy a průmyslu nejen na Zemi, ale i ve vesmíru. Hlavním zájmem této diplomové práce je detektor vyvíjen pro "European Laser Timing", což je projekt Evropské vesmírné agentury, který má za cíl zlepšit přenos informace o času z atomových hodin, které jsou na palubě Mezinárodní vesmírné stanice, na Zemi. Cílem této diplomové práce je zlepšit teplotní stabilitu zpoždění detektoru a rychlost jeho zhášení, čehož jsem se snažil dosáhnout modernizací současné podoby řídicího obvodu detektoru. Tedy jsem vhodně upravil celé detektorové pouzdro a změřil jeho nové vlastnosti. Nový detektor vykazoval jak lepší stabilitu detekčního zpoždění, tak rychlost zhášení, proto jsem usoudil, že cíle diplomové práce byly splněny. Nakonec tato práce pokračovala nad rámec původního zadání a zkoumala také vylepšení kontinuálně běžících detektorů jednofotonových detektorů u kterých jsem srovnával různé konfigurace jejich řídícího obvodu.

Klíčová slova: Polovodičový detektor jednotlivých fotonů, Řídicí obvod, Komparátor, Stabilita detekčního zpoždění

Abstract

This master thesis deals with optimization of semiconductor single photon detectors, these kinds of detectors can achieve time resolution better than 20 ps and propagation delay stability significantly better than 1 ps. They are used in many areas of science and industry, not only on Earth, but also in space. The detector that is of main interest to this master thesis is being developed for European Laser Timing, which is a European Space Agency project meant to facilitate transmission of time information from the atomic clock aboard International Space Station to Earth. The goals of this master thesis are to improve the detector's propagation delay temperature stability and the detector's quenching speed. I

have attempted to accomplish this by modernizing the current design of the detector's control circuit. I have appropriately modified the integrated detector package and measured its novel properties. The new detector package displayed both better propagation delay stability and quenching speed, therefore I have concluded this master thesis as successful. In the end, this work proceeded beyond the scope of the thesis assignment and explored the improvement of continuously operated single photon detectors, for which I have compared different configurations of their control circuits.

Key words: Semiconductor single photon detector, Control circuit, Comparator, Propagation delay stability

Contents

Introduction

Semiconductor single photon detectors are photon counters with great precision, they are capable of detecting individual photons. These detectors can achieve single shot precision better than 20 ps and stability significantly better than 1 ps. These astonishing characteristics are the reason why these detectors find applications in many fields not only on Earth, but also in space. The most important application for the particular single photon detector that is discussed in this master thesis is the European Laser Timing (ELT), which is set to facilitate transmission of time information from atomic clock aboard the International Space Station (ISS). The detectors employed for this task need to fulfill set of strict requirements, among which is also the need for minimal and most importantly stable propagation delay. One of the major factors influencing the detection delay stability in space is temperature change. According to the projections by European Space Agency for ELT, the single photon detector orbiting Earth should experience temperature changes of ± 2 K/orbit, however the mean temperature is completely unpredictable and reliant on many factors, hence most space instruments are required to be operational in the range -55 to +50 $^{\circ}$C, and the detector's propagation delay needs to remain as stable as possible within this range. This stability is heavily influenced by the detector's electric control circuit, the most problematic component in the current design of the semiconductor single photon detector is a comparator, which exhibits nonlinear propagation delay dependency. This kind of behaviour cannot be effectively compensated for in any way and therefore the comparator should ideally be replaced with a more suitable part. One of the endeavours of this master thesis is to find and test a new comparator that could serve as a suitable replacement and improve the detectors overall propagation delay temperature stability. [1, 2, 3]

In the first chapter I will be introducing the theory and achievements of single photon counting as well as its main applications. I will also look in detail into some of European Space Agency projects where the semiconductor single photon detector is planned to be utilized. In the second chapter I will describe basic principles behind the function of the detector, following which its two quintessential parts, the single photon avalanche diode (SPAD) and the electric control circuit, will be characterized at length. The end of this chapter will be dedicated to theory behind the detector temperature stabilization.

Chapter three will focus on comparators themselves as a basic understanding of this part is needed to propose a suitable candidate for the replacement. At the beginning their general operations will be described, following which are details of the specific operation of the comparator in the single photon detector.

The fourth chapter encompasses information about the new design of the detector, which I have called SPAD TE1 v0.2. I will begin by first summarizing the previous achievements of mine and my predecessors. Afterwards will be some basic information about the new comparator and its implementation into the detector. The candidate chosen for the comparator replacement testing is the ADCMP573 comparator by Analog Devices. The fifth chapter will address the temperature stability measurements performed with the new detector as well as the results achieved.

The sixth chapter takes a brief look into the quenching speed of the single photon de-

tectors and two propositions for a speed up are made and then examined. The seventh chapter goes beyond the master thesis assignment and explores the continuously operated single photon detectors. Similarly to before, improvements in the form of a comparator replacement are proposed, these new candidates are then tested and evaluated based on the detector's dark count.

Chapter 1

Single photon counting

Single photon counting allows for detection of individual photons. Unlike in conventional photodetectors which generate signal whose strength corresponds to the photon flux, the output of single photon counter works in a purely digital mode, in other words a uniform output signal is generated once a photon is detected. This approach isn't chosen due to lack of photons reaching the detector, for example, a laser firing from earth at a detector in orbit would be able to deliver signal by many orders stronger than just a single photon. The main reason for choosing single photon detectors is their increased accuracy. While the multiphoton method is capable of reaching accuracy over hundred picoseconds, the single photon method can attain accuracy better than 20 ps. [4, 5, 6]

The propagation delay of the single photon detector is significantly affected even if more than one photon is absorbed in it during the course of a single detection event. This nature of the detector considerably restricts its applications to cases where single photons may be guaranteed. This kind of detection delay dependence on the strength of the incoming optical signal is called the detector time walk. If the detector is being employed in a multiphoton detection regime this detector time walk has to be minimised by proper compensation techniques. [5]

For multiphoton detection in the range $1 - 3000$ photons a time walk compensation may be built inside the detector package. For picosecond timing based on optical pulses with 10 to 10^4 photons another kind of compensation technique is employed, the incoming optical signal is divided into two rays and directed into two separate detectors. One of these detectors is the single photon avalanche diode (SPAD) detector used for precise timing. The other detector is an avalanche photodiode that is biased below its breakdown voltage, this diode is used for the delay correction of the timing signal. Results of using this compensation technique, can be seen in Fig. 1, which shows time resolution dependency on the incoming signal strength. Accordingly, the best attainable precision is as low as 3 ps for an incoming optical signal of 10^4 photons. [5]

Besides the 20 ps accuracy, the single photon detectors possess detection delay stability significantly better than 1 ps and they are capable of detecting radiation in the wavelength range from $0,1$ to 1800 nm. Since the remarkably high accuracy is a given feature of the single photon detectors, the detection delay stability is the key characteristic for most applications. This characteristic, with emphasis being put on the influence of detector temperature on the propagation delay, is also of great importance to this master thesis as one of the goals for this master thesis is to propose an upgrade to the current design of the single photon detector and test the propagation delay of this new detector in the temperature range of around -55 to 50 °C. [5, 1]

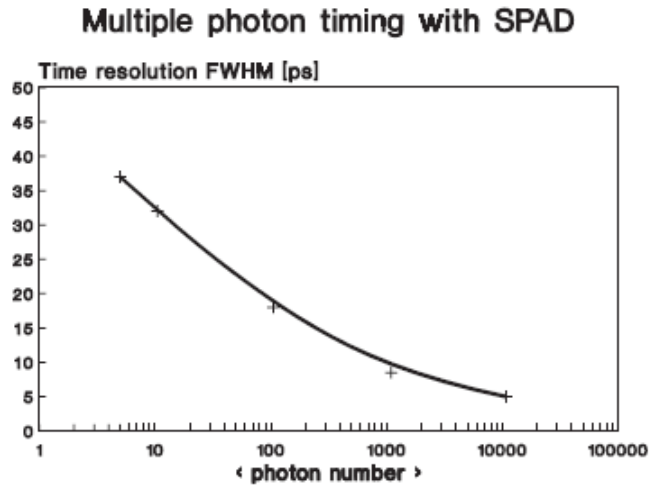


Figure 1. Multiple photon timing with SPAD, time resolution FWHM versus signal strength, dynamic range 10 to 10^4 photons/pulse [5].

1.1 Applications

It is precisely thanks to the advantageous qualities highlighted in the previous text that single photon detectors are used in many fields of science and industry, not only on earth, but also in space. Some of these applications are listed below.

Satellite Laser Ranging

This was the original application of photon counters developed at the Czech Technical University, Faculty of Nuclear Sciences and Physical Engineering (CTU FNSPE). Terrestrial targets have been ranged with 1 mm precision and precision of $3-4$ mm is feasible for satellite ranges from 400 to 20 000 km in both single and multiphoton approaches. Silicon based detector packages with thermoelectric cooling and time walk compensation were installed in more than a dozen of satellite laser stations located on five continents. [5]

Space-borne applications

The SPAD on silicon is very suitable for space deployment and has been continuously optimized for precisely this purpose. The semiconductor single photon detector was used in a photon counting laser altimeter constructed for the Soviet space project Mars '92 and the same detector was installed into the Lidar for Mars atmosphere monitoring aboard the NASA probe Mars Polar Lander 98. SPAD based detectors are suitable for the Mars surface and deep space environment due to their low operating voltage, low power consumption, high radiation resistance and no analogue signal processing. The detectors that were deployed on Mars had to be able to endure harsh temperatures ranging from -80 °C at night to over 0 °C during the day. [5]

Laser time transfer

Laser time transfer is the current prime focus of the development of the single photon detectors at CTU FNSPE. The intended objective of these detectors is to be part of the European Laser Timing (ELT) project, thus facilitate transmission of time information from atomic clock aboard the ISS. This will be further discussed in Chapter 1.2.

Other applications

Other applications include optical time domain reflectometry, fibre optics sensors, atmospheric lidar, optical sensors, quantum key distribution, cryptography, astronomy and other areas of science and industry. [5, 1]

1.2 Laser time transfer

The laser time transfer link is currently under study in the frame of the European Space Agency (ESA) mission Atomic Clock Ensemble in Space (ACES). ACES is an ESA ultra-stable clock experiment, a time and frequency mission to be flown on the Columbus module of the International Space Station (ISS), the rendition of ACES is shown in Fig. 2. The mission objectives are both scientific and technological and the mission is mainly of interest to two scientific communities. The first being the Time and Frequency (T&F) community, which aims to use ACES as a tool for high precision Time and Frequency metrology and the second being the Fundamental Physics community, which will benefit from the use of ACES data for accurate tests of general relativity. Besides these two primary applications, ACES will find purpose in many other fields. [2, 7]

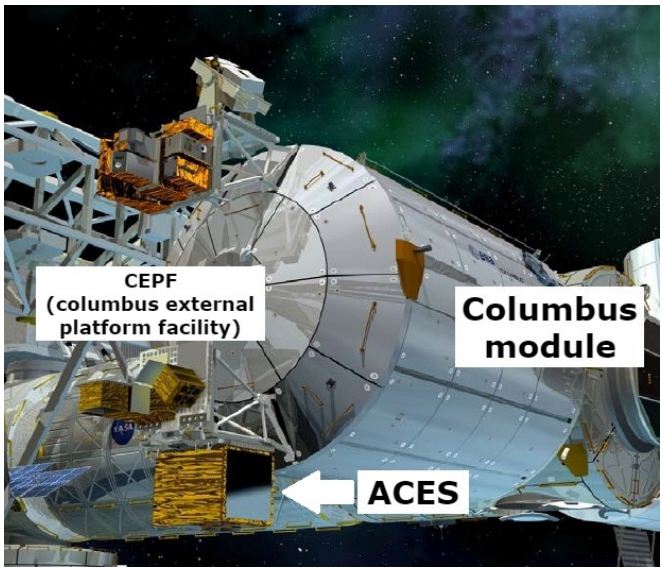


Figure 2. Rendition of the ACES payload on the Columbus module aboard the ISS [7, 8].

1.2.1 Atomic Clock Ensemble in Space

ACES is a new generation of atomic clock operating under the micro-gravity environment of the ISS. The micro-gravity environment significantly improves stability and allows for better control of systematic effects. ACES payload will distribute a stable and accurate time base that will be used for space-to-ground as well as ground-to-ground clock comparisons. At the core of this payload lies an atomic clock based on laser cooled Caesium atoms, called PHARAO. The PHARAO is a so called 'cold-atom' clock precisely because its caesium atoms are cooled to a temperature approaching the absolute zero, rendering them virtually motionless so that the 'tick-tock' oscillations of the wave they emit can be counted more accurately. Cold-atom clocks are currently the best clocks operating on Earth. The exceptional performance of the PHARAO is combined with the characteristics of a Space Hydrogen Maser (SHM). Therefore, the ACES clock signal combines the excellent short- and medium-term frequency stability of SHM with reference long term stability and accuracy of the PHARAO system based on the Caesium cold atoms. [7, 8, 9]

Stable and accurate time and frequency transfer is accomplished using a specially developed state-of-the-art microwave link (MWL). Additionally, ACES is equipped with a GPS receiver, which will supply a very precise position of the clocks, as well as an optical link - The European Laser Timing (ELT), which also ensures a high-performance exchange of time with the ground. These three mechanisms ensure flawless communication with ACES from Earth, and it is the third one, the ELT, which is of importance to this master thesis, as will be shown in Chapter 1.2.2. [8]

The next step in the ACES project will be the Space Optical Clock (SOC) which aims at operating lattice clocks on the ISS for tests of fundamental physics and for providing high-accuracy comparisons of future terrestrial optical clocks. The final goal of this project is to reach a substantial improvement compared to PHARAO, i.e. an instability and inaccuracy at the 10^{-17} level. [10]

1.2.2 European Laser Timing

Although the MWL is the main communication channel of ACES, it is 'only' capable of accuracy of several hundred picoseconds, meanwhile optical technologies might reduce this uncertainty to the level of tens of picoseconds. The comparison of time scales by means of optical frequency transfer is the most advanced technique and has been used to compare optical clocks over distances of several kilometres. This concept was already proven by T2L2 (Time Transfer by Laser) experiment, which is currently located aboard the Jason 2 satellite, and the Chinese satellite navigation project abroad the Chinese Compass-M1. The T2L2 mission was launched in 2008 and has been in operation since then, it is able to perform comparison of two clocks between remote sites with accuracy better than 140 ps. The Chinese Compass-M1 was already launched in 2007 and it has managed to achieve accuracy of 50 ps. This accomplishment is in part attributed to the Compass-M1 utilizing the single photon counting approach, unlike the T2L2, which employed the multiphoton procedure. [2, 4, 11]

The ELT project, as an indirect successor to the Chinese Compass-M1, sets out to utilize

this promising optical link technology. The ELT is developed by the Czech Space Research Center and the CTU FNSPE. The on-board equipment inside the space payload consists of a corner cube retro-reflector (CCR), a single photon avalanche diode (SPAD), and an event timer board connected to the ACES time scale. The space-ground transfer uses two-way concept. Optical pulses fired toward ACES by a laser ranging station on Earth will be detected by the SPAD diode and time tagged in the ACES time scale. Simultaneously, the CCR will re-direct part of the laser pulse toward the ground station providing precise ranging information, therefore providing information about the space-to-ground signal propagation delay. [7, 2, 6]

Among the most important parts of this setup is obviously the SPAD detector, which needs to fulfil many strict requirements in reference to its time resolution, detection delay stability and last but not least its propagation delay, moreover it needs to maintain these characteristics in environments with high radiation and temperatures ranging from -55 to 50 $^{\circ}$C. [6]

Chapter 2

Semiconductor single photon detector

Semiconductor single photon detectors are based on single photon avalanche diode (SPAD) with electric control circuit, which ensures proper function of this diode. Photon detection occurs after absorption of a photon inside the SPAD, which results in the creation of electron-hole pair. Subsequently, due to the SPAD being biased above its breakdown voltage, these charge carriers will begin to quickly multiply and force a diode breakdown. The consequence of all these events is increased electric current flowing through the diode. By detecting the edge of this rising electric current it is possible to pinpoint the time of photon absorption inside the SPAD with precision of picoseconds. An ultra-fast comparator is being employed inside the detector circuit for this purpose. This comparator, as well as its properties and capabilities, are an important point of this master thesis and they are further discussed in Chapter 3. The detector is quenched shortly after detection happens, meaning of which the voltage applied to the SPAD is lowered under its breakdown value. In this state the detector is incapable of photon detection and for further detection to occur the voltage applied to the SPAD must be once again increased above its breakdown value. All of these processes are defined and managed by the electric control circuit. This manner of operating an avalanche diode is sometimes called Geiger mode. [5, 1]

An ideal single photon detector for assumed deployment in space should primarily possess low energy requirements, satisfactory stability, resistance against radiation and minimal dependence of propagation delay on temperature and other external factors. The goal of this master thesis is an overall improvement to the current design of the semiconductor single photon detector, with special focus given to improvements in its propagation delay stability and quenching speed.

2.1 Single photon avalanche diode

Photodiode is a semiconductor device used to convert light energy into electric energy. It's comprised of a p-n junction, whose reverse current rises if there are photons being absorbed in the diode. Whenever a photon is absorbed anywhere in the diode an electron-hole pair is generated. However, these charge carriers can only be transported in certain direction when they are located in places inside the diode that contain electric field, otherwise they recombine back. Therefore, these carriers are usually generated in the depletion region of the photodiode, which leads to electric current flowing through the circuit. It is a common practice to apply increased reverse voltage on the photodiode, the result of which is higher charge carrier speed, better time response and interception of more photons. [12]

Avalanche photodiode is such photodiode, which is meant to be operated beyond the breakdown voltage, i.e., it is biased above the breakdown voltage. This kind of diode transforms absorbed photons into cascade of moving pairs of charge carriers, therefore

even a very weak optical signal is enough to generate strong electric current. Additionally, if only one photon is sufficient to initiate this kind of avalanche multiplication of charge carriers, then we call this diode a single photon avalanche diode (SPAD). [1, 12]

SPADs can be constructed from many semiconductor materials ,e.g. Si, Ge, GaAs or InGaAs. Among these, silicon SPADs have already been and still are being researched to great extent and their properties are well mapped. Moreover they are readily commercially available. For the time being they can be divided into two categories by the thickness of their depletion region, namely these categories are thin SPADs (1 μm) and thick SPADs ($5 - 150$ μm). In this master thesis I will be working with thin SPADs, that have breakdown voltage in-between 10 and 50 V, active region with radius of 5 to 200 μm and detection probability in the visible spectrum at around 45% [1]. The structure of SPAD can be seen in figure 3, where the depletion region is formed at the boundary between N+ and P region. The N region creates a ring, which increases the SPADs resistance against surface voltage breakdown. Cathode and anode are formed by gold contacts. [5]

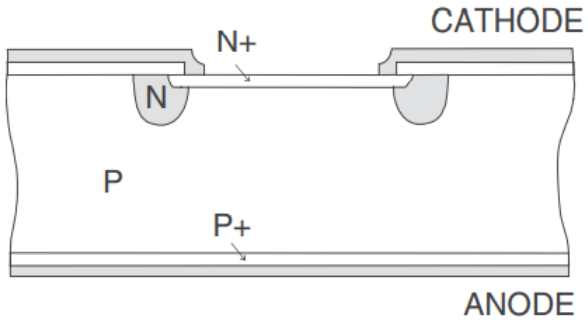


Figure 3. Cross-section of the single photon avalanche diode (SPAD) on silicon structure, where the anode and cathode are formed by metallic Au contacts [5].

The SPAD inside a single photon detector is connected in reverse direction. If the voltage applied to the SPAD is lower than breakdown voltage V_{BD}, then only minimal amount of electric current is allowed to flow through it. Even if the SPAD is biased above the breakdown voltage, its actual breakdown is not instantaneous. If at such moment a single photon is absorbed inside the depletion region of the diode, unsurprisingly an electron-hole pair is generated, however, under the effects of the strong electric field, caused by the high voltage applied to the SPAD, these two charge carries cause an avalanche multiplication, which results in accelerated breakdown of the SPAD and rapid rise of the electric current flowing through the diode. This elevated current can then be detected by the subsequent control circuit [5]. Dependence of the electric current following a diode breakdown on the voltage applied to the SPAD is shown in Fig. 4.

2.2 Electric control circuit

The electric control circuit defines the overall function and many of the characteristics of the single photon detector. The design of the electric control circuit decides the way in which the SPAD is operated. It has three main functions, which are quenching, gating and detecting the edge of the onset of electric current. The objective of quenching is to lower the voltage applied to the diode V_a under the breakdown voltage V_{BD}, and to do

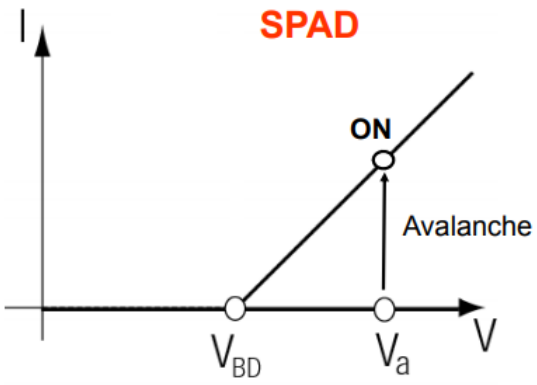


Figure 4. Graph of electric current dependence on voltage applied to the SPAD in reverse direction before and after avalanche, where V is voltage, V_a is bias voltage, V_{BD} is breakdown voltage and I is electric current [13].

that fast enough after its breakdown. Whereas gating is responsible for synchronising the active detection times with times of expected signal arrival, this is achieved by increasing the voltage applied to the diode above the breakdown voltage V_{BD} only at such times of expected signal arrival. Detecting the edge of the onset of electric current allows us to acquire the time at which the absorption of photon occurred, accuracy of such a measurement is as high as several picoseconds. Quenching and gating can be both passive or active. [1]

The principle of passive quenching lies in lowering the voltage applied to SPAD below the breakdown value V_{BD} as a result of voltage drop caused by passage through a load with high impedance. After the diode is quenched, the voltage applied to it will automatically begin to rise again, eventually passing the breakdown voltage value, making the diode once again biased above the breakdown voltage, and finally climbing to the original value from before diode breakdown. However, if a photon is absorbed inside the diode while the voltage is still increasing and hasn't yet reached the breakdown value V_{BD}, then it can't be detected. The detection can only occur after the threshold of breakdown voltage V_{BD} is crossed, after which the probability of absorbed photons successfully triggering an avalanche grows with the rising voltage being applied to the diode. Nevertheless, these following measurements will have lowered probability of successful photon detection and worse time resolution unless the voltage applied to the diode reaches the original value of bias V_a. Another option which allows us to avoid these blaring disadvantages is active quenching. The gist of active quenching lies in detecting edge of the onset of electric current using a comparator and subsequently enforcing a change in voltage applied to the SPAD by controlling its power supply. This permits us to decrease the time necessary for both the quenching itself and the ensuing elevation of the voltage applied to SPAD back to the bias value V_a. Unlike with the passive quenching, this active version allows us to define these two times with great accuracy, which is another major advantage in and of itself. Disadvantage of the active system is increased complexity of the control circuit, brought by the necessity of adding additional parts. [1]

The gating of SPADs is executed by gating signal V_g, which must be greater in amplitude than value of excess bias voltage V_e (viz. Chapter 2.3). This signal is utilized to switch the diode from closed state $V_z < V_{BD}$ to opened state $V_a = V_z + V_g = V_{BD} + V_e$, i.e. the

state in which it is biased above the breakdown voltage. Single photon detectors feature inherent down times when detection of incoming photons is impossible, hence gating allows us to synchronize the times of active detection, when the diode is in open state, with the times of expected signal arrival and maximise the detection efficiency as this kind of operation of the diode allows us to minimise effective dark count rate (will be discussed in 2.3). Passive and active versions of gating work on analogical principles to quenching. Essentially, circuits with passive gating are satisfactory in applications which require detection of only the first photon during a single gating sequence. Gating is very beneficial in many applications of the single photon detectors, but there can be some applications where it is unnecessary or even impossible to employ due to lack of the gating signal, in such cases it is possible to use continuously operated detectors (CW detectors). CW detectors utilize control circuit that can only quench and detect the edge of the onset of electric current, the gating function is omitted and instead they use RC circuit and a latch to introduce delay into the operation of the control circuit. This delay defines the fixed time between two detection events, therefore once one detection event has ended and the set delay has passed the next detection event begins immediately. [1]

Active quenching and gating circuit (AQGC) is a control circuit, which utilises ultra-fast comparator to detect the edge of the onset of electric current, brought by the avalanche multiplication of charge carriers inside the SPAD, to generate synchronized and processable output impulse, which signifies the moment of successful photon detection. Immediately after the conclusion of these events, the circuit has to lower the voltage applied to the diode, so as to prevent its potential damage and/or decrease in accuracy of subsequent measurements. Finally, after these steps are finished, the circuit needs to prepare the diode for another detection action, this is done by increasing the voltage applied to it to the bias value V_a shortly before the expected arrival of another photon. Besides precise control over the time in-between individual detections, this kind of dual active circuit allows for more clear-cut control over the bias voltage applied to the SPAD. [5, 1]

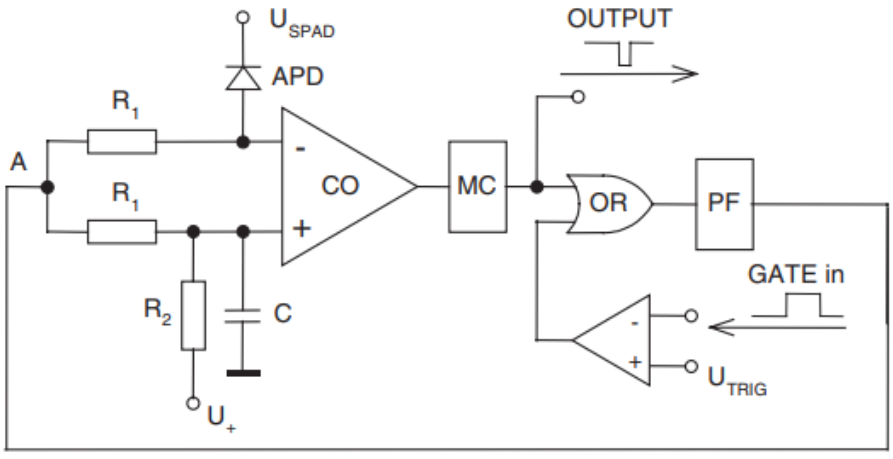


Figure 5. Block schematic of active quenching and gating circuit, the respective components are described in the accompanying text [5].

In Fig. 5 is an example of active quenching and gating circuit, this particular version is being used in a semiconductor single photon detector developed on CTU FNSPE. The photon absorption and following breakdown of the APD diode is reflected on CO comparator which shifts its output value, the principles of comparator operation are described

in detail in Chapter 3.3. The comparator output is prolonged by the monostable circuit (MC), which is a circuit that can output two discrete values and after the arrival of the start impulse it switches into the second state. The MC output is combined in the logical OR gate with the gate signal. The output of the OR drives a pulse-forming circuit (PF), which controls the APD bias. The trigger threshold can be adjusted by resistor R_2 and the APD capacitance is compensated for by capacitor C. This circuit always requires some minor alteration to match the different types of diodes in order to attain the ideal balance between optimal bias above breakdown voltage, propagation delay, energy requirements and best time resolution. [5]

2.3 Key parameters and characteristics of single photon detectors

The operation of single photon detector is characterised by several parameters, which are oftentimes interconnected and improvement in one of these parameters might lead to decrease in performance in different areas. The typical arduous challenge in building these detectors is the design optimization with the purpose to achieve the best possible performance in one of the parameters, without significantly compromising any of the other characteristics.

The properties of single photon detectors are measured in time correlated single photon counting experiments. An example of such experiment is shown in Fig. 6. A pulse generator initiates the entire experiment, sending simultaneous signals to a laser, which produces the optical signal, and active quenching and gating circuit. In this case the laser used to generate the optical signal is HAMAMATSU PLP01, which radiates at wavelength of 757 nm with power of 5 mW. The AQGC activates at the same time or with a slight delay to prepare the SPAD in time for receival of the incoming optical signal. Once the optical signal arrives to the SPAD, it breaks down, which results in the appropriate response in the AQGC. The AQGC then processes these changes and sends an output signal, meaning that a diode breakdown has been detected. This output signal from the AQGC, along with the initial impulse that started the laser action, is directed into a time to amplitude converter. This device evaluates the time difference between the arrival of these two signals and sends the final time information through a multichannel analyser into a computer. [5]

Excess bias voltage

One of the detector's main characteristics is the excess bias voltage V_e, which is defined as $V_e = V_a - V_{BD}$, where V_a is the value of bias applied to the SPAD and V_{BD} is the value of the SPADs breakdown voltage. The excess bias voltage decides the electric current which will flow through the diode after its breakdown, as can be seen in Fig. 4. The typical V_e values in available SPADs are in range of $1 - 50$ V. [1]

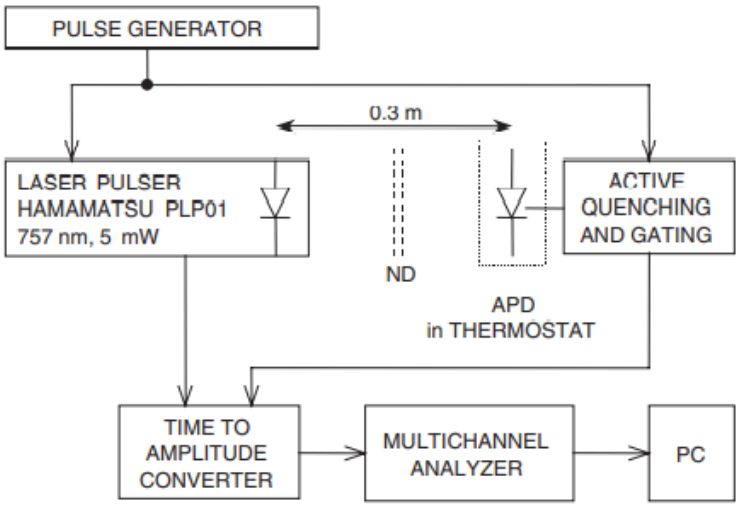


Figure 6. Schematic of a time correlated single photon counting experiment, the respective components are described in the accompanying text [5].

Gate signal frequency and length

In certain applications, it is necessary or at least advantageous to operate the detector under the control of gate command V_g, the particularities of gating have been explained in Chapter 2.2. As has been explained, the gate signal needs to be stronger than excess bias voltage V_e, nonetheless it also needs to feature very fast rise and fall times. Its other properties such as frequency and length depend mainly on applications, as they define the overall performance of the detector. For example, higher gating frequency allows for quicker data gathering, but results in greater effective dark count rate (will be explained in the following text). [1]

Single photon detectors can also be operated in continuous mode, in this mode the SPAD is continuously biased above the breakdown voltage following a certain delay after each breakdown.

Photon detection probability

Photon detection probability is influenced by two factors, which are photon absorption probability and probability of initiating an avalanche of charge carriers. The final photon detection probability is obtained by multiplying these two auxiliary probabilities. [1]

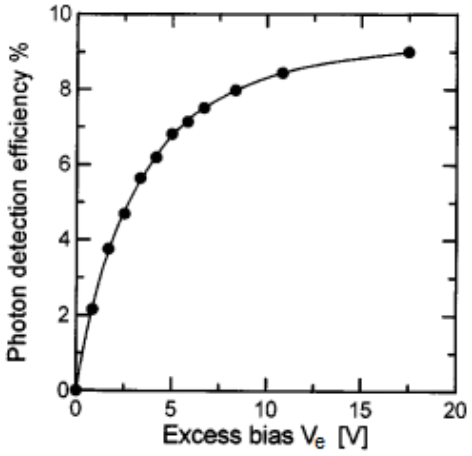
The photon absorption probability describes the probability that photon will be absorbed inside the depletion layer of the SPAD which would subsequently result in generation of electron-hole pair of charge carriers. This probability cannot be directly influenced as it is given by the structure of the single photon detector. [1]

The probability of initiating an avalanche of charge carriers specifies the probability that once these two charge carriers are generated, they will be able to launch an avalanche multiplication of themself. This probability, until a certain point of saturation, grows along with the value of excess bias voltage V_e, as this value defines the intensity of the electric

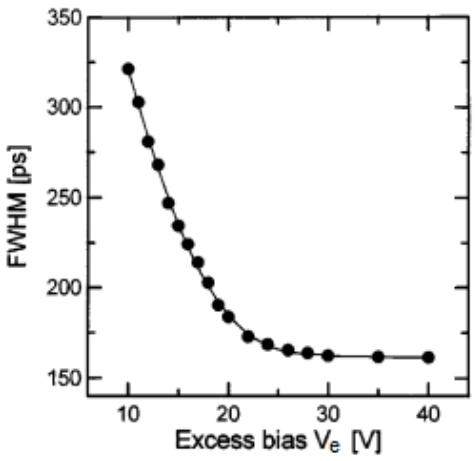
field inside the depletion region and by extension the probability of successfully initiating the avalanche reaction. The influence of the excess bias voltage V_e on the final photon detection probability can be seen in Fig. 7a. [1]

Time resolution

Time resolution is typically represented by full width of the signal at half of its maximum (FWHM - full width half maximum). The statistical fluctuation of the time interval in-between the photon arriving to the detector and the output signal being generated is defined as the time resolution or also time jitter [14]. The time resolution can also be improved by increasing the excess bias voltage V_e, as is shown in Fig. 7b. [1]



(a) An example of the dependency of photon detection probability on the excess bias voltage V_e applied to the SPAD [1].



(b) An example of the dependency of time resolution FWHM on the excess bias voltage V_e applied to the SPAD [1].

Figure 7. Graphs showing the impact that the excess bias voltage V_e applied to SPAD has on the detector's characteristics.

Time deviation

Time deviation or TDEV in short is a measure of time stability based on the modified Allan variance. It is particularly useful for measuring the stability of a time distribution network. The measurement of time deviation over certain time (usually several hours) is used to measure the stability of a detector. For finite number of measurements N it can be approximated as

$$\mathrm{TDEV}(n\tau_0) \cong \sqrt{\frac{1}{6n^2(N-3n+1)} \sum_{j=1}^{N-3n+1} \left[\sum_{i=j}^{n+j-1} (x_{i+2n} - 2x_{i+n} + x_i) \right]^2} \tag{1}$$

where x are the individual measurements, τ_0 is period defined by the repetition rate of the measurement and n is selected freely from $n \in \mathbb{N}$, $n < N/3$. [15, 16]

Propagation delay stability

Propagation delay stability describes changes in the propagation delay brought about by external conditions of the detector, such as temperature, radiation, power supply instability, etc. This particular characteristic of the detector plays a major role in this master thesis, with emphasis being put on the influence of detector temperature on the propagation delay. One of the goals of this thesis is to propose an upgrade to the current design of the single photon detector in this regard and then test the propagation delay of this new detector in the temperature range of around -55 to 50 °C. Appropriate propagation delay temperature stability in this temperature range, the proposed target is less than $|0,25|$ ps/K, is crucial for the intended application of this detector in space.

Effective dark count rate

Effective dark count rate represents detection noise, which manifests itself when the SPAD breaks down, and thus the detector is triggered, without absorbing any photons. The specific value of effective dark count rate is defined as the inverse value of the mean time during which the SPAD can be biased above the breakdown limit before the breakdown occurs by itself. Effective dark count rate is divided into primary and secondary impulses. [1, 5]

One of the sources of the primary dark pulses are thermally generated carriers, whose significance rises with the temperature. Another cause of the primary dark pulses is high excess bias voltage V_e, as that enhances emission rate from the generation centres and increases the probability of triggering an avalanche. [1, 5]

Secondary dark pulses are caused by an event called the afterpulsing, which strongly influences the final effective dark count rate. This afterpulsing begins during an avalanche when some of the charge carriers are captured by deep levels in the junction depletion region. Afterwards, they are released with a statistically fluctuating delay. These released carriers may trigger another avalanche reaction, causing the generation of afterpulses that have in fact stemmed from the previous avalanche pulse. The secondary dark pulses increase with delay in the SPAD quenching, excess bias voltage V_e and higher gating frequencies. Since excess bias voltage V_e and gating frequency are important parameters that are usually defined by the application of the single photon detector, the most appropriate way to reduce afterpulsing is to strive for maximum quenching speed. One of the goals of this thesis is to propose an upgrade to the current design of the single photon detector in this regard and then test the quenching speed of this new detector. [1, 5]

Temperature

The value of breakdown voltage V_{BD} of the SPAD depends on its temperature. If we were to use constant bias voltage V_a, then the changes brought by the differing breakdown voltage V_{BD} would affect the value of excess bias voltage $V_e = V_a - V_{BD}$, which, as was said in previous paragraphs, is closely tied to many of the major detector characteristics. However, even the avalanche multiplication of charge carriers itself causes non-negligible

heating of the SPAD, let alone the external conditions that might influence the whole detector package, as such the instability in breakdown voltage V_{BD} is an unavoidable factor. For these reasons it is absolutely necessary to employ certain methods to stabilize the SPAD temperature, such as with cooling, or compensate its fluctuation with flexible bias voltage V_a, so as to avoid deterioration in measurements quality. These methods are further discussed in Chapter 2.4. [1]

2.4 Temperature compensation

As was explained in Chapter 2.3 temperature strongly influences the overall detecting abilities of the single photon detectors. Specifically, temperature induced change in breakdown voltage V_{BD} results in variable excess bias voltage V_e. To avoid diminishing in detection quality, brought about by these variables, it is necessary to utilize certain compensation techniques. The two main techniques are SPAD cooling and SPAD bias control.

SPAD cooling

The SPADs utilized at CTU FNSPE, called SPAD TE1, can be thermoelectrically cooled. Besides the temperature compensation, this kind of modification allows for reduction in the effective dark count rate. Every 30 K drop in SPAD temperature results in improvement of the effective dark count rate by order of magnitude. [17]

Although the cooling is overly advantageous it brings its own complications, namely, afterpulsing. The decrease in temperature leads to reduced speed of charge carriers, which means that it takes longer time to eliminate them from the medium, hence elevating the chance of triggering an unwanted avalanche produced by the afterpulses. This effect is negligible for low gating frequencies, but results in much worse performance for higher frequencies, even worse than an uncooled SPAD would have produced. This problem can be overcome by a slight modification of the control circuit. Whereas previously the circuit could only be quenched by comparator output switching, the new circuit can quench itself even by the trailing edge of the gating pulse. The circuit is quenched by whichever pulse occurs first. This design allows for successful quenching every time the circuit is primed, even if there is no subsequent photon absorption. [17]

SPAD bias control

This technique uses voltage regulators to passively control the bias voltage V_a applied to SPAD. Voltage regulators maintain a constant amount of voltage on a load, even during fluctuations of the power source or if the amount of current drawn by the load changes. [18]

Inside the single photon detector circuit, a voltage regulator LM723 is used to stabilize the voltage applied to the diode, marked as U_{SPAD}, in other words it stabilises the bias voltage V_a. This voltage stabiliser can operate in temperature ranges of -55 to $+150$ °C. The schematic and detailed properties of this component can be found in [19]. The important

characteristic is that this component can feature its own temperature drift proportional to mV/K. This temperature drift can be used to compensate for the temperature drift of the SPAD breakdown voltage V_{BD}, therefore ensuring constant excess bias voltage V_e. The breakdown voltage of SPAD increases by roughly 30 mV/K, hence this amount should be the optimal temperature drift for the LM723, which can be adjusted by proper resistor connection.

The detailed connection of the voltage stabilization/regulation with the LM723 can be seen in Fig. 8. The voltage stabilizer is connected behind the +35 V supply and it outputs voltage which is then applied to the SPAD, denoted in the figure as U_{SPAD}. The adjustable resistor R_P is used for finetuning the specific value of bias voltage V_a that is to be applied to the SPAD. The stabilizer is also connected to temperature sensor AD590KH, which produces voltage according to the formula: 1 mV = 1 K, this allows the stabilizer to react to the temperature of the detector package. The temperature drift of the stabilizer can be altered with the R resistor, the exact profile of this dependency will be measured in Chapter 5.1.

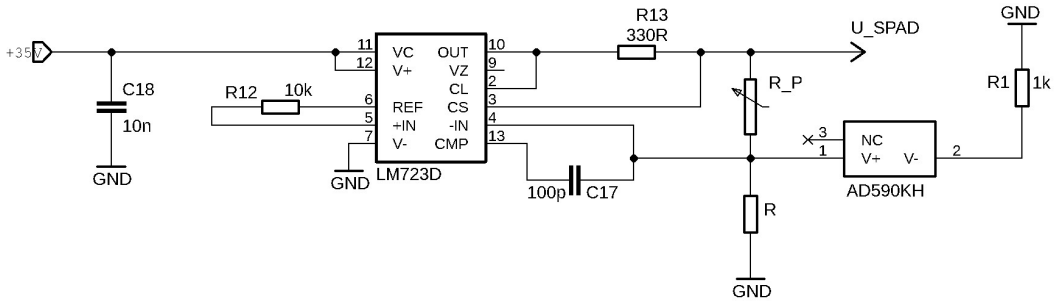


Figure 8. Schematic showing the detailed connection of LM723 inside the single photon detector.

It may seem that matching the temperature drift of the stabilizer equal to drift of the SPAD, and therefore keeping the excess bias voltage constant is the best approach, but that may not be the case, as was proven by Tereza Fleková in her bachelor thesis [20]. The theory presented in that thesis is based on the fact that excess bias voltage inversely affects the propagation delay, therefore by using higher excess bias voltage, which would be the result of higher temperatures, we could lower the propagation delay. This could potentially, and as was proven, it indeed does compensate the detector's propagation delay dependency on temperature, which is in the hundreds of fs/K. [20]

Experimental results measuring single photon detector's relative propagation delay dependency on temperature using SPAD bias control to compensate for temperature change are shown in Fig. 9, where U_{AB} marks excess bias voltage. From this graph it can be seen that the ideal temperature drift of the voltage stabilizer is around 36 mV/K, instead of the 30 mV/K which would match SPAD drift. Notable peculiarity of this graph is the switch in drift value sign at around the room temperature. This occurrence has evident impact on our application of temperature compensation, since as can be seen from the graph, changing the stabilizer drift results in overall tilting of the propagation delay curve, and there is no way to compensate this 'v' shape just by curve tilting. This anomaly is attributed to the comparator used in the circuit for that particular detector (comparator ADCMP553 [21]). Following these results, it was concluded that this comparator is not completely

ideal for further use in the detector and might be replaced. [20]

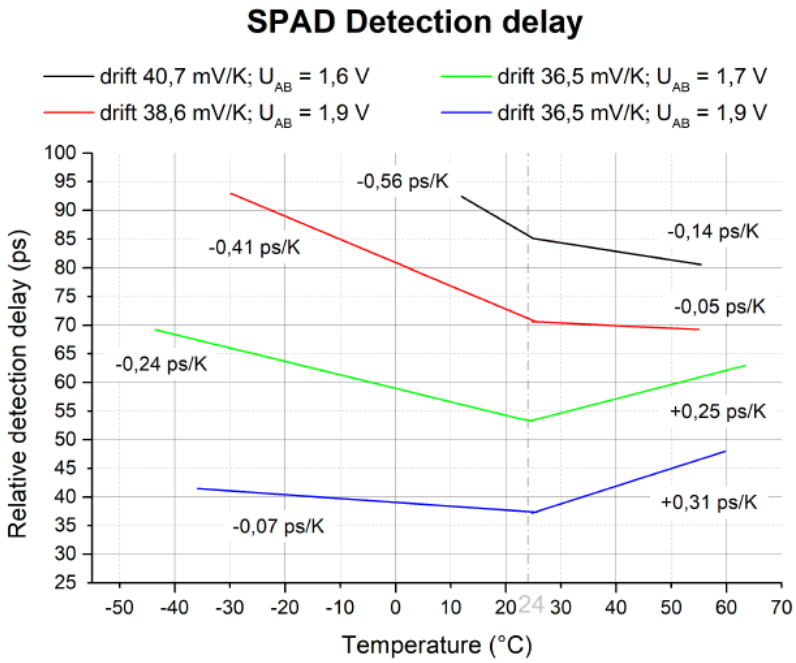


Figure 9. Experimental results measuring single photon detector's relative propagation delay dependency on temperature using voltage stabilization to compensate for temperature change, where U_{AB} marks excess bias voltage [17].

Chapter 3

Comparator

Comparator is an integrated circuit that compares the voltage applied to its two inputs (inverting - and noninverting +) and switches its output in-between HIGH and LOW setting in response to which of its inputs is being affected by higher voltage. The voltage connected to one of its inputs is often constant and is referred to as reference voltage, the operation of such a comparator is depicted in detail in Fig. 10. The comparator output only has these two available voltage values (HIGH and LOW), which is the reason why the comparator can function as analogue-to-digital convertor. However, this concept of binary output is rather idealistic as there exists a transition region in-between these two output values, this region and the involved transition times are non-negligible in ultra-fast applications. Comparator operation requires its own power supply. [22, 23]

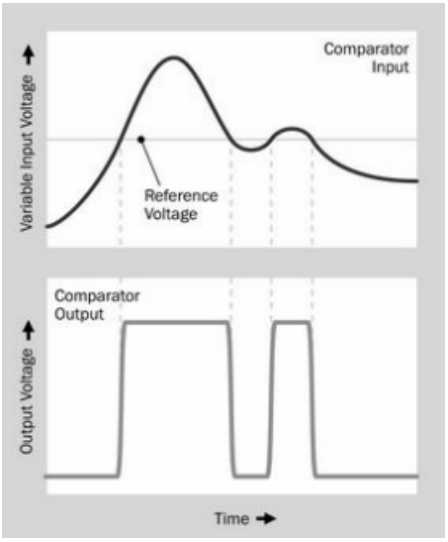


Figure 10. Graph describing the performance of comparator output in relation to the voltage being applied to its inputs [22].

3.1 Select comparator variants

Hysteresis can be introduced in a comparator through an independent pin on the chip package. The hysteresis zone, equal to voltage value of V_H, can be envisioned extending above and below the reference voltage level, so that any small input fluctuations that fall within this zone are ignored. The comparator only reacts when the input asymmetry exceeds the set hysteresis zone. If the input voltage approaches the threshold (0.0 V in this example) from the negative direction, the comparator switches from low to high only when the input crosses + $V_H/2$. The switching threshold then changes to a new value of -$V_H/2$. In this manner, input noise centred on 0.0 V does not cause the comparator to wildly switch states unless it exceeds the hysteresis region. [22, 24]

Some comparators may feature internal latch, which likewise corresponds to a separate

pin. Enabling the latch forces the comparator to lock its current output value and no amount of change on the inputs will be able to shift the output while the latch is still enabled. This can be used to allow other components in a subsequent circuit to properly read the comparator output. Using a comparator with latch is a necessary requirement for continuously operated single photon detectors. [22]

Significant for the single photon detectors are ultra-fast comparators that are designed to minimise their propagation delay, or in other words to cross the transition region between the two output states as fast as possible. The ultra-fast comparators allow for the closest portrayal of the perfect binary output. The ultra-fast comparators are in fact a combination of two other comparator variants, the open-loop comparator and the regenerative comparator. The open-loop comparators are essentially operational amplifiers without compensation, while the regenerative comparators utilize positive feedback. [23]

3.2 Key parameters and characteristics of comparators

Input resolution

Input resolution describes the minimal input asymmetry ΔV necessary to switch the output voltage value in-between its two states. The ideal input resolution should approach zero. [23]

Input offset voltage

Input offset voltage, denoted as V_{IO} or V_{OS}, is variable small amount of voltage by which it is necessary to cross the reference voltage to truly force an output swing. It factors a kind of inaccuracy in the process of evaluation of the input voltage asymmetry. An ideal comparator should have negligible input offset voltage. The effect of input offset voltage is depicted in Fig. 11. [22]

HIGH and LOW output values

HIGH and LOW output values are respectively denoted as V_{OH}, resp. V_{OL}. These parameters specify which two voltage values can be held by the comparator output. Whichever of these two values is currently held on the comparator output is entirely dependent on the state of the comparator inputs. [23]

Voltage gain

Voltage gain A_{VD} is defined as maximal ratio of output voltage to input voltage. It can be therefore mathematically expressed as

$$A_{VD} = \frac{V_{OH} - V_{OL}}{\Delta V} \tag{2}$$

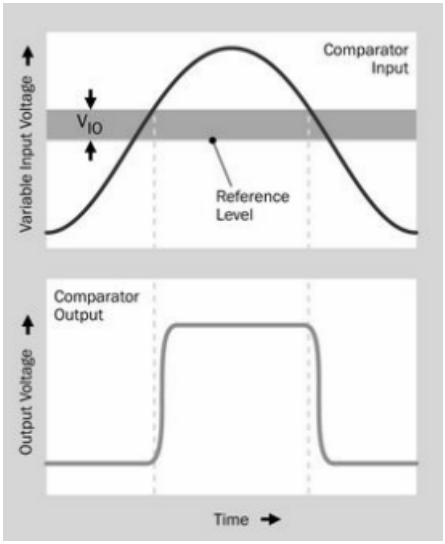


Figure 11. Graph which shows the effect of input offset voltage V_{IO} on a comparator [22].

where V_{OH}, resp. V_{OL} describe HIGH, resp. LOW output value and ΔV references to the input resolution. Typical voltage gain values range from 40 to 200. [22, 23]

Propagation delay

Propagation delay t_P is measured from the moment when the inputs cross the threshold needed to switch the output until the moment when output reaches 50% of its final value. Propagation delay value may differ for entering LOW and HIGH output state. Propagation delay is an important characteristic for the purposes of this master thesis and Chapter 5.2 describes the measurement of propagation delay, and its stability, of the complete single photon detector package which will include new comparator ADCMP573. [22]

Propagation delay dispersion

Propagation delay dispersion specifies maximal change in the propagation delay brought about by either change in overdrive or slew rate. Overdrive describes amount of voltage by which the switching threshold was exceeded, while slew rate describes how fast the switching threshold was crossed. This value is especially significant in ultra-fast comparators. [24]

Input common mode range

Input common mode range defines the range of voltage which can be applied to the comparator inputs for it to still function properly. [23]

3.3 Comparator operation in the semiconductor single photon detector

The comparator plays vital role inside the control circuit of the single photon detector, as can be seen in Fig. 5. The comparator is used to detect the edge of the onset of electric current, which comes about as a result of the avalanche multiplication of charge carriers and the subsequent breakdown of the SPAD. Its digital output is then directed into a computer as well as further on into rest of the control circuit to initiate quenching and gating sequences, these mechanisms were previously described in Chapter 2.2.

The specific comparator circuit connection is shown in Fig. 12, in accordance with the figure the reference voltage is applied to inverting input (-) and the anode of the SPAD is connected to the noninverting input (+). If the SPAD breakdown hasn't occurred yet, only very limited amount of electric current flows through the diode and higher voltage is by default applied to the inverting input (-), which means that the comparator is outputting LOW voltage value. After photon absorption causes breakdown of the SPAD, increased current will start flowing through it, which results in the voltage being applied to the noninverting output (+) exceeding the reference voltage and finally the output switching to the HIGH voltage value. This moment of switching to the HIGH value marks the time of photon detection. Comparator appropriate for this purpose needs to be able to react to impulses with relatively low amplitude, i.e. it requires low input offset voltage. Additionally, it needs to keep the total charge flowing across the structure after the SPAD breakdown minimal, which means quenching the circuit as fast as possible. This helps counter afterpulsing, the effects of which were described in Chapter 2.3. However, these two requirements run contrary to each other, which makes finding suitable comparators truly difficult. [1, 5]

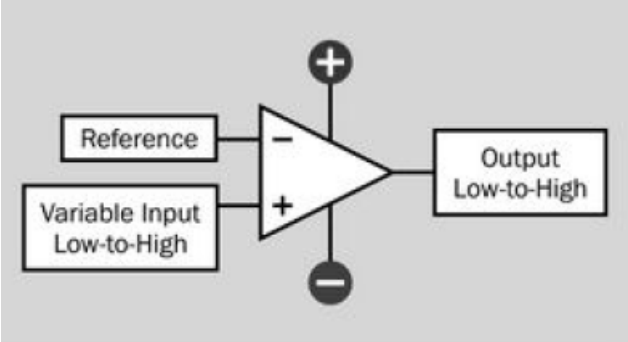


Figure 12. Schematic describing comparator circuit connection in the semiconductor single photon detector, where the variable input is connected to anode of the SPAD. [22]

Chapter 4

SPAD TE1 v0.2

SPAD TE1 single photon detector is a detector package currently in development at the CTU FNSPE for expected deployment in ESA mission ACES, where it will function as vital part of the laser time transfer. The ACES mission was discussed in detail in Chapter 1.2.1

4.1 Previous versions and achievements

The latest approved design of the single photon detector utilizes a 100 μm active area diameter SPAD called TE1 connected to an electric control circuit, which generally resembles the one depicted in Fig. 5. At the core of this particular control circuit lies comparator ADCMP553. This specific comparator is largely suitable for use in this detector as it perfectly fits many of the criteria imposed by expected application in space. The notable ones among these are high input impedance (>1kΩ), short propagation delay (500 ps), proper input common mode range (-2,0 to 3,0 V), sufficient signal switching speed and most important is its certification for deployment in space. Its only significant problem arises if we take a look at its temperature propagation delay stability, this specific parameter is also important for the space application of the detector. According to the data supplied by the manufacturer, Analog Devices, this comparator has perfectly linear propagation delay dependency on temperature with growth coefficient of $0,25$ ps/$^{\circ}$C, viz. Fig. 13. However, in reality this comparator doesn't possess such qualities. As per the measurements conducted in the laboratories of CTU FNSPE, the true qualities of the ADCMP553 comparator should be those shown in Fig. 14. By comparing these two graphs it can be seen that the data published by the manufacturer are roughly valid only for temperatures surpassing 23 $^{\circ}$C, where the measured dependency is linear with growth coefficient of $(0,20 \pm 0,03)$ ps/$^{\circ}$C. On the other hand, for lower temperatures the dependency changes sign altogether and becomes descending with coefficient of $(-0,20 \pm 0,06)$ ps/$^{\circ}$C. It is precisely this change of sign for the dependency coefficient that is so problematic for our application of the comparator. If the propagation delay dependency of the comparator was linear, then no matter its coefficient, we would have been able to compensate it, as was discussed in Chapter 2.4. There we have also arrived at a conclusion, that there is no way for the current detector to compensate for such non-linear dependency in shape of 'v' and as such the comparator ADCMP553 was ultimately deemed imperfect for usage in the single photon detector. [21, 17, 20]

The way to resolve this issue is seemingly simple, as it is to replace the current comparator ADCMP335 with a more suitable one. However, as simple as it sounds, it is necessary to find a comparator which fulfils all of our other requirements, some of which were mentioned in previous paragraph, while also possessing improved propagation delay dependency on temperature. Such comparators are hardly in abundance and even if we do find a viable candidate it obviously insufficient to blindly trust the data published by the manufacturer as was proven by my predecessors. The manufacturer is unable of

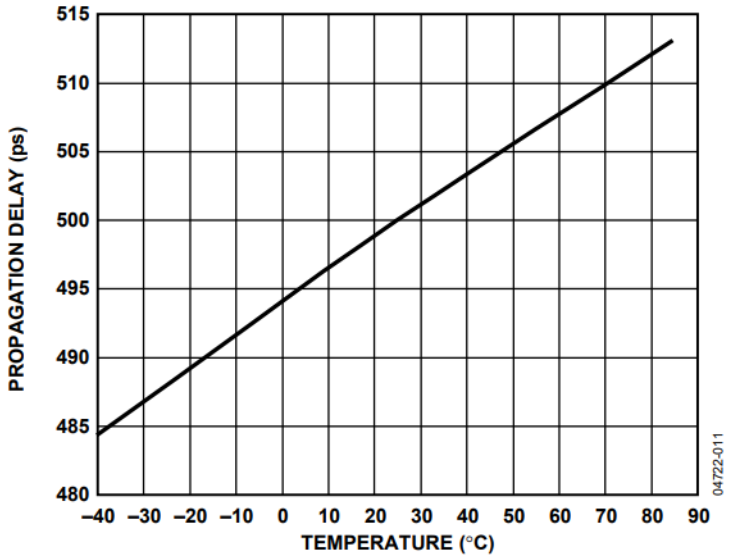


Figure 13. Graph showing propagation delay dependency on temperature for the ADCMP553 comparator, taken from the data sheet published by the manufacturer [21].

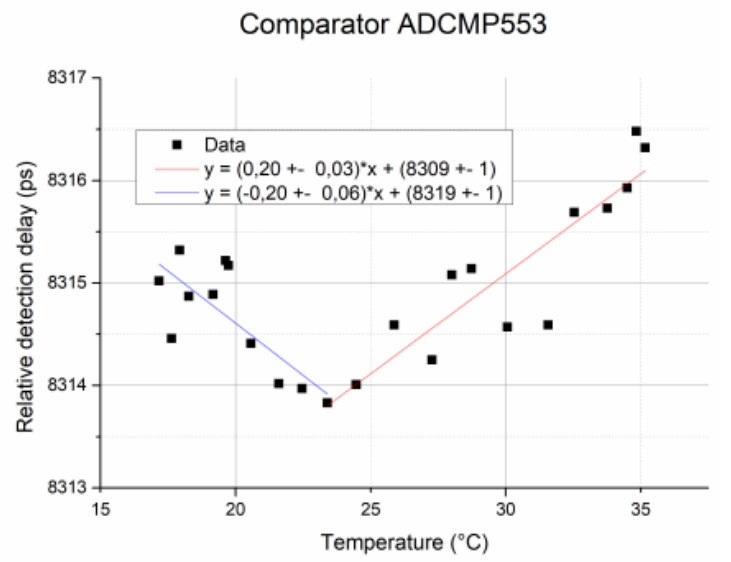


Figure 14. Graph showing propagation delay dependency on temperature for the ADCMP553 comparator as it was measured in laboratories of CTU FNSPE, taken from [17].

conducting measurements with precision matching the one possible in our laboratory. Ultimately each identified candidate needs to be tested and only afterwards can its suitability be determined.

In my previous work I have identified and tested one such candidate, namely the comparator ADCMP565, the detector package featuring this comparator was marked SPAD TE1 v0.1. ADCMP565 fulfilled all of our necessary requirements while promising better propagation delay dependency on temperature. However, in addition to these characteristics it also had some unnecessary or borderline unwanted features, such as second channel or -5,0 V power supply requirement. The second channel was completely redundant and -5,0 V supply had to be added to the package just for the comparator. Nonetheless just these

drawbacks are not enough to disqualify the comparator. I have measured the comparator's propagation delay temperature dependency, the results of this measurement are shown in Fig. 15. The dependency shown in this graph is once again different from the one shown in the datasheet published by the manufacturer, though this time the difference isn't so drastic. The overall growth coefficient is slightly higher than expected, but the bigger issue is that the dependency is still not perfectly linear. Nevertheless, the dependency of the ADCMP565 comparator doesn't feature any sharp turns or sign changes and in this regard the comparator is much better than the ADCMP553. However, because the dependency is not perfectly linear, coupled with some of the unwanted attributes of this comparator and the fact that comparator ADCMP565 doesn't yet have space deployment certification, it was ultimately deemed that the comparator isn't sufficiently superior to its predecessor to warrant its replacement and the full detector package incorporating it was never built. [25, 26].

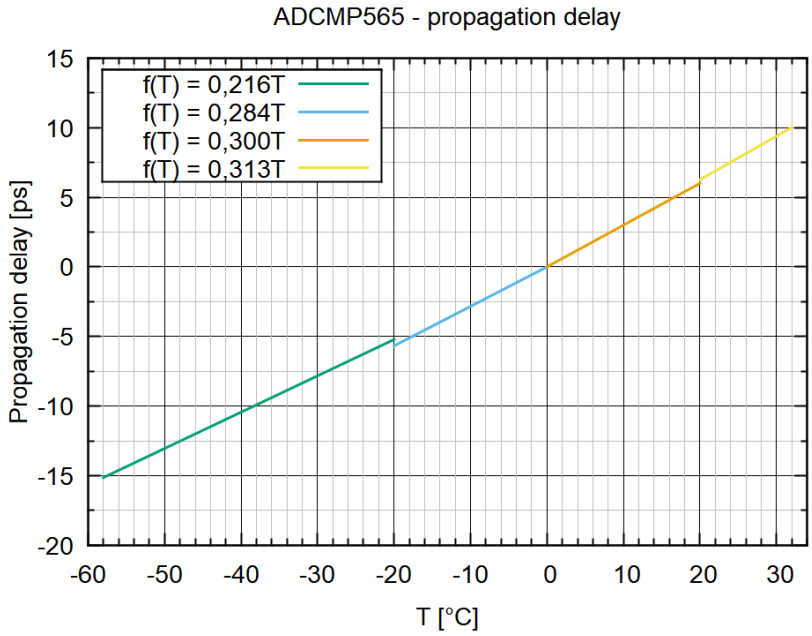


Figure 15. Graph showing propagation delay dependency on temperature for the ADCMP56 comparator, taken from [26]

The goal of this master thesis is to identify and verify a new candidate for the comparator used in the SPAD TE1 single photon detector. The candidate that will be discussed in the following text is ADCMP573, which fulfils all of our necessary requirements, has no redundant features and some of its characteristics are even adjustable, so we can choose the settings that best fit our needs. Its propagation delay dependency on temperature seems promising, however this aspect will have to be remeasured in our laboratory.

4.2 Basic information about ADCMP573

The comparator block diagram is in Fig. 16. ADCMP573 is an ultrafast comparator made by Analog Devices. It offers 150 ps propagation delay and 80 ps minimal pulse width for 10 Gbps operation with 200 fs rms random jitter. Propagation delay dispersion is typi-

cally less than 15 ps. The device possesses adjustable input common mode range of either -0,2 V to +1,2 V or -0,2 V to +3,2 V based off of its power supply connections. Input impedance can also be adjusted in-between high and low settings thanks a 50 Ω on-chip termination resistors that can be left open. The complementary outputs are designed to drive 400 mV into 50 Ω terminated to V_{CCO} and they are compatible with PECL families. The HIGH and LOW output levels are dependent on power supply connections. The comparator inputs offer robust protection against large input overdrive, and the outputs do not phase reverse when the valid input signal range is exceeded. High speed latch and programmable hysteresis features are also provided. The possible supply voltage connections are either V_{CCI} = V_{CCO} = 3,3 V or V_{CCI} = 5,2 V and V_{CCO} = 3,3 V. The comparator comes in two similar versions, the aforementioned ADCMP573 and the ADCMP572. The 572 features CML output drivers, while 573 offers reduced swing PECL output drivers that are also featured in ADCMP553, which is the reason why it was chosen, as it will require fewer modifications to the control circuit. The two versions should be identical in performance. The comparator is available in a 16-lead LFCSP package. [24]

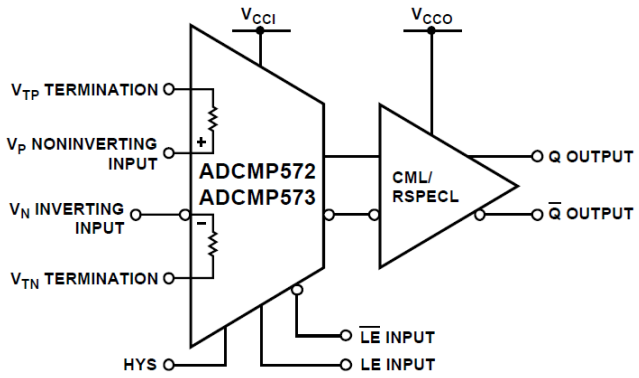


Figure 16. ADCMP572/ADCMP573 comparator block diagram, taken from [24].

As an ultrafast SiGe device, for it to function properly and achieve the specified performance, the ADCMP573 comparator needs to be paired with appropriate high speed design techniques. The most critical one is the use of low impedance supply planes, particularly the output supply plane (V_{CCO}) and ground plane. Individual supply planes are suggested as part of a multilayer board. It is also of great importance to adequately bypass the input and output supplies. A 1 μF electrolytic bypass capacitor should be placed within several inches of each power supply pin to ground. In addition, several high quality 10 nF bypass capacitors should be placed as close as possible to each of the V_{CCI} and V_{CCO} pins and should be connected to GND with redundant vias. High frequency bypass capacitors should be carefully selected. In case that the input and output supplies are connected separately, therefore $V_{CCI} \neq V_{CCO}$, care should be taken to bypass each of them separately to the GND plane. It is recommended that the GND plane separate the V_{CCI} and V_{CCO} planes to minimize coupling between the two supplies. This improves the performance when split input/output supplies are used. [24]

The comparator features an internal latch which is connected to a set of two pins (LE/$\overline{\text{LE}}$). The latch inputs are active low for latch mode and are internally terminated with 50 Ω resistors to Pin 8, which corresponds to and is internally connected to the V_{CCO} supply. The latch function can be disabled by externally connecting V_{TT} pin to the PECL termination supply $V_{CCO} - 2$, connecting the LE pin to V_{CCO} with an external 500 Ω resistor and lea-

ving the $\overline{\text{LE}}$ pin disconnected. In this case, the resistor value does not depend on the V_{CCO} supply voltage setting. This comparator also features a hysteresis option, which is often desirable in an environment with high noise levels or when the differential input amplitudes are too small or slow changing. The ADCMP573 comparator offers a programmable hysteresis. By connecting an external pull-down resistor from the HYS pin to GND, a variable amount of hysteresis can be applied. Leaving the HYS pin disconnected disables the feature, and hysteresis is then less than V_H = 1 mV. [24]

The comparator provides an internal 50 Ω termination resistors for both positive and negative input. The return side for each input termination is pinned out separately. If a 50 Ω input impedance is desired on either of the inputs, the respective termination pin should be connected to GND, in case that 50 kΩ input impedance is desired then the termination should be left open. When leaving the input terminations disconnected, the internal resistor acts as a small stub on the input transmission path and can cause problems for very high speed inputs. It is recommended, that the drive source impedance is no more than 50 Ω for best high speed performance. [24]

The comparator is designed to reduce propagation delay dispersion. The dispersion is typically < 15 ps for overdrive between 10 and 500 mV and the input slew rate ranges from 2 V/ns to 10 V/ns. This characteristic applies for both positive and negative signals. As with similar devices, a requirement of minimal slew rate must be met so that the output doesn't oscillate when the input crosses the threshold. The minimum value for the ADCMP573 comparator is 50 V/μs. [24]

Propagation delay of the ADCMP573 is 150 ps, which is considerably better than the previous versions, where the ADCMP553 had delay of 500 ps and the ADCMP565 had delay of 300 ps. In graph Fig. 17 is, the most important piece of data for the purpose of this master thesis, the propagation delay dependency on temperature for the ADCMP573 comparator, taken from the data sheet published by the manufacturer [24]. The dependency is obviously not perfectly linear, but it rises with coefficient of roughly 100 fs/K. On the other hand, this imperfection gives it more credibility, as the critical point is around the 20 °C mark, which we have previously confirmed to be problematic spot. Even though the dependency is non-linear, there are no drastic shift or even sign changes and therefore the comparator could be suitable for our application. However as was mentioned in the previous text, such conjectures need to be confirmed with measurements at our laboratory. [24]

4.3 ADCMP573 implementation

Scheme of the SPAD TE 1 single photon detector containing the ADCMP573 comparator is in Fig. 39, 40. The comparator itself is located in areas designated as 6-7/E and its name is IC2. The original schema and printed circuit board (PCB) design are the ones used in my bachelor thesis [26] and they were previously taken from the master thesis of Tereza Fleková [17]. The comparator ADCMP573 ECAD model was taken from Component Search Engine site [27]. I have completed the replacement and implementation of the comparator in the program EAGLE [28]. The comparator is connected as per the specifications defined in the data sheet supplied by the manufacturer [24], which were

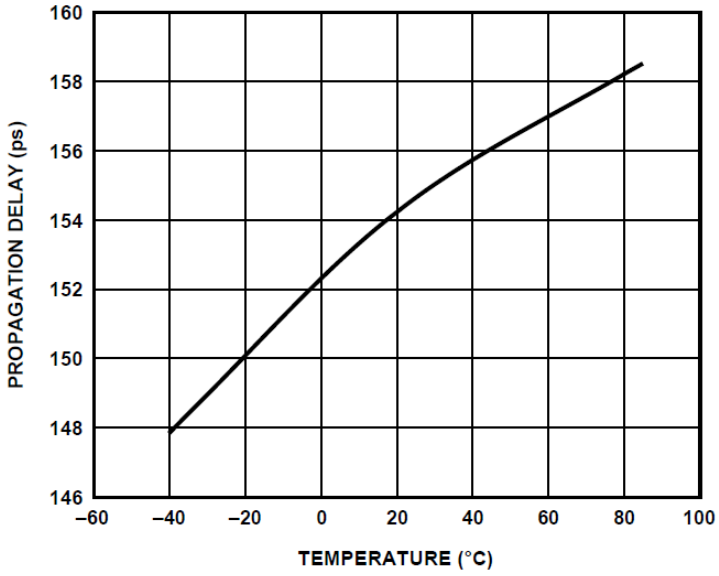


Figure 17. Graph showing propagation delay dependency on temperature for the ADCMP573 comparator, taken from the data sheet published by the manufacturer [24].

discussed in the previous Chapter 4.2.

The anode of the SPAD is connected to the noninverting input (VP) and the reference voltage value is connected to the inverting input (VN), both input terminations (VTP and VTN) are left open to set input resistance to the high value of 50 kΩ, which more than enough satisfies our requirement of at least 1 kΩ. Input supply ($V_{CCI}1/2$) is connected to +5,0 V and the output supply ($V_{CCO}1/2$) is connected to +3,3 V to ensure wide enough input common range of -0,2 to +3,2 V. All supplies are adequately bypassed according to the description cited in Chapter 4.2. Both ground pins (GND1/2) are connected to supply ground. The EPAD remains unconnected, nonetheless it is soldered to the PCB to facilitate better thermal and mechanical stability. The hysteresis pin (HYS) is left open for minimum hysteresis zone. Latch enable pin (LE) is connected to +3,3 V supply through a 500 Ω resistor, its complementary pin ($\overline{\text{LE}}$) is left disconnected and the latch termination (V_{TT}) is connected to +1,3 V, which is created from the +3,3 V supply, this is done to disable the latch feature, as it is unwanted in our application. The outputs are terminated to ground with 120 Ω resistors, this particular connection is used to ensure the smallest possible deviation from how the original SPAD TE1 with ADCMP553 was wired. The outputs are also led through voltage divider to the other parts of the circuit that handle quenching and gating of the SPAD. Other than that, the noninverting output is led through a capacitor to a SMA port, from which it can be wired with a coaxial cable to where it needs to go. The inverting output is similarly led to ground as only one of the outputs is truly needed here, a 50 Ω resistor is used here to match the resistance of the SMA port used on the other complementary output and therefore ensure symmetry. I have made a minor mistake here, the inverting output signal is the one that should have been routed out, as that is the signal, that the subsequent devices in our lab require, however this can be easily fixed by connecting inverting transformer after the output, which inverts the signal. This mistake was fixed in following versions. [24]

The comparator in the single photon detector operates in a manner that is described in

Chapter 3.3. When the detector is idle, specifically for this detector that is when the reference voltage is higher by 19 mV than the voltage on SPAD anode, the noninverting output is in a LOW output state which corresponds to the value of +2,0 V. After a successful photon absorption results in the breakdown of the SPAD the voltage on the diode anode becomes higher compared to the reference value and the output swings to the HIGH value, which corresponds to +2,3 V.

In Fig. 18 is a screenshot of a oscilloscope showing the function of a single photon detector featuring the new ADCMP573, in this particular test the SPAD is replaced by a capacitor, so only the electric control circuit is tested. The graph number 2 shows an initial gating signal, which commences the detector function. Whereas the graph number 1 monitors the detector noninverting output, specifically the SMA port that is connected to the output. It is seen that shortly after the gating signal the output switches to a value of +0,3 V. This test indicates that ADCMP573 comparator functions properly inside the electric control circuit and the implementation was successful.

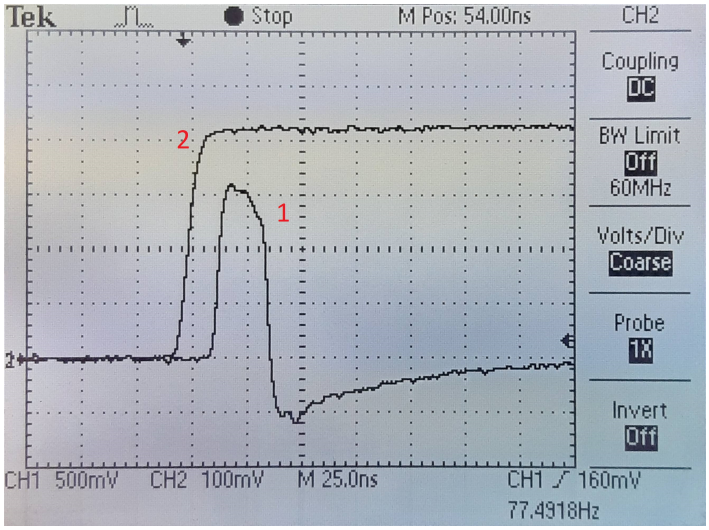
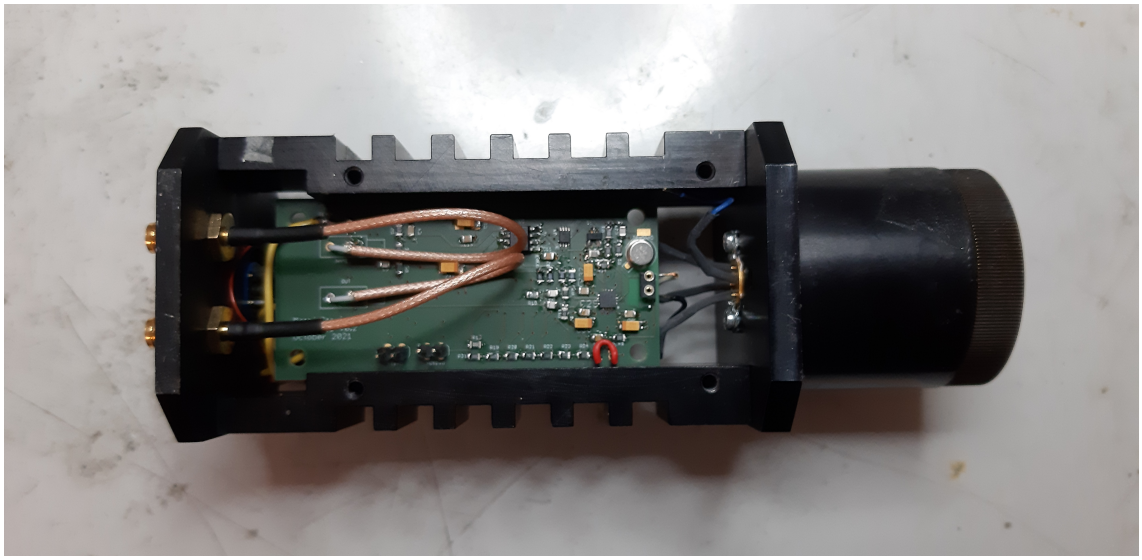


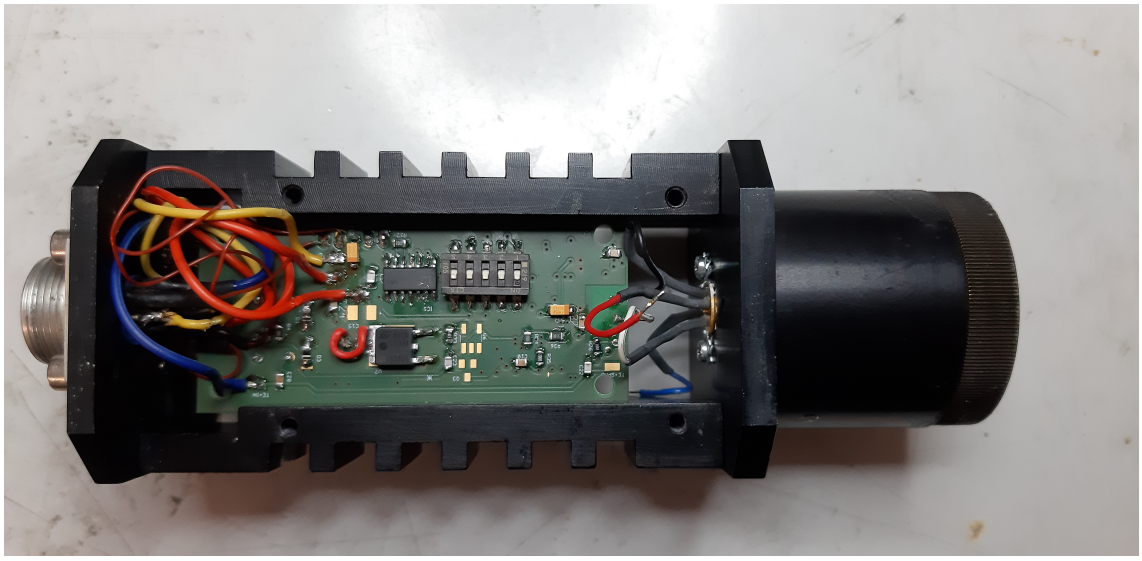
Figure 18. Oscilloscope screenshot showing signal development on single photon detector noninverting output connected to SMA port (1) after a successful detection following a gating trigger input signal (2).

4.4 Integrated detector package

In the end the completed the PCB containing the electric control circuit, including the new ADCMP573 comparator, is mounted and properly connected inside a final metal detector package, this is shown in Fig. 19. On the right side of both of these pictures we can see the housing of the input optics inside of which the SPAD is located. The SPAD is connected to the PCB through a series of cables that can be seen on the right side of the PCB. On the left side of the top picture are two SMA ports that are wired to the PCB. The higher one is a gating signal input, while the lower one is the detector output. On the left side of the bottom picture is a 12-pin port which is wired to several areas on the PCB, these areas correspond to the power supply, detector temperature measurement and cooling of the SPAD. The SPAD cooling remains unconnected for our use. An associated power supply using appropriate 12-pin connection needs to be used with the detector.



(a) Top view.



(b) Bottom view.

Figure 19. Final detector package containing the electric control circuit, SPAD, input optics and connector ports.

4.5 Associated power supply

In Fig. 20 is the power supply associated to the semiconductor single photon detector. The supply feeds power directly from the electrical grid, and it is connected to the detector with a 12-pin connecting cable, that can be seen in the above-mentioned picture. The power supply is capable of generating stable supply voltage of +5,0 V and +35,0 V. It is also responsible for measurement of the detector temperature and regulation of SPAD cooling. The SPAD cooling remains unconnected inside the detector package for our use. At the back of the supply are two testing points, one for GND and the other for voltage corresponding to the detector temperature, where the conversion characteristic is 1 mV = 1 °C. At the front of the supply is a green led diode indicating its on/off status.

(a) Front view. (b) Rear view.

Figure 20. Photo of the power supply associated to the semiconductor single photon detector.

Chapter 5

Temperature stability measurements

As was mentioned in the previous text, the true capabilities of the new SPAD TE1 v0.2 semiconductor single photon detector need to remeasured and affirmed in our lab where we can attain results with the highest possible accuracy. This will be the content of the following chapters.

5.1 Bias voltage V_a temperature drift measurement

According to the theory explained in Chapter 2.4, induced bias voltage V_a temperature drift can be used to compensate for the natural breakdown voltage V_{BD} temperature drift or if set properly, it can even improve the overall performance of the single photon detector. To do this the induced temperature V_a drift needs to slightly exceed the natural V_{BD} temperature drift. In this chapter, I will be testing different value settings of the R16 and R24 resistors (viz. Fig. 39) and measuring the resulting bias voltage V_a temperature drift.

Initially I have measured the breakdown voltage of the SPAD at room temperature to be at roughly 29,34 V. The bias voltage V_a needs to always stay above this value, otherwise the detector will cease to function. Through the adjustable resistor, which in the detector electric circuit is represented by switch SWS005 and several serially connected resistors of varying values (viz. Fig. 39), I have set the bias voltage value to $V_a = +31,3$ V, by having the number 1 and 2 switches ON. Afterwards, I have measured the bias voltage V_a temperature drift by heating the whole package with a heat gun while monitoring the bias voltage value V_a (or U_{SPAD}) on the testing point JP2 (viz. Fig. 39). I have done this for several values of the combined resistance of R16 and R24 resistors. The results of this measurement are in Fig. 21.

This graph can be later used for tilting the curve expressing the propagation delay dependency on temperature and therefore achieving propagation delay that is almost invariable on temperature, similarly to what is shown in Fig. 9. I have chosen to use resistors R16 = 3,3 kΩ and R25 = 15 kΩ for the following measurements. This setup corresponds to the voltage bias V_a temperature drift of 35,2 mV/K, a value, which according to the available data, should be near ideal.

5.2 Propagation delay measurement

Propagation delay is one of the most important characteristics of the semiconductor single photon detector, and so is the propagation delay's volatility towards changes in external conditions. As was explained in in Chapter 4.1, it was previously concluded that the comparator contained inside the electric control circuit plays major role in the determining the final value and behaviour of the propagation delay. Therefore, it is now necessary to remeasure the propagation delay stability of the new detector package, which includes the

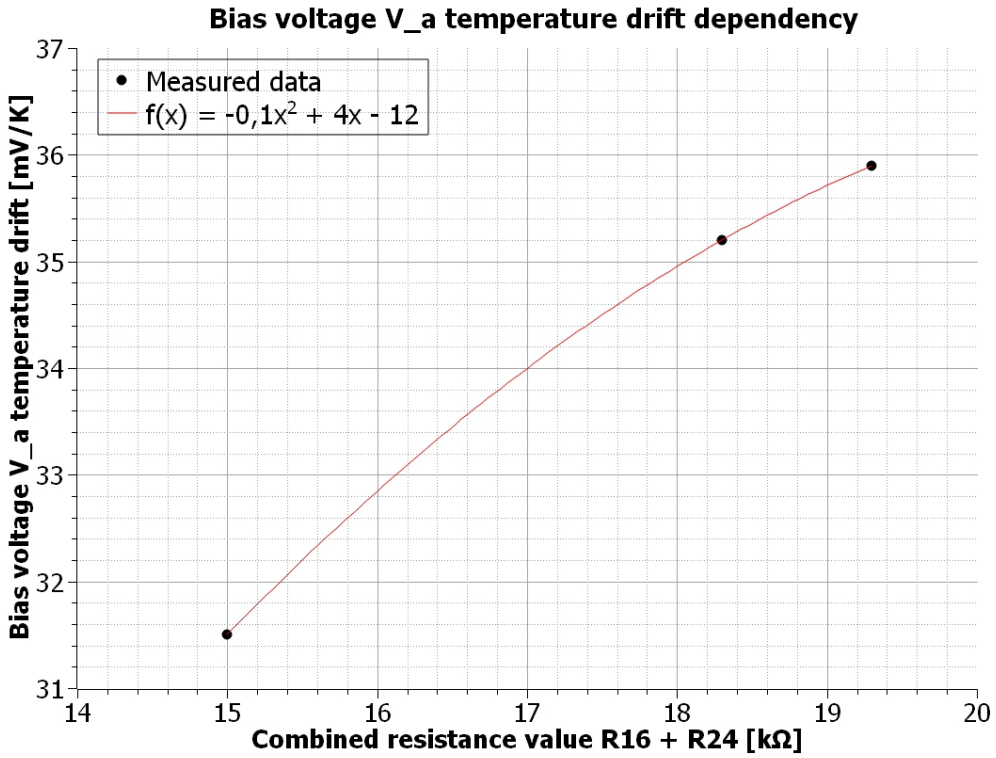


Figure 21. Graph showing the bias voltage V_a temperature drift dependency on the combined resistance value of R16 and R24 resistors.

ADCMP573 comparator, to ensure that the new comparator is indeed a good replacement for the ADCMP553 comparator that is used in the current design.

5.2.1 Time correlated single photon counting experiment setup

To measure the propagation delay I have built a time correlated single photon counting experiment similar to the one shown in Fig. 22. In this particular picture the ps trigger laser pulse comes from the left side and is split into two beams of equal optical length. The strong (multi-photon) part is detected by a fast linear photodiode PD, and the weak part (single photons) is detected by a photon counter SPAD. This kind of setup allows for the most precise of measurements as the optical delay is eliminated since the optical paths are equal. [6]

In Fig. 23 is the block scheme of the complete time correlated single photon counting experimental setup from laboratory number 313 at CTU FNSPE in Prague, which was used to confirm the properties of the new single photon detector featuring the ADCMP573 comparator. It is in essence similar to the one shown in Fig. 22, but it allows for the detector's temperature control and, since I'm only measuring the relative change in propagation delay, it doesn't necessarily require equal optical paths for the measured and the reference signal. The experiment is initiated by the HAMAMATSU C4725 laser pumping, which powers the laser head and generates the gating pulse for the single photon detector. The laser generates radiation at 780 nm and the pulses are FWHM 42 ps long, the beam is split two ways. The stronger part proceeds to a optical trigger, while the weaker part is direc-

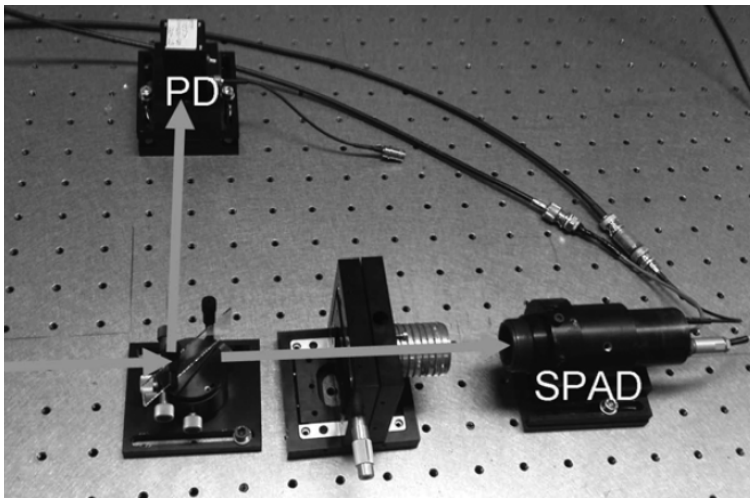


Figure 22. Photo of a time correlated single photon counting experiment setup, taken from [6].

ted towards the thermobox and the detector inside it. The thermobox allows for heating or cooling of the detector, all the while the changes in its propagation delay are measured in the NPET by comparing it to the stable reference optical trigger. The time measurement system determines the time interval between the arrival of these two signals and the information is stored in a PC.

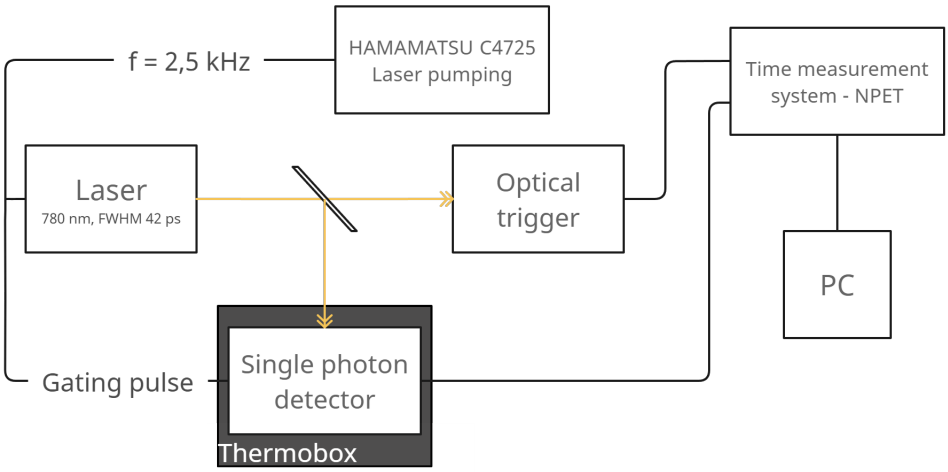


Figure 23. Block scheme of the complete experimental setup from laboratory number 313 at CTU FNSPE in Prague, which was used to confirm properties of the new single photon detector featuring the ADCMP573 comparator.

In Fig. 24 is photo of the aforementioned experimental setup from laboratory number 313 at CTU FNSPE in Prague, marked within the photo are the individual parts of the time correlated photon counting measurement. Marked with number 1 is the HAMAMATSU stabilized picosecond light pulser C4725 that powers and controls the laser. The laser pumping can generate either singular manually activated pulses or automatic periodic pulses, these are timed internally or by an external trigger. I'm using the internal setting to generate periodic pulses with period of 400 μs. This particular period was chosen because it matches the maximal processing ability of the time measuring system used,

which operates at 2,5 kHz. It's also possible to drive the trigger out, either with or without a delay. The trigger out pulse, with an additional delay of 60 ns, is used as the gating pulse for the single photon detector. Number 2 marks the diode laser that generates near infrared light at 778 nm with pulse width of 42 ps and maximum peak power of 188 mW. The laser itself is attached to a holder, which allows for its path to be adjusted with screws. Number 3 is a semitransparent mirror that splits the beam, majority of the beam passes through, but a small part is reflected to the side. The stronger part of the beam travels to a fast linear photodiode, which serves as a optical trigger. The smaller part is directed towards an optical input of a thermobox, which houses the semiconductor single photon detector. Series of filters is placed in the optical input to attenuate the incoming signal as well as to eliminate the artificial lighting of the laboratory.

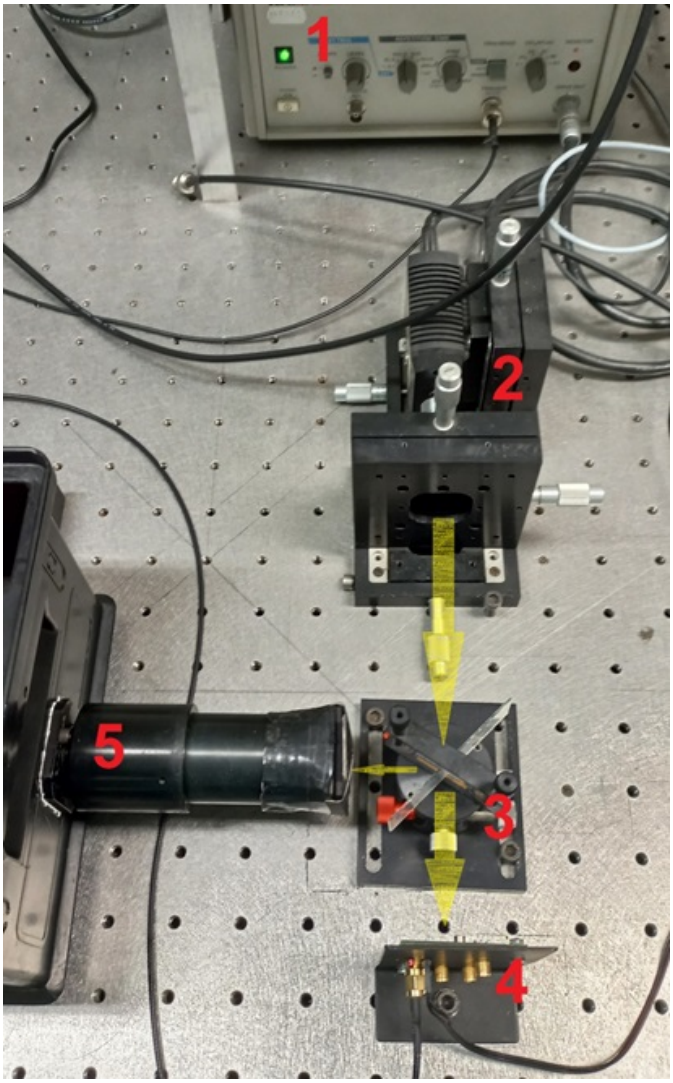


Figure 24. Photo of the experimental setup from laboratory number 313 at CTU FNSPE in Prague, which was used to confirm properties of the new single photon detector featuring the ADCMP573 comparator.

Thermobox

Fig. 25 shows inside of the thermobox that was previously shown in Fig. 24. Mounted to one side of the thermobox, the side on which the input optics are located, is the semiconductor single photon detector package. The package is surrounded by heat insulation to ensure better efficiency for when sources of heat or cold are placed around it during the following measurements. Connected to the detector is the 12-pin cable from the power supply as well as two coaxial cables, these were previously described in Chapter 4.5. The upper one is carrying the gating signal from the HAMAMATSU stabilized picosecond light pulser. The lower one is carrying the output signal out of the thermobox and towards the time measurement system.

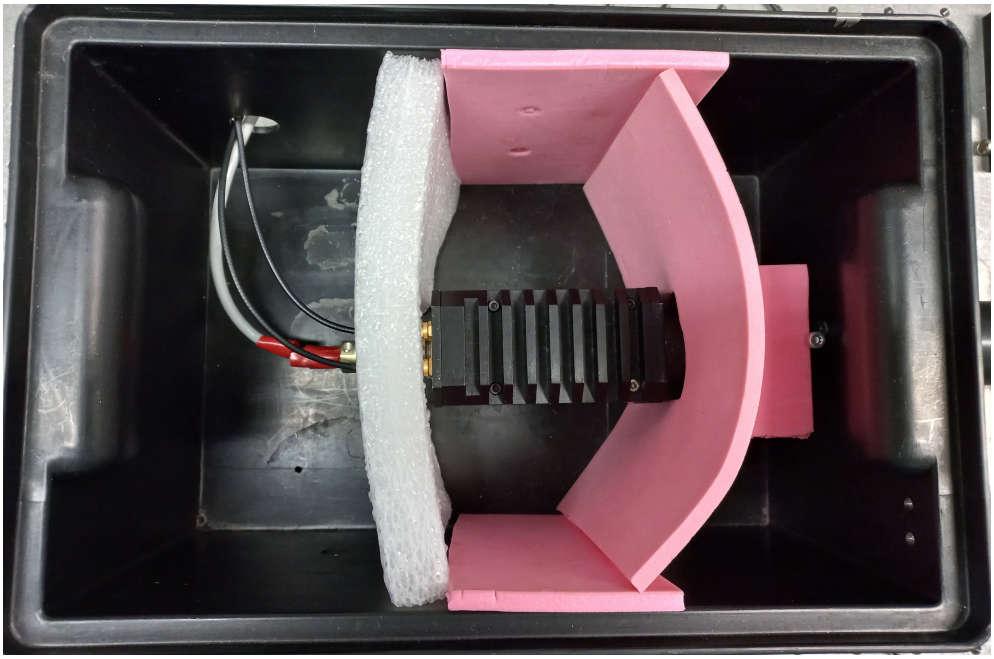


Figure 25. Photo of inside of the thermobox, which is seen in Fig. 24 as part the experimental setup for confirming properties of the new single photon detector featuring the ADCMP573 comparator.

The time measurement system

Shown in Fig. 26 is the time measurement system. The core of this system is the New Pico Event Timer & Two Ways Time Transfer (NPET). Connected to the first inputs (IN1) of both its channels are two black coaxial cables, one of them carries output signal from the fast linear photodiode, while the other one carries output signal from the single photon detector. The NPET processes these two signals and measures the time delay inbetween their arrival. This information is subsequently sent to the attached white computer, which records the measured data. The computer is also used to control the NPET settings.

The NPET clock is a timing device that uses a surface acoustic wave filter to indicate time. This clock typically has a high time-related stability of up to around 4 fs. This method of time interval measurement is based on the fact that a surface acoustic wave filter excited by a short pulse can generate a finite signal with a highly suppressed spectrum outside a narrow frequency band. Thus, once the responses to two consecutive excitations

Figure 26. Photo of the time measurement system, consisting of the NPET clock and computer, that was used for confirming properties of the new single photon detector featuring the ADCMP573 comparator.

are sampled at clock ticks, they can be accurately reconstructed from a finite number of samples, and the time interval between the two excitations can be determined. [29]

Computer control

Before the NPET can be used for precise time interval measurements its two channels need to be synchronised. This can be done by launching the 'two_npet_sync.exe' program located on the computer, this program uses the internal computer time to synchronize the two NPET channels together. After this is done, the measurement can be simply commenced by opening the 'npets.exe' program. The parameters of the measurement can be adjusted by editing the 'NPETconfig.txt' file. The adjustable parameters are minimum and maximum range, standard deviation used for averaging, baud rate, etc.

Once the measurement has begun, all of the measured data is recorded and appended to a single 'stat.txt' file. In case the file is deleted, it is created anew once another measurement begins. The data is recorded in format that is show in Tab. 1. The first column notes the computer times in seconds at which the measured value was taken. The measured propagation delay in nanoseconds and jitter in picoseconds are shown in the second, resp. third column. Value written in the fourth column describes the percentage of accepted measured values, i.e. values that are within the range specified in the configuration file.

computer time [s]	propagation delay [ns]	delay jitter [ps]	Values within accepted range [%]
xxxxx.xxxxx	x.xxxxxx	x.xxxxxx	x.x

Table 1. Table showing format in which time interval data measured by the NPET is recorded.

5.2.2 Temperature stability analysis

The experimental setup described in the previous chapter was used to test the propagation delay temperature stability of the new detector package containing the ADCMP573 comparator. The NPET settings for this measurement, as entered in the computer control, were: range of accepted values from 8,0 to 8,3 ns; 500 points in statistic; standard deviation of 2,1 σ; baudrate 576000 Bd; frequency of incoming pulses 2,5 kHz.

By introducing sources of heat or cold into the insulated part of the thermobox (viz. Fig. 25), I have regulated the detector temperature, which I have monitored using the testing point at the rear of the associated power supply (viz. Chapter 4.5). Specifically, I have employed dry ice to quickly cool the detector and then performed the measurement while the dry ice was sublimating and the detector was slowly warming. After the detector was restored back to room temperature, I have used a heat gun to gradually, step by step, heat the detector to the desired temperature, all the while writing down the measured temperature values. I have found the detector to react wildly to very steep changes in temperature, which is why in duration of the measurement the speed of temperature change was kept in moderate levels.

As was shown in Tab. 1, the time measuring system records the measured values along with information of the time they were recorded. Similarly, I have written down the measured detector temperatures along with the time they were measured. Since the NPET clock is synchronized against the computer time, then as long as the computer time is correct, it is possible to match the times of these two measurements and hence arrive at final propagation delay temperature dependency.

In the end, I have measured the temperature range of -20 to +50 °C. The detector is not expected to behave irregularly beyond this range since the problematic point should be somewhere around 20 °C. The results of this measurement are shown in Fig. 27. As shown in the graph, the resulting dependency is linear with growth coefficient of $0,14 \pm 0,01$ ps/K. The resulting dependency being linear means a marked improvement from the previous version of the detector. The growth coefficient itself can still be adjusted using the graph established in Chapter 5.1, but the current coefficient is already very acceptable. It can be concluded that the comparator replacement was successful and the ADCMP573 comparator is fit to be used in the semiconductor single photon detector. The only thing left to do is acquire space qualification for the new detector design.

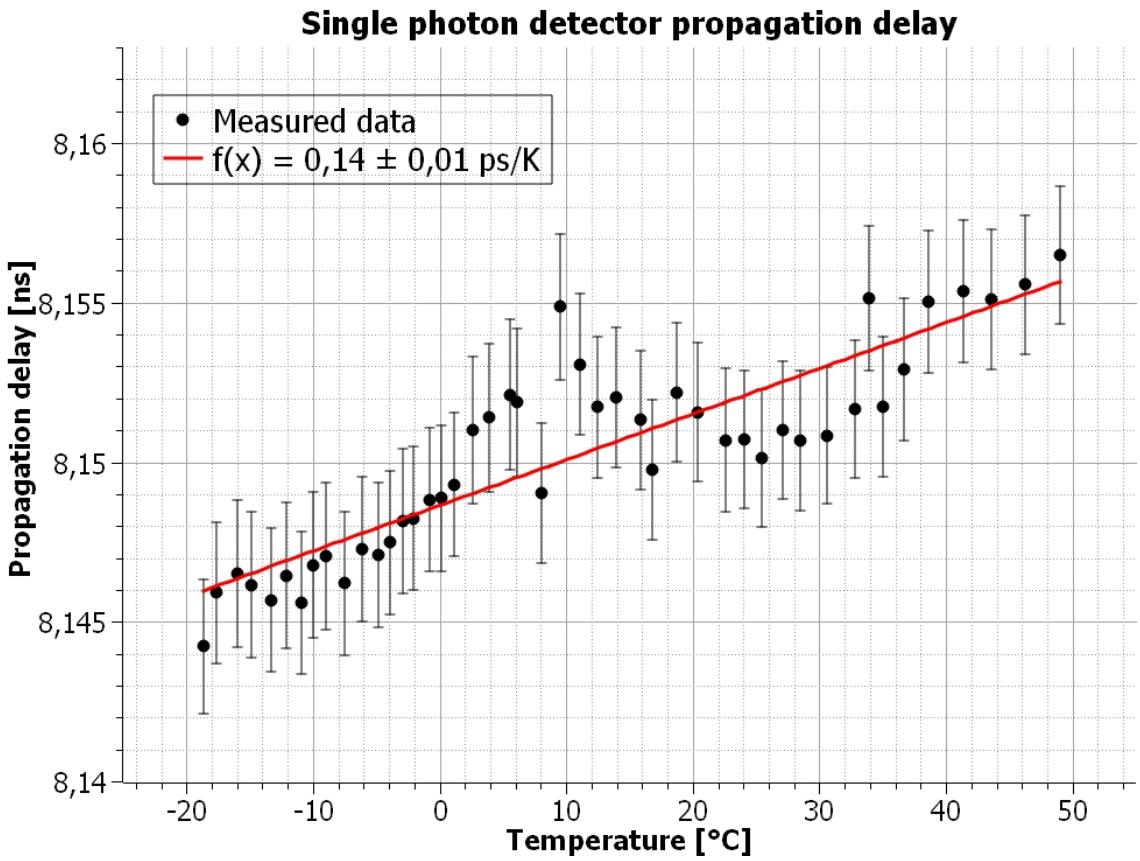


Figure 27. Graph showing propagation delay dependency on temperature for the new semiconductor single photon detector containing the ADCMP573 comparator.

Chapter 6

Quenching speed upgrade

Quenching speed describes the time interval in which the control circuit lowers the high voltage applied to the SPAD after its breakdown has already occurred. It plays an important role in defining the detector's final abilities. Higher quenching speed allows the detector to be operated at higher frequencies and decreases the afterpulsing, hence lowering the effective dark count rate.

6.1 Voltage divider replacement

My colleague Tomáš Novotný theorized in his bachelor thesis "Nový řídící elektronický obvod detektoru jednotlivých fotonů pro kosmické projekty" (New electric control circuit of single photon detector for space projects) [30], that the duo of voltage dividers currently used at the beginning of the quenching part of the control circuit is completely unnecessary and that they are in fact responsible for considerable delay in the detector quenching speed. Namely these are comprised of resistors R27, R28, R29, R30 in Fig. 39, 40, shown in Fig. 28 is a simplified block scheme of the related part of the circuit. These voltage dividers decrease the amplitude of detector output signals that are then directed into the differential receiver (specifically into the SN65LVDS9637BD, viz. 39). These two voltage dividers are part of the original detector design developed for space application, but at this point noone really knows the reason for their usage in this part of the circuit. However, due to the rather high resistance value of the involved resistors, they can introduce a non-negligible quenching speed delay to the detector. Additionally, after reviewing the differential receiver datasheet, it would seem that the subsequent parts are perfectly capable of handling the full power output signals and there is no real need for the continued use of these voltage dividers. As such, in this chapter of my master thesis I will be testing out the possible replacement or removal of these voltage dividers.

I have measured the quenching speed of the detector by measuring the propagation delay of the quenching circuit, which is represented by the FWHM of the detector output signal. This interpretation was chosen because the rising edge of the output pulse serves as the trigger pulse of the quenching circuit and the falling edge of the output pulse represents the moment when the circuit has been successfully quenched. I have performed a series of experiments in which I have used various combinations of resistors that comprise the aforementioned voltage dividers and then measured the resulting FWHM of the output signal using a Tektronix DPO7254 oscilloscope with 2,5 Ghz bandwidth. The most important results of these experiments are shown in Tab. 2.

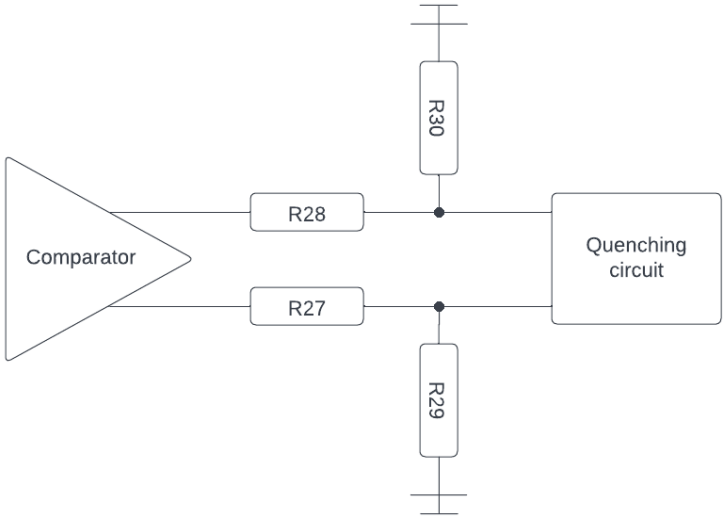


Figure 28. Simplified block scheme of a part of the single photon detector circuit (Fig. 39, 40) which contains the possibly redundant voltage dividers.

R27/R28 [Ω]	R29/R30 [Ω]	Pulse width FWHM [ns]
1000	5100	23
330	-	18
50	-	16,6
0	-	16,3

Table 2. Table showing results of measurements of FWHM of the output pulse based on the resistors used in the above discussed voltage dividers.

According to these measurements the detector can function properly without the use of voltage dividers and as such it is pointless to continue employing them. Furthermore, by removing them I have achieved decrease in output pulse width, i.e. increase in the quenching speed. From the results in Tab. 2 we can see, that decreasing the resistance value of the resistors decreases the output pulse width and it would seem, that outright removing all the resistors is the best choice. However, when examining the shape of output pulses for R27/R28 = 0 Ω, it can be seen that the output features an overshoot on both the rising and falling edge of the pulse, viz. 29, and this is an unwanted property. As such we cannot simply remove all the resistors.

The next best option would be using the R27/R28 = 50 Ω as this setup doesn't introduce an overshoot to the output pulse, while keeping minimal output pulse width. I have also observed the other characteristics of the output pulse and found, that they aren't negatively influenced by this change in the voltage divider. As such we have decided to replace the voltage divider with the 50 Ω serial resistor connection in all future designs.

Figure 29. Oscilloscope screenshot showing the output pulse of the single photon detector, an overshoot is visible on the rising and falling edge.

6.2 Integrated circuits modernization

Based on the experience of upgrading the comparator and removing the redundant voltage divider, we've decided to review and attempt to modernize the remaining integrated circuits in the quenching circuit to further increase the quenching speed. The integrated circuits in question are denoted U3 and U4 in Fig. 39. They are, in order, a high-speed differential receiver by Texas Instruments and a D flip-flop by onsemi. These components are also shown in Fig. 30, which displays a simplified block scheme of the AQGC currently used in the single photon detector, it is similar and it operates the same way as the one shown and discussed in Fig. 5.

The first step in the upgrade process is to measure and establish the component's propagation delay directly inside the detector. To do this I have decided to introduce a defined trigger pulse in lieu of the SPAD diode inside the detector, as is shown in Fig. 31. I have defined the propagation delay of all the subsequent integrated circuits as the time difference between their input reaching 50% maximum value and their output doing so. These events were observed on the Tektronix DPO7254 oscilloscope, from which the resulting time difference was read. The results are in Tab. 3.

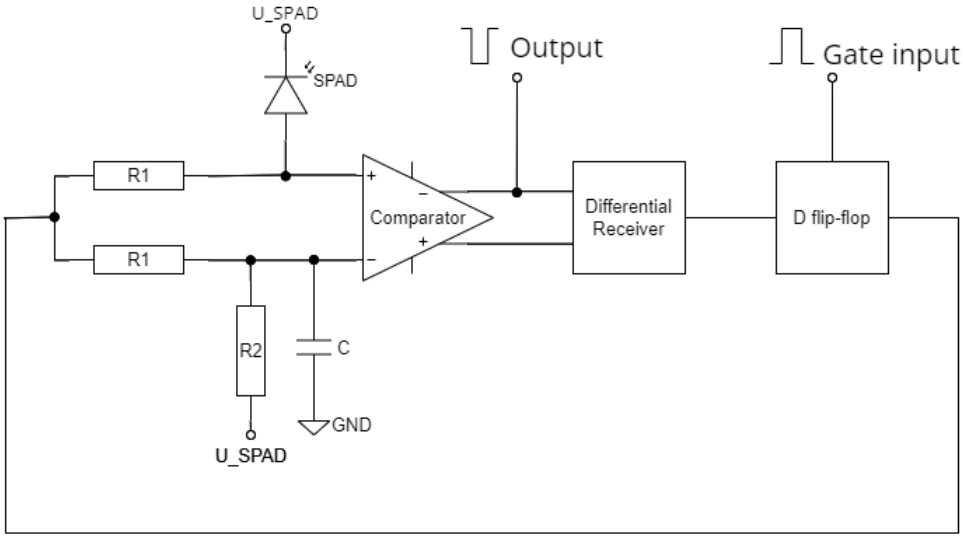


Figure 30. Simplified block scheme of the AQGC currently employed in the single photon detector.

Component	Measured propagation delay [ns]
Comparator ADCMP573BCPZ-R2	< 0,1
Receiver SN65LVDS9637BD	4,1
D flip-flop NL17SZ74USG	1,6

Table 3. Table showing results of measurements of propagation delay of the individual components in the quenching circuit.

From the previous section we know that the total propagation delay of the AQGC is 16,6 ns. However, from this measurement we also know that the three integrated circuits that comprise the circuit have combined propagation delay of less than 6 ns, which leaves us with more than 10 ns unaccounted for. Some of this time may be used up on the Q1 transistor (viz. 39), the passive components as well as the connections, but it definitely shouldn't amount to this much. In the end we have concluded that the remainder of the unaccounted time is credited to the inner processes of the SPAD and therefore it cannot be influenced by simply replacing the integrated circuits in the quenching circuit.

Although majority of the quenching propagation delay is not influenced by the aforementioned components, I have still researched candidates for replacement of the said components and although I have found some with potentially slightly better propagation delay, the difference was not significant enough to warrant this change from an already established and functional setup. As such for the time being we have decided to abandon the idea of replacing these integrated circuits employed in the AQGC.

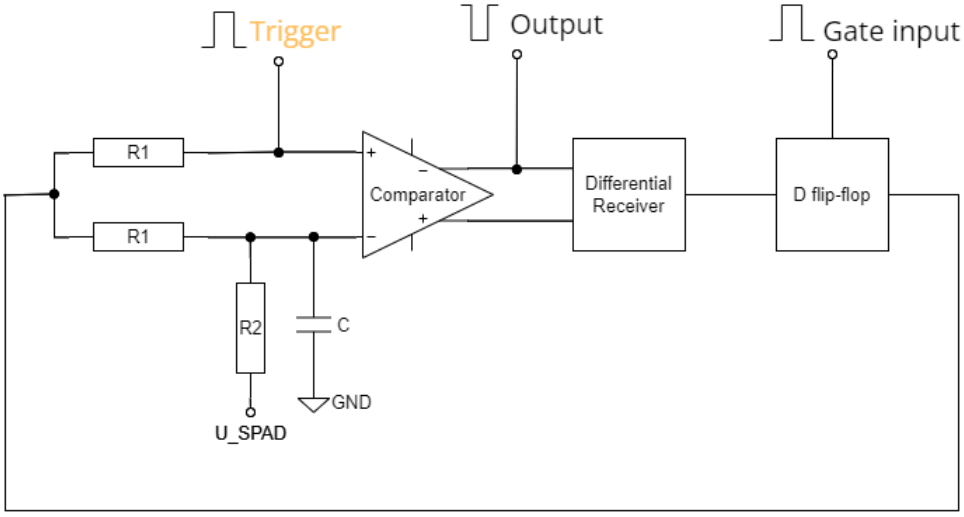


Figure 31. Simplified block scheme of the AQGC currently employed in the single photon detector, modified showing the defined trigger pulse.

Chapter 7

Continuously operated single photon detector

Although it goes beyond the scope of the master thesis assignment, as it was defined at the beginning of the thesis, I have decided to further my work by additionally researching continuously operated single photon detectors (CW detectors) that are developed at CTU FNSPE for expected application in quantum communications. Even the single photon detectors developed for laser time transfer were originally meant to be continuously operated and it was only at a later time that gating was included as it was deemed necessary due to otherwise high background photon flux. This version of single photon detectors was previously mentioned in Chapter 2.2 as part of the description of the gating function of the electric control circuit, these detectors are completely lacking such a function. These detectors are comprised of the very same SPAD and a control circuit, however, this control circuit can only detect the edge of the onset of electric current and quench. The absence of one of the main functions means quite a simplification in the design of the control circuit, but also imposes limitations on the function of the detector. [31]

Due to the lack of gating, the CW detectors are incapable of synchronizing their times of active detection with the incoming signal. Instead, the times of active detection and the deadtime continuously follow one after each other. The deadtime can be set and maintained to last for a certain period of time, but the active time of detection lasts until the breakdown of the diode, which is an event that happens after statistically varying periods of time. This means that these detectors are also incapable of operating with certain defined period, which would enable them to accept periodic signals that could be manually delayed to match with the operation of the detector. As such, by definition, these detectors feature higher dark count rate than their gated counterparts, since the incoming signal can quite often arrive during deadtimes of the detector. This isn't necessarily a hindrance for application where there is no gating signal available to begin with and it can be compensated for by simply gathering more data and then carrying out a more sophisticated data analysis.

7.1 CW detector upgrade

Inspired by the success of the gated detector, I have attempted to update the current design of the CW detector developed at CTU FNSPE by replacing the comparator that is used at the core of the detector's control circuit with a more modern counterpart and hopefully achieve overall improvement in the detector's characteristics. In Fig. 41 is scheme of the current CW single photon detector, and in Fig. 32 is a close up of the section containing the comparator, comparators in general were described in Chapter 3. The comparator currently in use in the CW detector is MAX961 by Maxim Integrated.

The control circuit connection shown in Fig. 32 is similar to the one used in a gated detector, shown in Fig. 30, the difference is that there are no further integrated circuits connected behind the comparator. Instead, the comparator output leads directly to the beginning

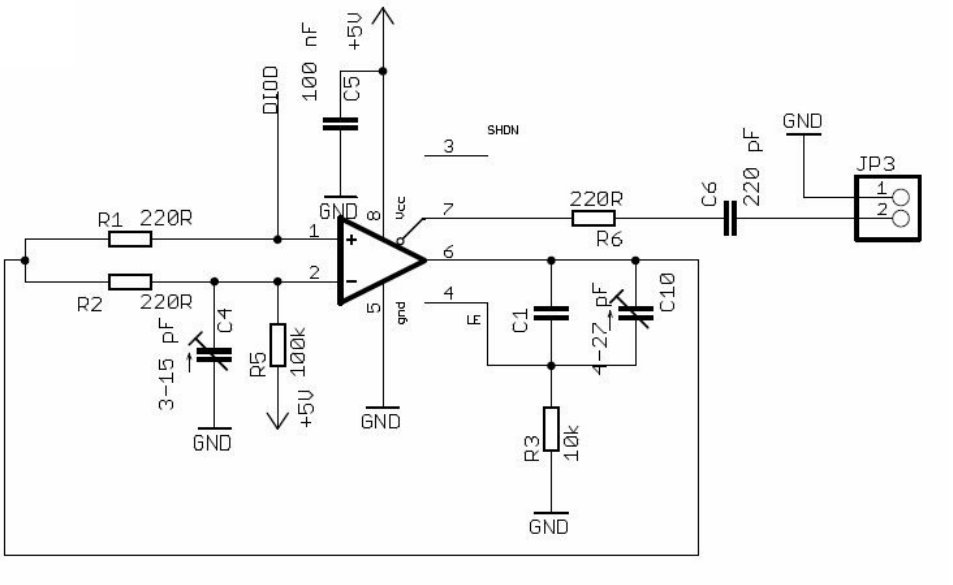


Figure 32. Section of the scheme of CW single photon detector (viz. Fig. 41) containing the comparator.

of the circuit, therefore a triggering of the comparator leads to immediate quenching of the SPAD. The comparator output is also routed to the latch pin of the comparator through a RC circuit (C1,C10,R3) that contains a trimmer capacitor (C10). This connection means that once the comparator is triggered it quenches the diode and keeps it quenched for as long as the latch is held, this period of time can be regulated with the trimmer capacitor and it represents the deadtime of the detector. Once the latch is released the SPAD is no longer being quenched, hence it is once again biased above the breakdown voltage and another detection can occur. Typical deadtimes range from tens to low hundreds of nanoseconds. The complementary output of the comparator leads to the detector package output.

I have chosen three candidates for the possible replacement of the MAX961 comparator [32], namely they are AD8611 by Analog Devices [33], ADCMP601 by Analog Devices [34] and LT1711 by Linear Technology [35]. The next step is to test the detectors that employ these comparators. However, to completely build three separate detectors, each with one of the comparators, is unnecessarily complicated. As such I have decided to design testing printed circuit boards (PCB), which will all contain only the part of the circuit equal to what is shown in Fig. 32 and the remaining parts of the circuit will be either omitted or connected externally. Since this is quite a simple task I have also decided to design one of these test PCBs for the MAX961 comparator to reaffirm its properties.

7.2 Test printed circuit boards

The test PCBs are all two layered. They contain the comparator and all its necessary connections, power source connections, a coupling for SPAD and connection for V_a, the voltage applied to SPAD, marked in the schemes as U_SPAD. The comparators all have their latch connected using a RC circuit which defines the deadtime of the detector. The

complementary comparator output is routed through serially connected resistor and capacitor into a coaxial cable. In Fig. 33 is a photo of all the four PCBs, they are described in detail in the following text.

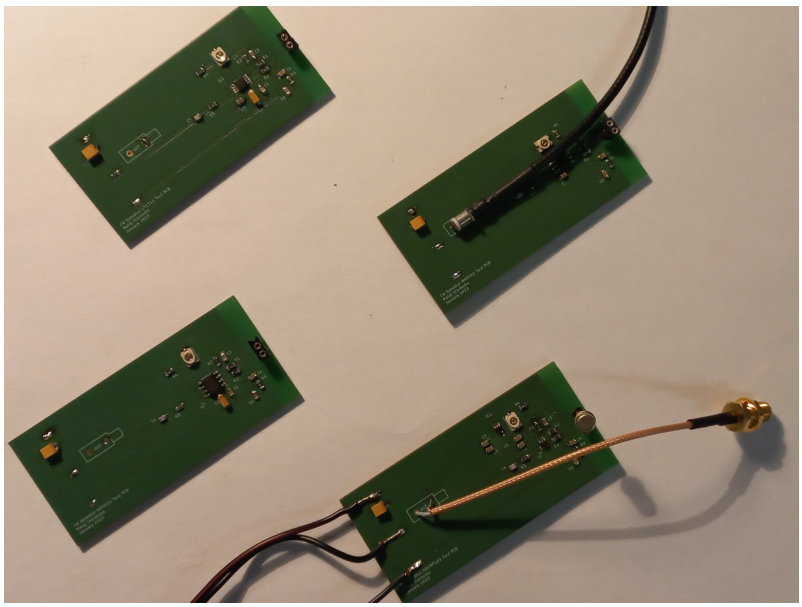


Figure 33. Photo of all the four test PCBs.

MAX961

In Fig. 42 is scheme of the MAX961 test PCB that was used to reaffirm the properties of MAX961 comparator in the CW single photon detector. Connected to the inputs of the comparator is the anode of the SPAD and the reference voltage in very much the same was as if it was a gated detector. The comparator is powered by external supply and it can accept supply voltage V_CC in range of +3 V to +5 V. The GND pin and the Shutdown pin are both connected to ground plane, the shutdown function is not needed in our application. Since latch is active for HIGH voltage value, the latch is connected to the noninverting output, so that breakdown of the SPAD results in triggering of the comparator and the output signal is then held for period of time defined by the RC circuit consisting of resistor R4 and trimmer capacitor C5, this period of time is the detector's deadtime.

AD8611

In Fig. 43 is scheme of the AD8611 test PCB that was used to asses the properties of AD8611 comparator in the CW single photon detector. The AD8611 comparator is connected almost identically to the MAX961 comparator discussed in the previous section, except for a few differences. There is no shutdown pin on the AD8611, instead it has negative supply pin, but just as the shutdown pin previously, it is connected to ground plane. The latch connection remains the same, however, the AD8611's latch only functions for supply voltage higher than +4,1 V, which means that the whole detector also only works

with supply voltage higher than +4,1 V, since the comparator's latch is required for its proper operation.

LT1711

In Fig. 44 is scheme of the LT1711 test PCB that was used to asses the properties of LT1711 comparator in the CW single photon detector. The LT1711 comparator is connected identically to the AD8611, but it accepts supply voltage in a broader range of +2,4 V to +7 V and its latch works along this whole range.

ADCMP601

In Fig. 45 is scheme of the ADCMP601 test PCB that was used to asses the properties of ADCMP601 comparator in the CW single photon detector. This PCB is distinctly different from the previous three and the reason for that is that ADCMP601 has two features that distinguish it from the other comparators, its latch is active for LOW signal and it has no complementary output. As it has no complementary output, the comparator's noninverting output was driven out of the detector, meaning of which the detector's output signal has opposite polarity compared to the rest of the test PCBs. The difference in latch operation wouldn't have posed an issue if the comparator had complementary output as it could have been used to drive the latch LOW, but since that's not possible, I have used a second ADCMP601 comparator with swapped input connections to create a LOW signal for the first comparator's latch, therefore the detector requires two of these comparators. Both comparators require supply voltage in range of +2,5 V to +5 V and the latch feature functions across this entire range.

Unfortunately this kind of detector design didn't work properly, the detector's output signal's leading edge was too gradual, which interfered with the latch control and even by itself, it presented an unwanted property. The underlying reason for this peculiarity is unknown, but since the other the test PCBs did not exhibit such properties, we concluded that it was either because of the comparator itself or because of the complicated way it had to be connected. It would have been been simpler if I haven't used the second comparator and simply switched the inputs of the first one. Ultimately, this comparator was disqualified from this CW detector upgrade and we may try it again in later tests.

7.3 Test CW detectors dark count measurement

Using the test PCBs described in Chapter 7.2 and connecting them to external power sources, I have built three separate CW detectors. To achieve this I have used two independent power sources, the first one could output up to +15 V and it served as the comparator's power supply. The second one was custom build supply that could output voltage ranging from +25 V to +35 V while allowing for extremely fine control, this one was used for providing the U_SPAD (V_A) voltage. To asses the difference between these three detectors, and then choose the most suitable comparator for use in the standard CW detector, I

have conducted a dark count measurement. The detector's dark count was chosen as the determining element because of the detector's expected application in quantum communication, which requires low detection noise levels. To perform this measurement I used SPAD that has been covered in protective case and therefore had no access to outside light/radiation. In this way I have measured the frequency of detector counts that have resulted from the diode breaking down without the absorption of a photon, i.e. frequency of dark counts. The test CW detector that features lowest dark count frequency will naturally be the most stable and suitable one.

7.3.1 Experimental setup

In Fig. 34 is a block scheme of the experimental setup used to measure dark count frequency of the test PCBs discussed in Chapter 7.2. The PCBs were connected to two separate power sources, the first being RNG-1501 that can output up to +15 V, this one was used to power the comparator. The second power supply was custom built in our laboratory, it can output voltage in range from +25 to +35 V and it allows for very fine control with precision of 10 mV. The second power supply was used to provide the bias voltage for SPAD. The test PCBs output was connected to a Tektronix TDS380 400MHz oscilloscope and to a 5370B universal time interval counter. The oscilloscope was used to monitor the detector's deadtime and the universal time interval counter was used to measure dark count frequency. All test PCBs used the very same encased SPAD that had breakdown voltage of V_{BD} = 29,2 V. I used this setup to measure the test CW detector's dark count frequency dependency on comparator's power supply and the detector's deadtime.

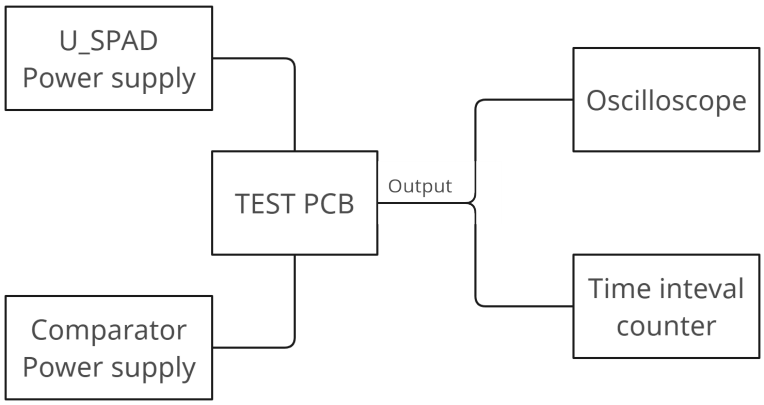


Figure 34. Block scheme of the experimental setup used to measure dark count frequency of the test PCBs discussed in Chapter 7.2, the individual parts of the setup are described in the accompanying text.

7.3.2 Measurement results

I have conducted measurement of dark count frequency for the three test CW detectors, the ADCMP601 comparator, and its test PCB, was previously disqualified, viz. Chapter

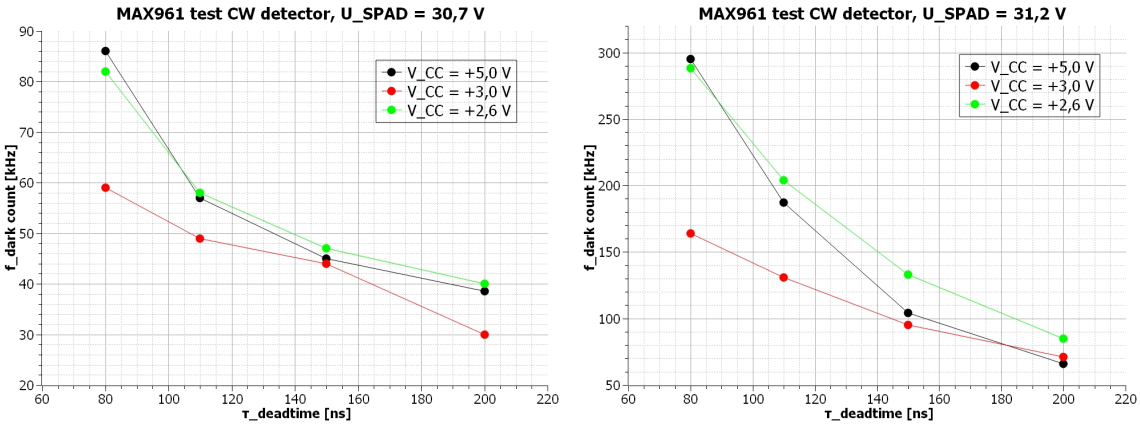
7.2. The same SPAD, that had breakdown voltage V_{BD} = 29,2 V, was used in all the measurements. All the test CW detectors were evaluated at different voltage supply settings, excess bias voltage applied to SPAD and detector deadtimes. The supply voltage settings for each test PCB differed due to different comparators having different limitations. The excess bias voltage values measured were always 1; 1,5; 2 V, i.e. since the break down voltage is V_{BD} = 29,2 V, the bias voltages used were 30,2; 30,7; 31,2 V. The dark count frequency was always measured for deadtimes of 80, 110, 150, 200 ns, these values were chosen because ~70 ns was the absolute lowest that could be set and in out previous measurements I have found out that the frequency remained mostly the same beyond 200 ns deadtime.

MAX961

In Tab. 4 are results of dark count measurement of the MAX961 test PCB that was used to reaffirm the properties of MAX961 comparator in the CW single photon detector, some of these results are also depicted in Fig. 35. MAX961 is the comparator currently used in the standard CW detector design, hence it is the comparator that we are potentially trying to replace. According to the datasheet, the MAX961 comparator can be operated with supply voltage of atleast +3 V, but I have found out that it function even at supply voltage of +2,5 V. The MAX961 comparator that is currently used in the standard CW detector design is power by +5 V voltage supply. However, these recent test, viz. Fig. 35, show that this comparator actually performs best with supply voltage of +3 V.

		V_CC [V]:	5,0	3,0	2,6
U_SPAD [V]	τ_{dead} [ns]		$f_{darkcount}$ [kHz]		
30,2	80		30	23	27
	110		25	23	25
	150		23	22	23
	200		20,5	22	20,5
30,7	80		86	59	82
	110		57	49	58
	150		45	44	47
	200		38,5	30	40
31,2	80		295	164	288
	110		187	131	204
	150		104	95	133
	200		66	71	85

Table 4. Table showing results of dark count measurement of the MAX961 test PCB, where U_SPAD (sometimes noted as V_a) is the voltage applied to the SPAD, τ_{dead} is the deadtime of the detector, V_CC is supply voltage and $f_{darkcount}$ is dark count frequency.



(a) U_SPAD = 29,2 + 1,5 = 30,7 V.

(b) U_SPAD = 29,2 + 2 = 31,2 V.

Figure 35. Graphs showing the results of dark count measurement of the MAX961 test PCB for different supply voltage V_CC, deadtimes τ_deadtime and bias voltage U_SPAD.

AD8611

In Tab. 5 are results of dark count measurement of the AD8611 test PCB that was used to asses the properties of AD8611 comparator in the CW single photon detector, some of these results are also depicted in Fig. 36. According to the datasheet, the AD8611 comparator can be operated with supply voltage of atleast +4,1 V. I have found out that it function even at supply voltage of +3,9 V, but it behaves erratically at this exact value and so I've chosen to stay with the recommended value of lowest supply voltage +4,1 V. The measurements results turned out to be almost identical for different supply voltage except for bias voltage 31,2 V, which can be seen in Fig. 36, in this measurement the detector powered by +5 V performed slightly better. Therefore, I have concluded that the AD8611 comparator is best to be operated at +5 V power supply.

		V_CC [V]:	5,0	4,1
U_SPAD [V]	τ_{dead} [ns]		$f_{darkcount}$ [kHz]	
30,2	80		26	27
	110		25	25
	150		24	24
	200		24	23,5
30,7	80		70	68
	110		55	56
	150		47	47
	200		42,5	43
31,2	80		220	180
	110		163	160
	150		102	130
	200		73	97

Table 5. Table showing results of dark count measurement of the AD8611 test PCB, where U_SPAD (sometimes noted as V_a) is the voltage applied to the SPAD, τ_{dead} is the deadtime of the detector, V_CC is supply voltage and $f_{darkcount}$ is dark count frequency.

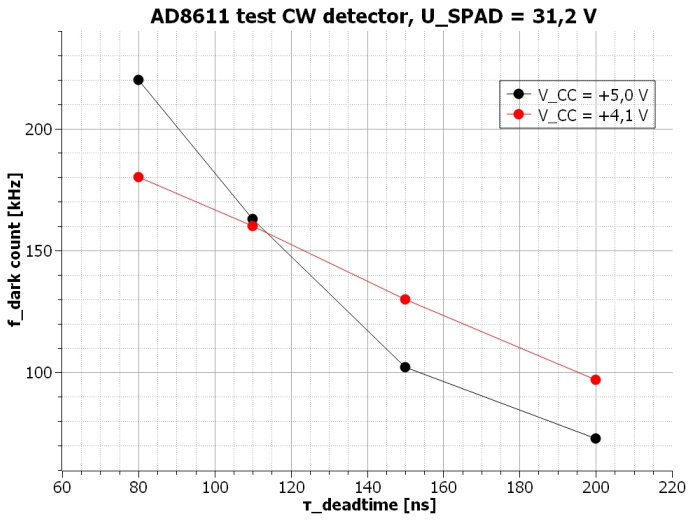


Figure 36. Graph showing the results of dark count measurement of the AD8611 test PCB for different supply voltage V_CC, deadtimes τ_deadtime and bias voltage U_SPAD = 29,2 + 2 = 31,2 V.

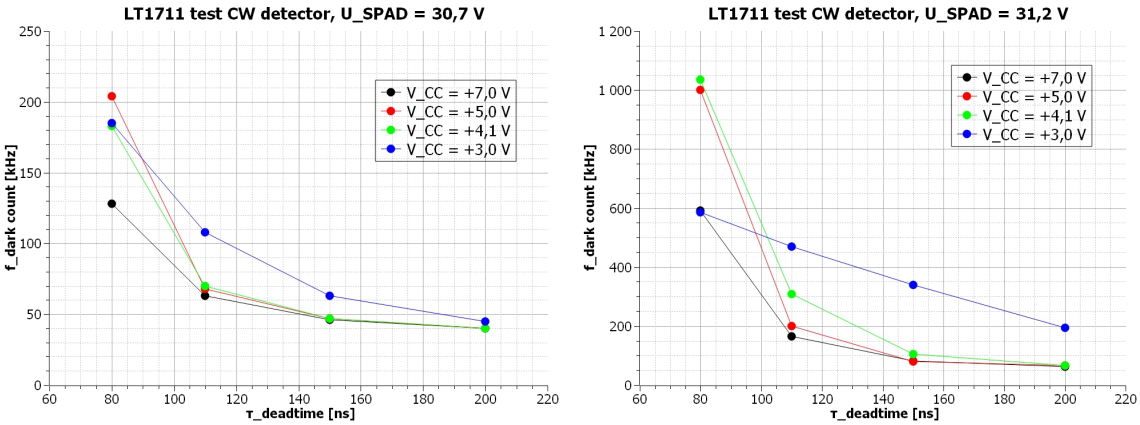
LT1711

In Tab. 6 are results of dark count measurement of the LT1711 test PCB that was used to asses the properties of LT1711 comparator in the CW single photon detector, some of

these results are also depicted in Fig. 37. According to the datasheet, the LT1711 comparator can be operated with supply voltage of atleast +2,4 V. I have found that it functions with supply voltage as low as +1,9 V, but only with supply voltage of atleast +3 V was I able to achieve deadtime of 200 ns that was necessary to perform this measurement, as such that was the lowest supply voltage used. From graphs in Fig. 37, and especially in Fig. 37b, it can be seen that CW detector using the LT1711 comparator generally struggles with lower deadtimes. Overall this detector best performed with supply voltage of +7 V, but our standard CW detector doesn't have +7 V supply and so this setting cannot be used, as such I have concluded that for our application the LT1711 comparator is best to be operated at +5 V power supply.

		V_CC [V]:	7,0,	5,0	4,1	3,0
U_SPAD [V]	τ_{dead} [ns]		$f_{darkcount}$ [kHz]			
30,2	80		34	33,5	39	38
	110		27,5	28	28	29,5
	150		24	25	25	25,5
	200		23,5	22,5	24	24
30,7	80		128	204	183	185
	110		63	68	70	108
	150		46	47	47	63
	200		40	40	40	45
31,2	80		591	1000	1035	585
	110		165	200	308	470
	150		81	80	104	340
	200		62	65	66	194

Table 6. Table showing results of dark count measurement of the LT1711 test PCB, where U_SPAD (sometimes noted as V_a) is the voltage applied to the SPAD, τ_{dead} is the deadtime of the detector, V_CC is supply voltage and $f_{darkcount}$ is dark count frequency.



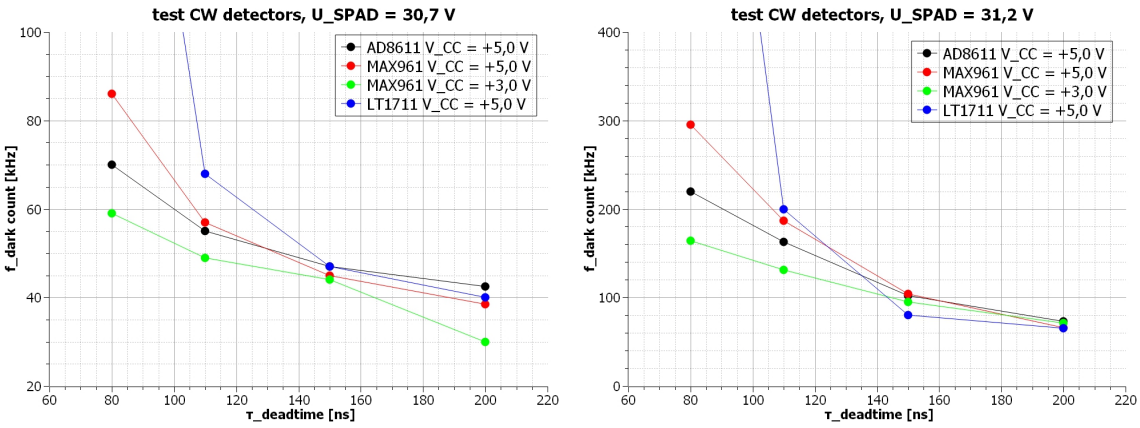
(a) U_SPAD = 29,2 + 1,5 = 30,7 V.

(b) U_SPAD = 29,2 + 2 = 31,2 V.

Figure 37. Graphs showing the results of dark count measurement of the LT1711 test PCB for different supply voltage V_CC, deadtimes τ_deadtime and bias voltage U_SPAD.

7.3.3 CW detector upgrade analysis

In Fig. 38 are the combined results of test CW detectors dark count measurements representing the best available performance for each test PCB, plus the addition of a MAX961 PCB operated at +5 V of supply voltage that represents performance of the current CW detector design. From these graphs it is obvious just how much the LT1711 comparator struggles at low deadtimes, but on the other hand its performance at longer deadtimes matches or even exceeds the current design. The AD8611 fares better at short deadtimes, but overall suffers from the same shortcoming. Surprisingly, powering the MAX961 comparator with only +3 V supply lead to the best results, which were cut above the rest over almost the entire range. Ultimately, it has been proven that none of the comparator candidates proposed in Chapter 7.1 are suitable, but we have come to the conclusion that simply powering the current comparator, the MAX961, with lower voltage supply will lead to an improvement in performance.



(a) U_SPAD = 29,2 + 1,5 = 30,7 V.

(b) U_SPAD = 29,2 + 2 = 31,2 V.

Figure 38. Graphs showing the best results of dark count measurement for each test PCB, plus the results for the current CW detector design.

Summary

This master thesis dealt with study of semiconductor single photon detectors and their optimization through several methods. At the core of this thesis is a detector that is being developed on the grounds of CTU FNSPE for the European Laser Timing, which is a project of the European Space Agency that sets out to facilitate transmission of time information from the atomic clock aboard the ISS. The great precision achievable using these single photon detectors is the reason why they are fit even for such demanding applications in space. The main undertaking defined in the assignment of this master thesis was to improve the detector propagation delay temperature stability and the detector's quenching speed. In follow up to the findings of my predecessors, the detector's comparator was replaced in an attempt to improve the temperature stability and afterwards we have reviewed several outdated or redundant parts in an effort to increase the quenching speed.

At the beginning of this thesis, I defined what single photon counting is and what its main applications are, including a more detailed description of the involved ESA projects. Afterwards, I delved deeper into the semiconductor single photon detectors from CTU FNSPE and their main components, the single photon avalanche diode and the electric control circuit. The next section of the text was focused on compensation techniques used to counter the instabilities brought about by changes in the detector's temperature. Following that was a brief introduction into the theory of comparators and a detailed description of the comparator's role in the detector. Subsequently, I have reported information about the various comparators used or considered for use in the single photon detector, including a new candidate, the ADCMP573 comparator. I have described the way in which this new comparator was implemented into the existing detector design, as well as the structure of the final integrated detector package, which I have come to call SPAD TE1 v0.2.

The fifth chapter covers the temperature stability measurements performed with this new detector package. First, I have established the detector's bias voltage temperature drift and its dependency on the settings of the temperature compensation, this dependency is shown in Fig. 21 and it can later be used to further improve the detector's temperature stability. Subsequently, by performing a time correlated single photon counting experiment, which I have set up at the CTU FNSPE, I have measured the propagation delay temperature stability of the new detector package, one of the detector characteristics that lies at the core of this thesis. The new detector package has distinctly linear propagation delay temperature dependency with growth coefficient of 0,14 $\pm$ 0,01 ps/K. This means that I have successfully confirmed the feasibility of using the ADCMP573 comparator inside the detector's control circuit to attain improved temperature stability.

In sixth chapter I have debated the options for achieving an increase in the detector's quenching speed. The first option examined the modification or removal of two voltage dividers in the control circuit. I have tested several iterations of modifications and ultimately decided to replace the voltage dividers with 50 Ω serial connections which lead to a 25% decrease in output pulse width without compromising other detection characteristics. The second option dwelled in reviewing the integrated circuits used in the control circuit and their possible replacement for modern counterparts, but in the end we haven't found any success in this venture.

The final chapter went beyond the master thesis assignment as I have decided to further my research with continuously operated single photon detectors. This kind of detector is developed at CTU FNSPE for the expected application in quantum communications, which poses considerable requirements on low detection noise levels. We have attempted to find a more suitable comparator for use in this detector and so I have proposed three possible candidates and built separate detectors for each of them to test their capabilities. Dark count measurements were used to compare the test CW detectors, the results of which can be seen in Fig. 38. Ultimately, these experiments have shown that none of the proposed candidates surpass the current detector design. However, I have found out that by operating the current CW detector at a lower supply voltage, it is still possible to further lower the noise levels.

Conclusion

I've studied the semiconductor single photon detector and its control circuit. I designed and implemented a comparator change in the detector circuit, which lead to improvement in the detector's temperature stability. The detector's propagation delay dependency on temperature is now linear with growth coefficient of 0,14 $\pm$ 0,01 ps/K with room for further improvement using temperature compensation techniques. By reviewing the detector design I achieved increase in quenching speed which lead to the shortening of output pulse by 25% and to a reduction in number of components. I tested several comparator changes in the continuously operated single photon detector and ultimately achieved decrease in the detector's dark count.

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Attachments

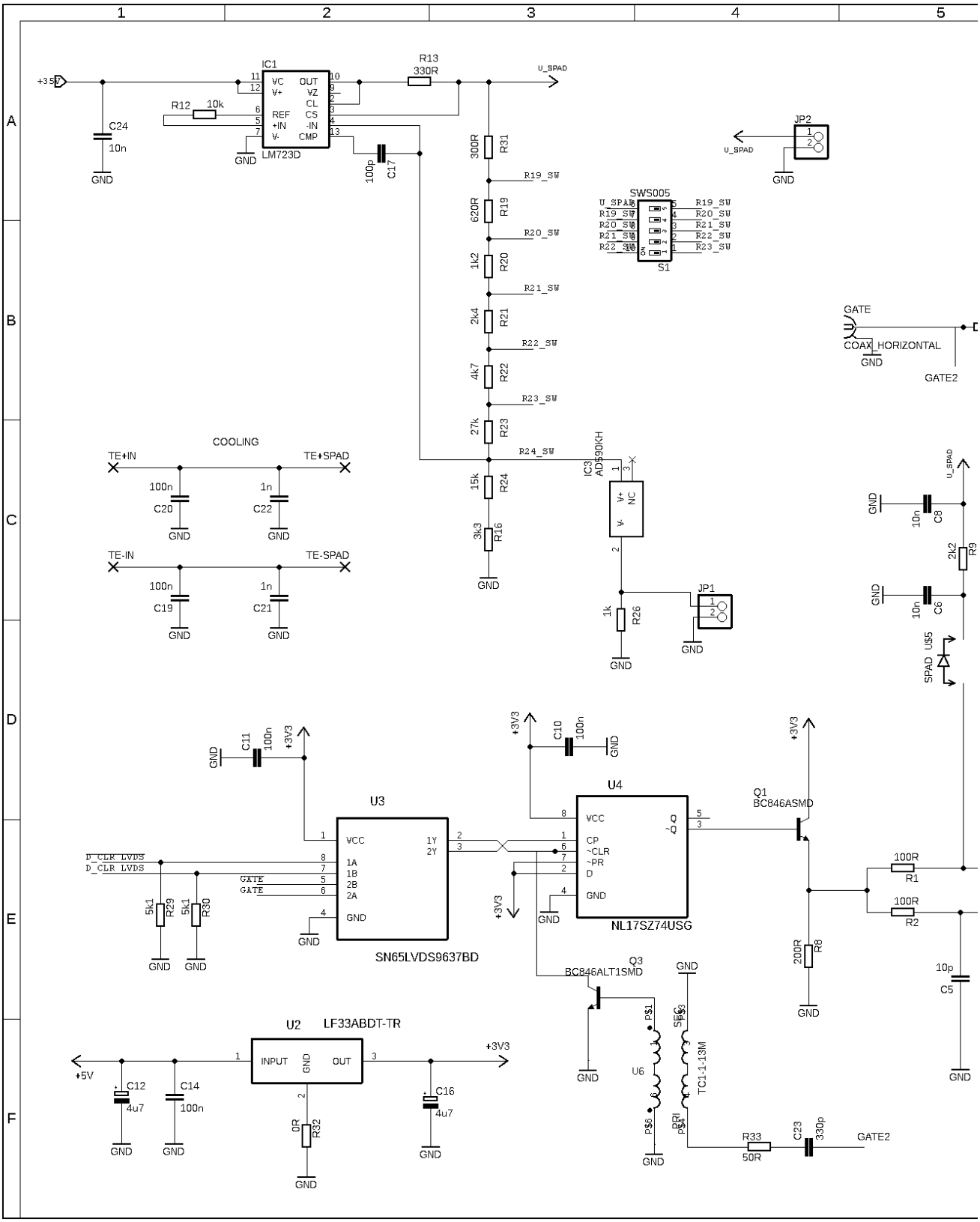

Figure 39. Scheme of the single photon detector containing the ADCMP573 comparator, part 1.

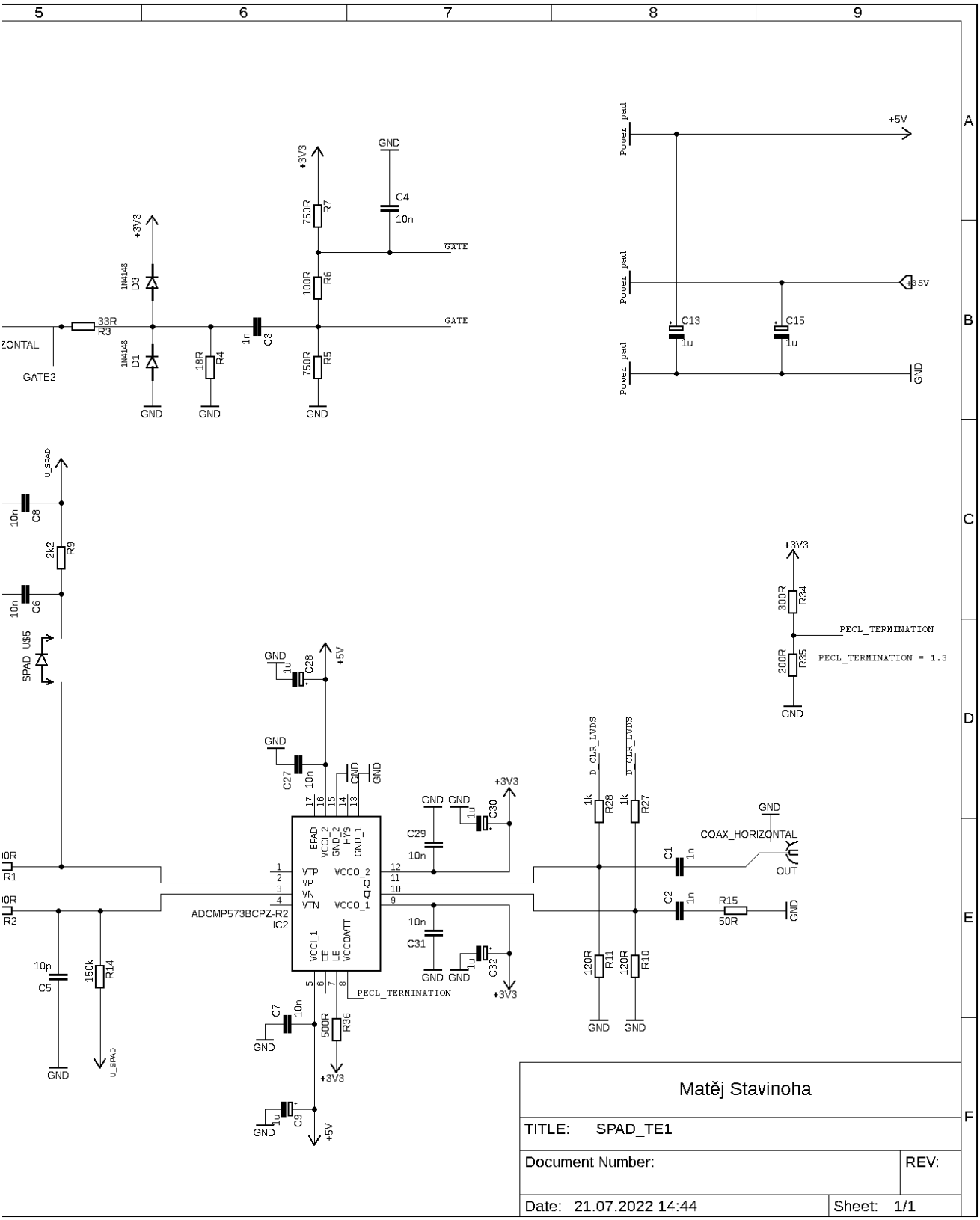

Figure 40. Scheme of the single photon detector containing the ADCMP573 comparator, part 2.

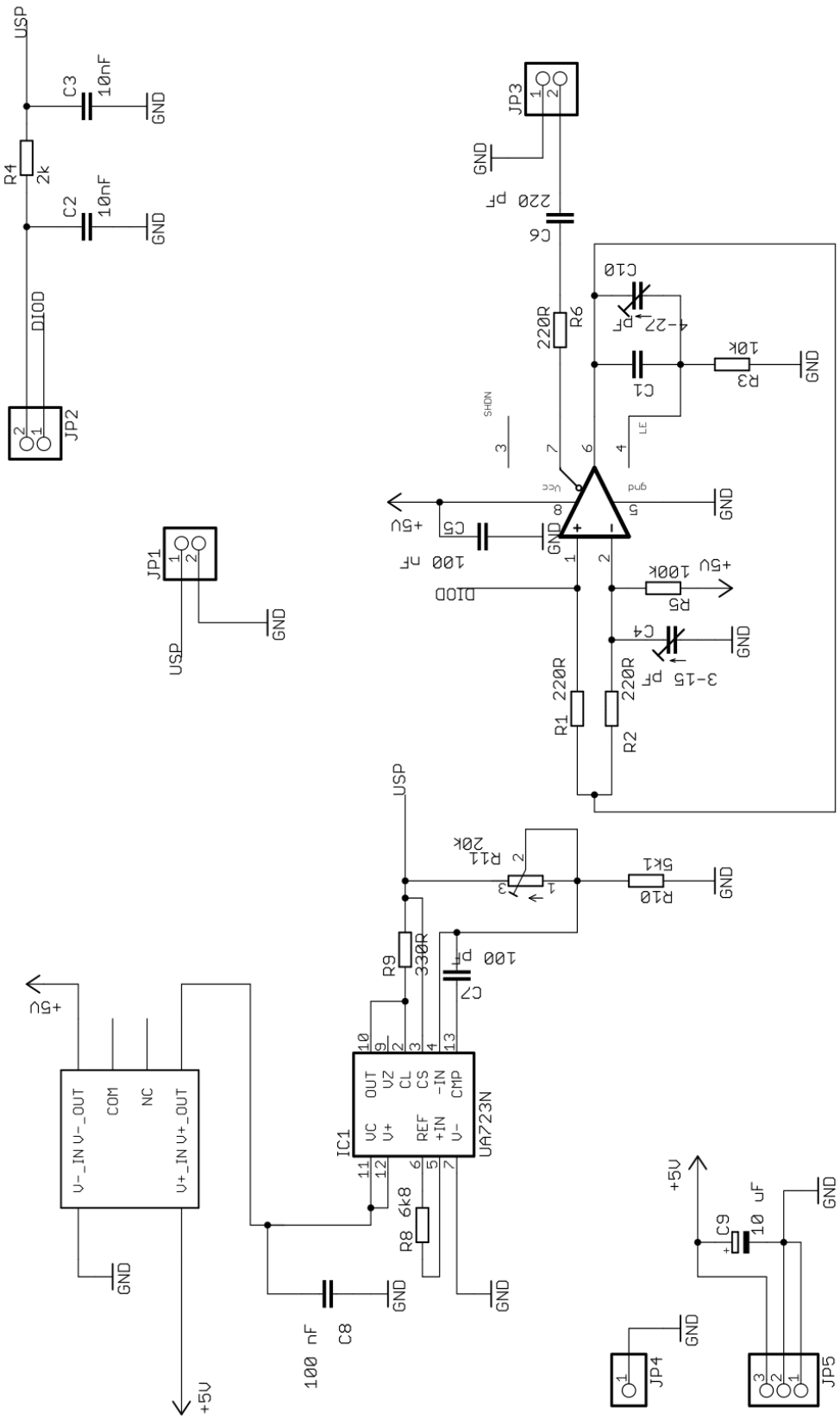

Figure 41. Current scheme of the continuously operated single photon detector.

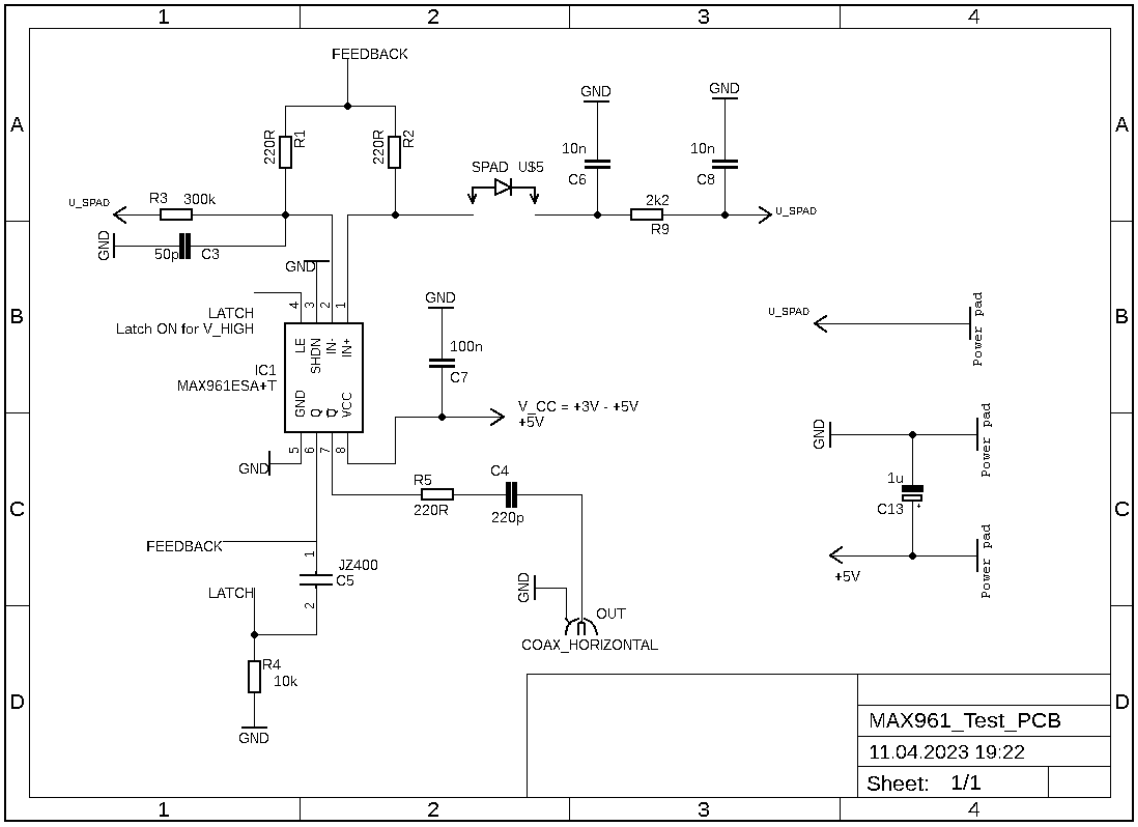

Figure 42. Scheme of the MAX961 test PCB.

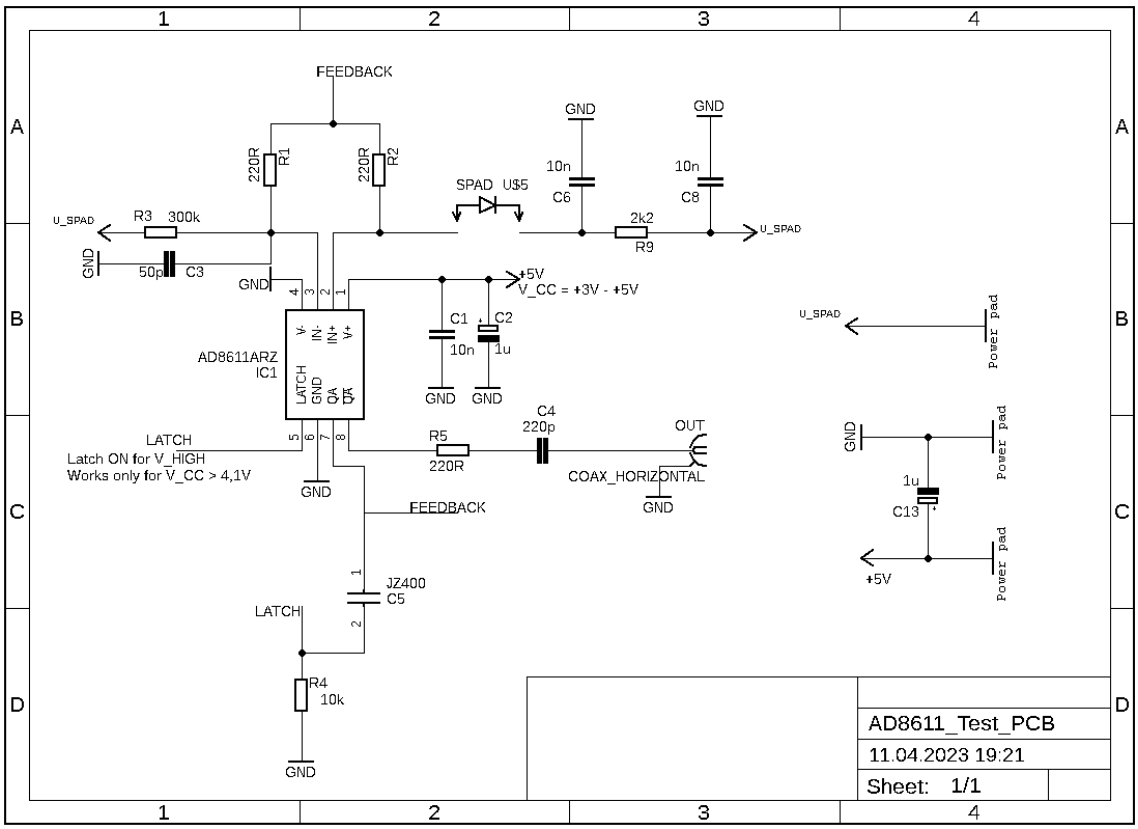

Figure 43. Scheme of the AD8611 test PCB.

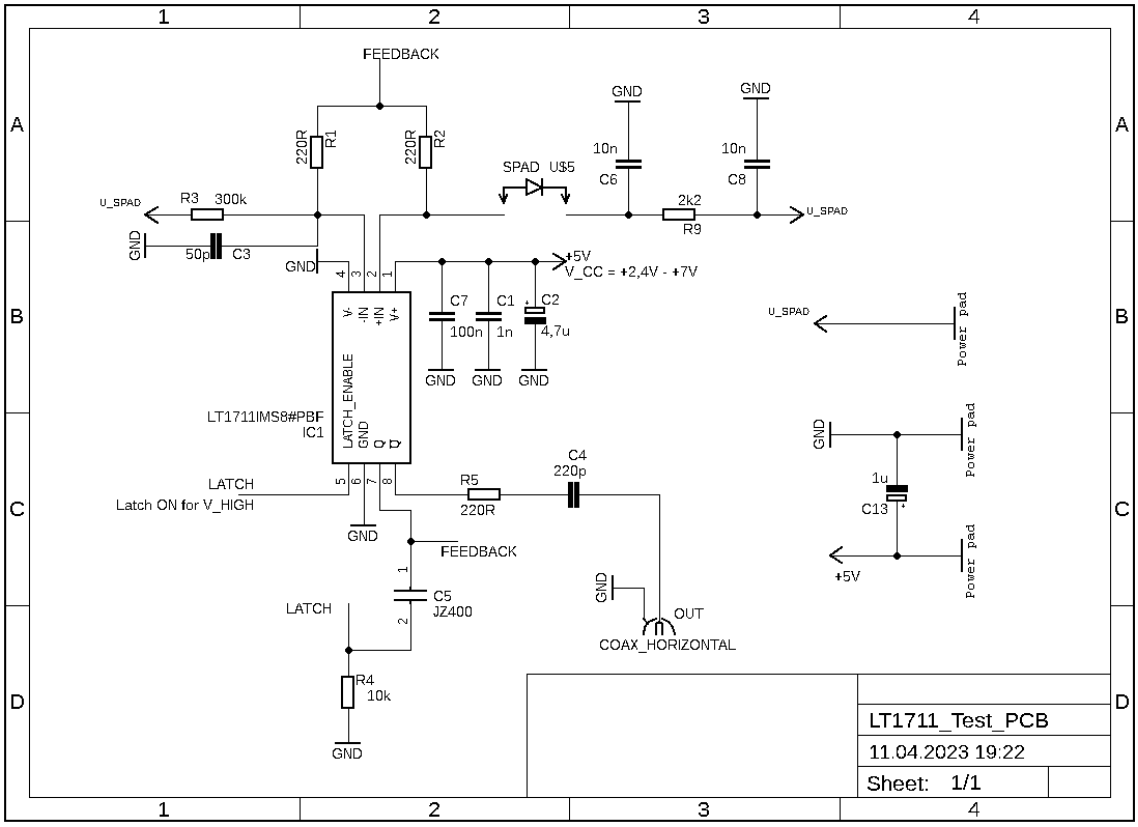

Figure 44. Scheme of the LT1711 test PCB.

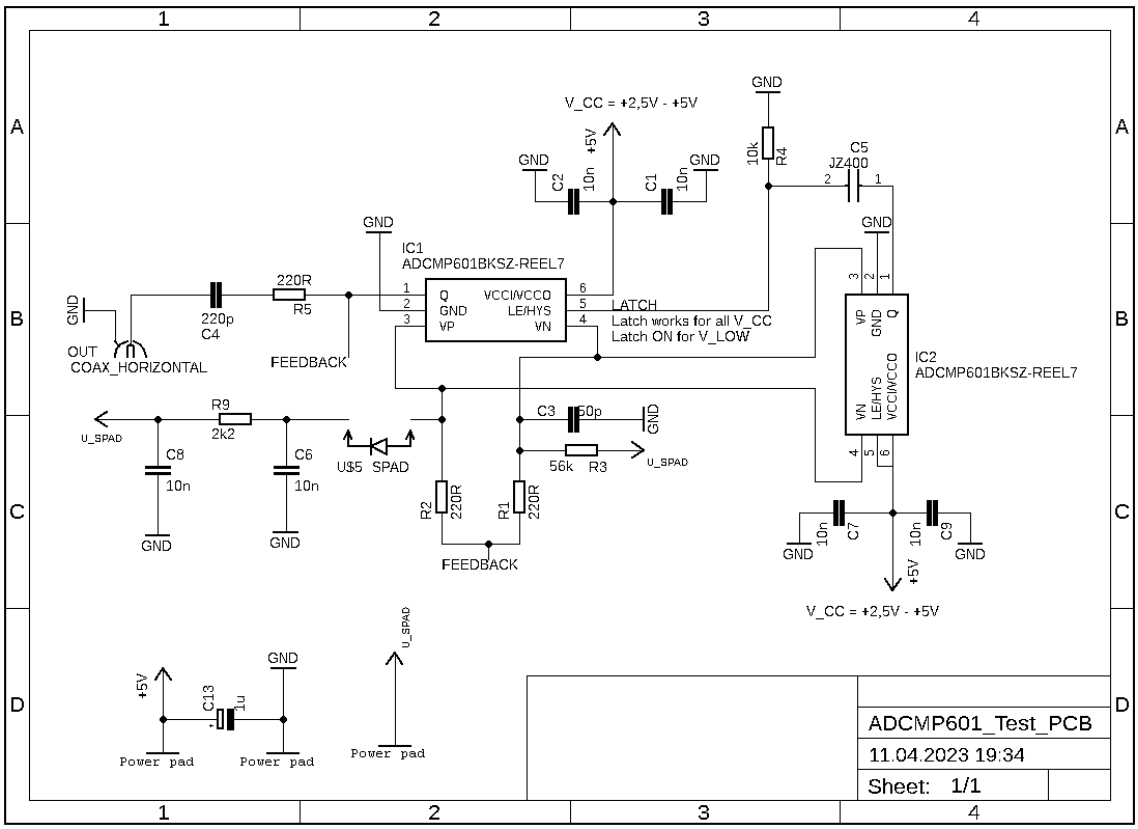

Figure 45. Scheme of the ADCMP601 test PCB.