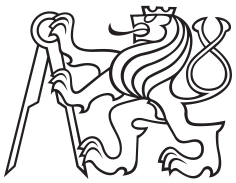
Master Thesis



Czech Technical University in Prague

F3

Faculty of Electrical Engineering
Department of microelectronics

Design of Readout System for Silicon Photomultipliers

Bc. Antonín Zeman

Supervisor: Ing. Jakub Jirsa
Field of study: Electronics and communications
Subfield: Electronics
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ZADÁNÍ DIPLOMOVÉ PRÁCE

I. OSOBNÍ A STUDIJNÍ ÚDAJE

Příjmení: **Zeman** Jméno: **Antonín** Osobní číslo: **474261**

Fakulta/ústav: **Fakulta elektrotechnická**

Zadávající katedra/ústav: **Katedra mikroelektroniky**

Studijní program: **Elektronika a komunikace**

Specializace: **Elektronika**

II. ÚDAJE K DIPLOMOVÉ PRÁCI

Název diplomové práce:

Návrh vyčítacího systému pro křemíkové fotonásobiče

Název diplomové práce anglicky:

Design of Readout System for Silicon Photomultipliers

Pokyny pro vypracování:

1. Seznamte se s detekčním principem křemíkových fotonásobičů (SiPM)
2. Prostudujte a vytvořte elektrický model SiPM AFBR-S4K33C0125B
3. Navrhněte analogový zesilovač pro křemíkových fotonásobič a simulujte s náhradním elektrickým modelem SiPM
4. Navrhněte základovou desku pro SiPM AFBR-S4K33C0125B s ADC a rychlým LVDS připojením k hradlovému poli Spartan-6
5. V jazyce Verilog2001 implementujte vyčítací systém, který bude přijímat data z ADC a následně je bude posílat přes rozhraní USB 3.0 do počítače.
6. V jazyce C++ vytvořte jednoduchou aplikaci, která umožní data ukládat do souboru.
7. Zhodnoťte dosažené výsledky.

Seznam doporučené literatury:

[1] Broadcom data sheet AFBR-S4K33C0125B
[2] Stefan Gundacker The silicon photomultiplier: fundamentals and applications of a modern solid-state photon detector

Jméno a pracoviště vedoucí(ho) diplomové práce:

Ing. Jakub Jirsa katedra mikroelektroniky FEL

Jméno a pracoviště druhé(ho) vedoucí(ho) nebo konzultanta(ky) diplomové práce:

Datum zadání diplomové práce: **25.08.2022** Termín odevzdání diplomové práce: **10.01.2023**

Platnost zadání diplomové práce: **19.02.2024**

Ing. Jakub Jirsa	prof. Ing. Pavel Hazdra, CSc.	prof. Mgr. Petr Páta, Ph.D.
podpis vedoucí(ho) práce	podpis vedoucí(ho) ústavu/katedry	podpis děkana(ky)

III. PŘEVZETÍ ZADÁNÍ

Diplomant bere na vědomí, že je povinen vypracovat diplomovou práci samostatně, bez cizí pomoci, s výjimkou poskytnutých konzultací. Seznam použité literatury, jiných pramenů a jmen konzultantů je třeba uvést v diplomové práci.

. _____
Datum převzetí zadání

_____
Podpis studenta

Acknowledgements

I want to express my gratitude to Ing. Jakub Jirsa. Without his insight and help, I would not have been able to complete this thesis.

Declaration

"I declare that I completed the presented thesis independently and that all used sources are quoted in accordance with the Methodological instructions that cover the ethical principles for writing an academic thesis."

Prague, 5. Ledna 2023

„Prohlašuji, že jsem předloženou práci vypracoval samostatně a že jsem uvedl veškeré použité informační zdroje v souladu s Metodickým pokynem o dodržování etických principů při přípravě vysokoškolských závěrečných prací.“

V Praze, 5. Ledna 2023

Abstract

This diploma thesis focuses on the development of a silicon photo-multiplier readout system. In the first part of this work, a detailed working principle of silicon photomultipliers is explored together with the introduction of their equivalent circuit model. With this complete equivalent model, an amplifier chain for the silicon photo-multiplier is simulated. The next part is dedicated to a PCB design that incorporates the analog part of the readout system followed by fast ADC. Firmware development for FPGA readout board and the description of the PC application written in C++ follow. Subsequently, measurements using a prototype of this readout system are carried out with a radiation source Plutonium 238 in combination with a scintillating crystal. In the last part, the measured results are presented and discussed.

Keywords: Readout system, Silicon photomultiplier, FPGA, FTDI

Supervisor: Ing. Jakub Jirsa

Abstrakt

Tato diplomová práce je zaměřena na vývoj vyčítacího systému pro křemíkové fotonásobiče. Na začátku této práce bude prozkoumán princip činnosti křemíkových fotonásobičů spolu s představením jejich ekvivalentního elektrického modelu. S tímto modelem je simulován zesilovací řetězec pro výstupní signál křemíkového fotonásobiče. Další část práce je věnována návrhu desky plošných spojů, na které je umístěna celá analogovou část vyčítacího systému s rychlým analogově digitálním převodníkem. Následuje vývoj firmwaru pro desku s FPGA a popis PC aplikace napsané v jazyce C++. Následně jsou provedena měření pomocí prototypu tohoto vyčítacího systému se zdrojem záření Plutonium 238 v kombinaci se scintilačním krystalem. V poslední části jsou prezentovány a diskutovány naměřené výsledky.

Klíčová slova: Vyčítací systém, Křemíkové fotonásobiče, FPGA, FTDI

Překlad názvu: Návrh vyčítacího systému pro křemíkové fotonásobiče

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Chapter 1

Introduction

Photon detection dates back almost a century to the invention of the photomultiplier tube (PMT). This device was invented in the year 1930 by the Soviet physicist L.A. Kubetsky [1]. The PMTs allowed for light current amplification and marked the beginning of this field of research.

In today's world, silicon photomultipliers (SiPMs) are becoming the device of choice for detecting single or multiple incoming photons. SiPMs are used in applications such as distance measurements (LIDAR) or positron emission tomography (TOF-PET). Their ability to detect incoming photons with precise timing allows for calculating the photon's time of flight or distance traveled. To fully utilize the exceptional performance of SiPMs, they have to be paired with high-speed electronics and readout systems. Such a readout system is the topic of this diploma thesis.

The opening chapter presents a brief overview of the complete readout system. The second chapter is dedicated to the exploration of SiPM's working principles. SiPMs are constructed from an array of single photon avalanche diodes (SPADs). Because of this, SPADs are described at first. This chapter is afterwards concluded by presenting an equivalent circuit of a SiPM. With this equivalent circuit, an analog amplifier chain is designed and simulated. The amplifier chain consists of a transimpedance amplifier and a differential driver as the second stage. A four-layer PCB that houses the complete analog chain and an analog-to-digital converter (ADC) is designed.

For the reassembly of the measured data samples, an FPGA SPARTAN-6 is used. This FPGA is placed on a second PCB that is connected to the first one with a serial low voltage differential signal (LVDS) interface. The data is reassembled within the FPGA using the input double data rate (IDDR) logic block. The data transfer to the PC program is realized via a high-speed FTDI interface. Here The data is saved into a binary file format.

The final chapter is dedicated to measurements on a prototype of the SiPM readout system. The proper function of the readout system is verified by capturing the specific SiPM pulses using the readout system. These pulses

are also at the same time captured at the end of the amplifier chain using a differential probe. Lastly, a long time period capturing of SiPM pulses is carried out. Measurement with a radiation source present at the SiPM is compared to a measurement of the background noise.

Chapter 2

Readout system overview

This chapter describes the architecture of the complete readout system. The following chapters are dedicated to the detailed description of individual functional blocks. The schematic diagram of the readout system is depicted in figure 2.1. The SiPM readout board contains four SiPM detectors connected to a four-channel ADC. This board is then connected to the FPGA board via 10 pair LVDS interface. Besides the FPGA, the second board also contains the FT 601 integrated chip. This IC provides high-speed communication with PC over USB 3.1.

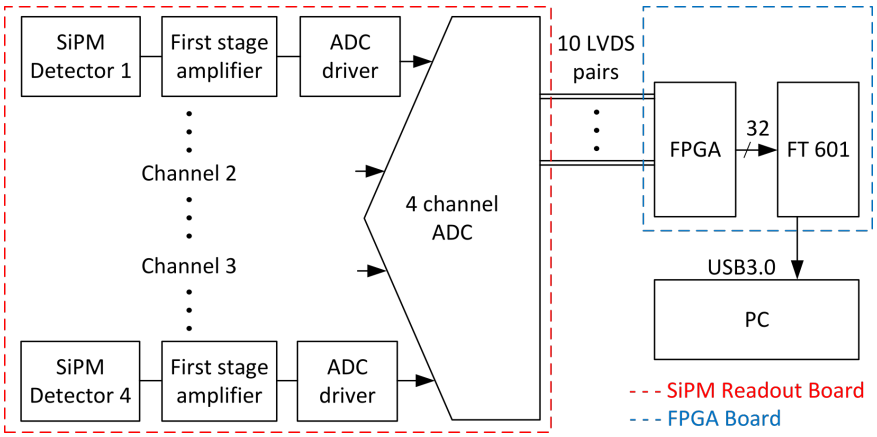

Figure 2.1: Readout system architectural diagram

In figure 2.1, all functional blocks until the FPGA board are integrated within the SiPM readout board. Each SiPM detector is connected to a two-stage amplifier. The first stage consists of a transimpedance amplifier and is used for signal amplification. The second stage amplifier serves as a differential driver for ADC input. Although the second stage is capable of further amplifying the signal, the gain of this stage was set to 1. These analog channels come together in the ADC. Here analog signal is sampled and continues further as discrete digital data samples.

FPGA board is in the second place in the architectural diagram in figure 2.1. The interface between the boards consists of 10 LVDS pairs because analog

data from each SiPM is split into two of them. The remaining two pairs carry clocking signals. Because the data is serialized into two channels, it has to be deserialized within the FPGA logic. After the data is assembled into individual samples, it can be sent to the PC program.

The FT 601 chip serves as a FIFO bridge over USB 3.1 [24]. It provides a solution for transferring high-speed data with minimal complexity. This communication is controlled within the PC program using a dynamically linked library provided by the chip's manufacturer. The program itself consists of an object-oriented C++ program. It provides a basic user interface and debug capabilities. As its main function, it saves received data into a binary file. Data obtained this way is ready for further analysis and use. In this thesis, this is demonstrated by calling external higher language script for signal processing and display.

Chapter 3

Silicon photo-multipliers

The entire topic of this diploma thesis is centered around SiPMs and data acquisition from these sensors. Therefore the SiPM functionality will be described in detail first. SiPMs are sensors capable of single photon particle detection. SiPMs have this ability because they are constructed from single-photon avalanche diodes (SPAD). This can be easily illustrated using a picture of an actual SiPM's surface. The left side of Figure 3.1 depicts SiPM's physical structure, and in the detailed section on the right, one can notice individual rectangular SPADs. These special PN junction diodes effectively act as pixels in a large array. This array altogether creates a single SiPM sensor. In figure 3.1, there is also highlighted that each SPAD has a resistive element connected to it. These resistances act as avalanche-quenching resistors. This will be further described in the following sections of this chapter.

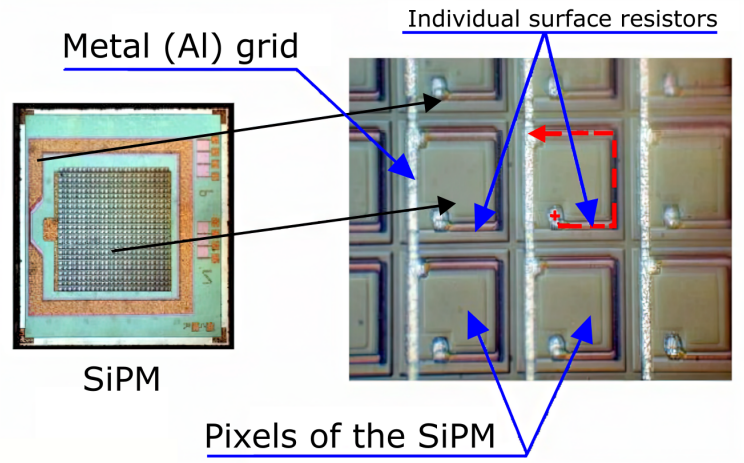

Figure 3.1: SiPM physical structure [3]

Because SPADs are the foundation on which the SiPMs are constructed, the first section of this chapter will be dedicated to their detailed description and characteristics. After that, a simplified electrical model of a singular SPAD will be introduced. When an understanding of SPAD's working principle is established, the complete SiPM structure can be examined. SiPMs inherit

most of their characteristics from SPADs as they are a large array of them. However, SiPMs introduce a structure in which SPADs are connected, and this also greatly influences their output signal and characteristics.

3.1 Single photon avalanche diode

Essentially, SPADs are not significantly different from standard photodiodes, and also their I-V characteristic is very similar. The main difference is that SPAD is constructed to be regularly used above its reverse breakdown voltage. The electric field at this point reaches a value higher than $3 \cdot 10^5$ V/cm, and that enables a single charge carrier in the depletion region to trigger a self-sustaining avalanche [4]. As visualized in figure 3.4, SPADs are capable of working in this region by introducing quenching.

3.1.1 Modes of operation

SPADs can operate in 3 regimes:

1. Photodiode mode
2. Avalanche photodiode mode
3. Geiger mode

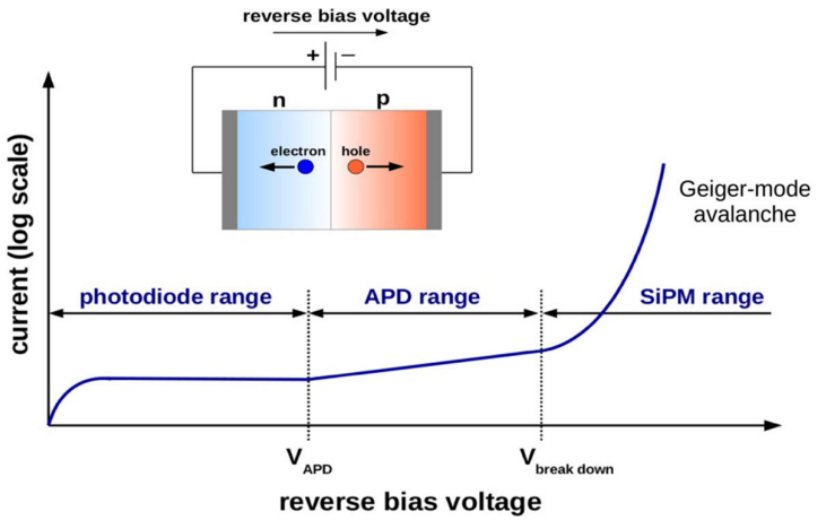

Figure 3.2: Ranges of operation of a SiPM [2]

In figure 3.2, the first regime is called the photodiode mode. SPAD requires a very low reverse bias voltage to enter this regime of operation. Here, the incoming photons are capable of creating an electron-hole pair. These current carriers then drift towards the terminals of SPAD accelerated by the electrical field, which is present in the depletion region due to the reverse voltage bias.

Although the electrical field is present, it is too weak to provide enough energy to the moving electrons and holes to create secondary electron-hole pairs via impact ionization [2]. As a consequence of this, no amplification of the incoming signal occurs. Output current becomes proportional to the light intensity present at the semiconductor's surface. SPADs are usually not used in this region as standard photo-diodes offer much more cost-effective solutions for these applications. However, thanks to this capability, SiPMs can offer a much wider range of conditions under which they can operate. This characteristic may be used for example in applications where a large disparity in incoming light is expected.

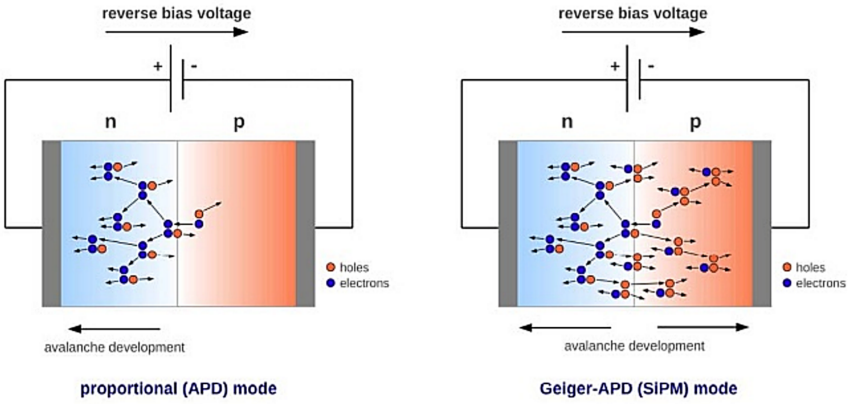

Figure 3.3: SiPM avalanche propagation [2]

The second mode is called the avalanche photodiode mode (APD). If the reverse voltage is raised above V_{APD} level, see fig. 3.2, the electrons freed up by impacting photons in the depletion region are accelerated by a much stronger electrical field. As an effect of this, the accelerated electrons gain high momentum. It enables them to create secondary electron-hole pairs upon impact with the silicon crystal [4]. Under reverse voltage in this range, holes cannot create secondary current carriers due to their higher effective mass. The secondary electron-hole pairs trigger avalanche discharge that only travels in the direction towards the n-doped cathode. This is illustrated in the left part of figure 3.3. The unidirectional avalanche eventually quenches itself. No extra circuitry for the diode's protection is necessary. Another consequence of this unidirectional propagation is relatively low amplification. The secondary induced e-h pairs offer a gain of ten to around a hundred. The current present at SPAD's terminals is still proportional to the number of incoming photons [2].

As illustrated in figure 3.2, if we keep increasing the voltage above the breakdown level V_{BD}, we enter the Geiger mode of operation. In this region, even holes gain the ability to create secondary e-h pairs when traversing the depletion region. This is caused by the very strong electrical field. The holes also gain enough energy to free up current carriers [2]. This in turn, causes

the avalanche to travel in both directions and effectively short the terminals of a SPAD. To conclude, a single photon impact gains the ability to create a self-sustaining avalanche. During this self-sustaining avalanche occurrence, the current through the diode rises very rapidly, and it has to be quenched to prevent the diode's thermal destruction. This quenching is assured by lowering the external reverse bias voltage to or below the breakdown level by using external circuitry. After the avalanche is successfully quenched, the biasing voltage has to be brought back above the breakdown level to allow for the detection of another incoming photon.

The gain achieved in Geiger mode is roughly around the order of 10^6 and can be determined by the following equation:

$$Gain = \frac{Q_{avalanche}}{q} = \frac{V_{ov} \cdot (C_q + C_d)}{q} \text{ [2].} \tag{3.1}$$

In this equation, q denotes the elementary charge of $1.602 \cdot 10^{-19}$ C, and the $Q_{avalanche}$ stands for the charge freed up by an avalanche occurrence. V_{ov} stands for excess overvoltage by which the internal SPAD capacitance C_d is discharged. C_q is the capacitance present in SPAD's quenching circuit. This capacitance enables the fast signal to cross the quenching resistance and reach the SPAD's terminals [2]. All of the component variables mentioned above can be seen in the SPAD's equivalent electrical circuit in figure 3.10.

3.1.2 Simplified working principle

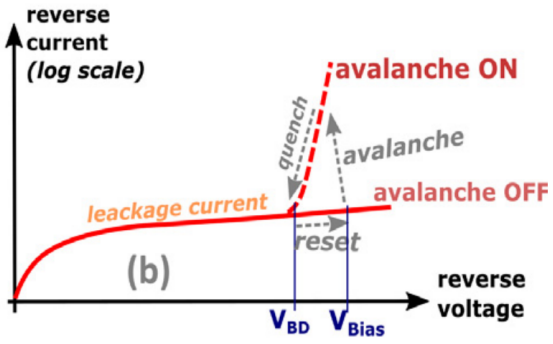

Figure 3.4: SPAD Current-Voltage characteristic [5]

Since SPADs are almost exclusively used in Geiger mode and so their operation in this region will be explained in detail. The working principle of SPAD can be better illustrated by its I-V characteristic in figure 3.4. During its standard operation, SPAD's operating point travels around the triangle marked by arrows in the counterclockwise direction.

SPAD's operation begins with the operating point at the intersection with breakdown voltage V_{BD}. The reverse voltage is slowly brought above this

point to the chosen level of V_{bias}. The leakage current still does not rise significantly. At this point, the incoming photon particle triggers an avalanche discharge, and the reverse current through SPAD exponentially increases. This creates a large current spike on the SPAD's terminals. The operating point moves up along the avalanche arrow. At this moment, maximal current flows through the SPAD and must be quickly returned to safe levels. This is achieved due to the quenching circuit that brings down the reverse voltage to or below the breakdown voltage V_{BD} [5]. Consequently, the operating point moves again to the intersection of V_{BD} and SPAD's characteristic curve. At this point, it has completed a revolution around the triangle in which one impacting photon was detected.

3.1.3 SPAD structure

Now with an understanding of SPAD's working principle in the Geiger mode, it is possible to explore the possible physical construction of basic types of SPADs.

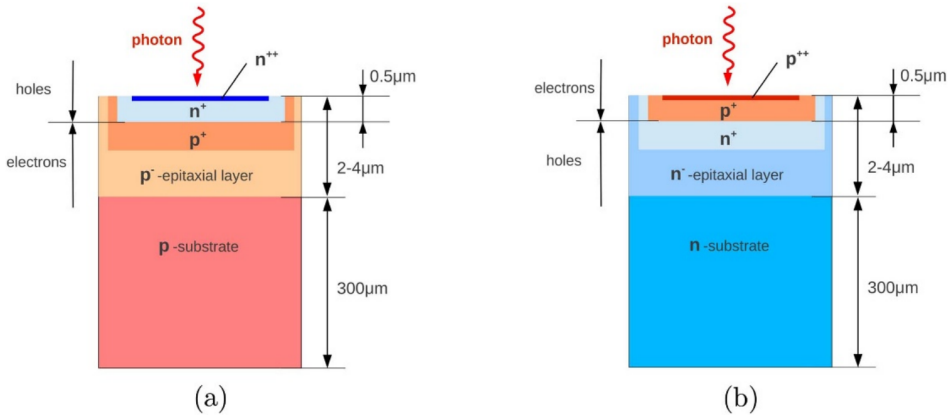

Figure 3.5: **(a)** N-on-P SPAD structure, **(b)** P-on-N SPAD structure [2]

There are two possible SPAD configurations: N-on-P and P-on-N. These configurations are displayed in figure 3.5. Choosing the configuration mainly depends on the absorption length of light of different wavelengths. As shown in figure 3.6, the light of shorter wavelengths is absorbed closer to the silicon surface, where it can generate a pair of current carriers (electron-hole pair). Due to the SPAD's PN junction being biased by voltage in the reverse direction, the electrons always travel in the direction of the strongly n-doped cathode. As established by Oldham et al. in 1972, the avalanche-triggering probability is significantly higher for electrons than for holes [6]. Therefore, in general, it is desirable to maximize the travel distance of generated current-carrying electrons in the SPAD active region. This way, we maximize the probability of the electron creating secondary e-h pairs via impact ionization [2]. And this way it is possible to maximize the probability of triggering an

avalanche discharge.

It is possible to use this knowledge to determine which SPAD structure is advantageous for the detection of photons of a given wavelength. To illustrate this in a particular example: if it is desired to detect the impact of photons of shorter wavelengths (for example, visible blue light), it is better to use the P-on-N structure. This is because the depth to which the incoming photons penetrate silicon is only in the range of tens of nanometers, see figure 3.6. This way the primary electron generated by impacting photon travels deep into the silicon to the n-doped cathode. Therefore it has a much longer trajectory through the depletion region of SPAD. This in turn, provides a higher chance of interacting with the crystal [2] and triggering an avalanche discharge.

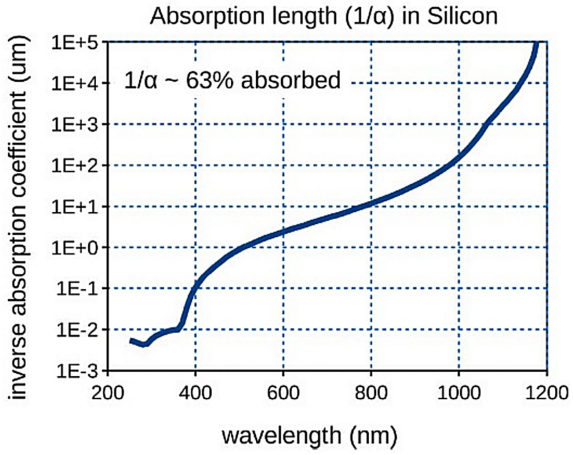

Figure 3.6: Light absorption length in silicon [2]

In contrast, the flipped structure becomes advantageous if the target wavelengths are significantly longer. For example, wavelengths at or above 600 nm. According to figure 3.6, photons of this wavelength have absorption lengths already in the order of single micrometers. Incoming photons penetrate deep in silicon, and thus the created electron will travel a longer trajectory if the n-doped terminal is located at the surface.

3.1.4 SPAD characteristics

SPADs are characterized by a set of specific parameters. These parameters describe the SPAD's performance when it comes to detecting incoming photons, signal amplification, and last but not least, their noise characteristics. All of these will be explored within this section.

Photon detection efficiency (PDE)

For a SPAD to detect photons, it has to be absorbed in the detector's active region (depletion region) and generate an electron-hole pair. On top of that,

the electron-hole pair must trigger an avalanche. These events are probabilistic, and their compound is called photon detection efficiency (PDE). Since the triggering probability can be improved by higher overvoltage at SPAD's terminals, the PDE can also be improved this way. This is illustrated in figure 3.7. It is possible to notice that raising overvoltage above 5V does not significantly improve PDE anymore. This is caused by the fact that PDE is a compound probability, and increasing the strength of the electric field does not improve the chance of the photon impacting the SPAD's active region [8].

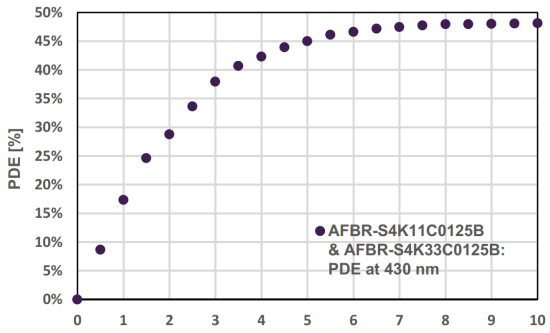

Figure 3.7: Photon detection efficiency in dependence on overvoltage[7]

Figures 3.7 and 3.8 are taken from the datasheet of SiPM that was used for the designed readout system [7]. Figure 3.8 contains PDE in dependence on wavelength. From this chart, it is apparent that SPADs integrated on this particular SiPM are of the P-on-N structure since PDE is the highest for wavelengths between 400 and 500 nm. The manufacturer does not provide this information in the part's datasheet [7].

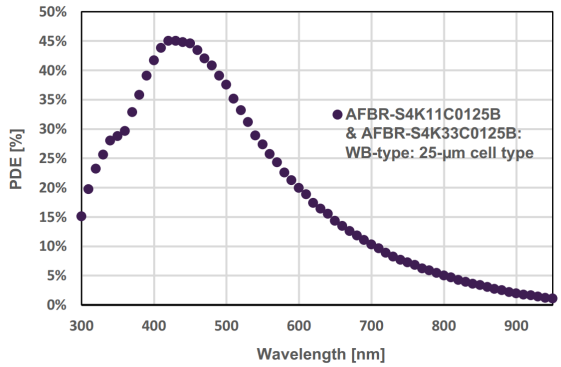

Figure 3.8: Photon detection efficiency in dependence on photon wavelength [7]

3.1.5 SPAD's internal noise: dark count rate and afterpulsing

The most crucial noise characteristics in SPADs significantly differ from other standard semiconductor devices. In this case, flicker and thermal noise don't concern us since they only play a marginal role. The prevalent noise sources in

SPADs can be divided into two main categories: primary pulses and secondary pulses [5]. These noise categories can be summed up into one characteristic called the dark count rate (DCR). Afterpulsing is another way of describing the secondary pulses and it is a compound of the DCR.

Dark count rate

In the depletion region, thermally generated carriers can trigger the avalanche discharge as well as the photon impact-induced ones. As a consequence, SPADs are triggered even in completely dark environments. The mean value of output pulses across a given unit of time is the DCR [4]. As stated before, the DCR includes primary and secondary pulses. The primary pulses are caused by thermally generated carriers triggering an avalanche discharge in the PN depletion region. This part of the dark count rate increases with rising ambient temperature the same way it does in standard photodiodes [8]. The dark count rate also increases significantly with rising overvoltage. This is due to increased avalanche-triggering probability, and enhancement of the emission rate from generation centers [8].

Afterpulsing

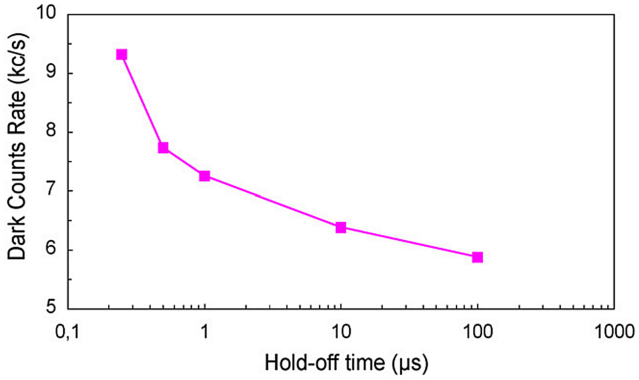

Figure 3.9: Influence of hold-off time on DCR [4].

A secondary source of noise is the so-called afterpulsing effect. It is caused by various crystal defects in the depletion region. These defects act as deep and shallow traps for carriers. They generally trap a carrier and release it with exponential time delay [2]. Said release can happen after overvoltage is returned to Geiger mode level. This released carrier can then trigger secondary avalanche discharge and thus cause unwanted noise on the output of the detector [4]. These afterpulses can greatly influence detector's DCR. The mitigation of this problem is illustrated in figure 3.9. It can be achieved by slower introduction of overvoltage to the SPAD. This unwanted behavior can also be optimized by minimizing the impurities of the crystal in the depletion region.

Afterpulsing can also be induced optically. During each avalanche, secondary photons are produced in the SPAD's active region, and these photons can be reabsorbed in the neutral region of the same SPAD. These carriers can afterwards diffuse into the active region with the strong electric field and trigger another avalanche [2].

3.1.6 Equivalent circuit of single SPAD

SPAD is in construction very similar to standard PN junction diode, and so is its equivalent circuit. Reversed biased PN junction diode is usually modeled as a parallel connection of its internal resistance and capacitance. In the equivalent schematic in figure 3.10, significant similarities can be noticed. In the schematic, the resistance R_d represents the SPAD's internal resistance through which current flows in the forward direction. The other branch represented by capacitance C_d is SPAD's internal capacitance. The energy here is stored in a strong electrical field in the depletion region [11].

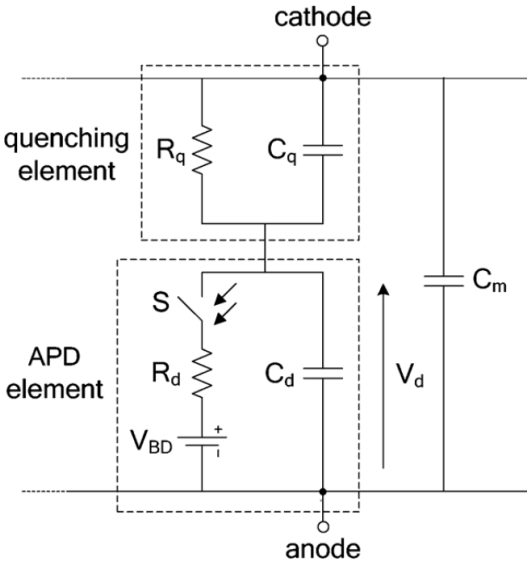

Figure 3.10: Single SPAD equivalent electrical circuit [10].

R_d is connected in series with voltage source V_{BD} and switch S_0. Voltage source V_{BD} represents the PN junction's breakdown voltage underneath which the voltage V_d does not fall. This is so because the avalanche is quenched when voltage descends to this level. Switch S_0 models an avalanche occurrence that is in the real semiconductor triggered by an incoming photon particle. This part of the equivalent circuit is in figure 3.10 labeled as an APD element [10].

The APD element is connected in series with a quenching element which consists of resistance R_q and parallel capacitance C_q. R_q in this configu-

ration represents the frequently mentioned quenching circuit. It is a weak current source of sorts, and if the current consumption of SPAD rapidly rises due to avalanche discharge, it assures the SPAD is not destroyed by the excessive current flow [10]. Capacitance C_q ensures the transfer of fast signals to SPAD's terminals [2]. Parasitic capacitance C_m across SPAD terminals is always present but does not significantly affect this circuit's behavior.

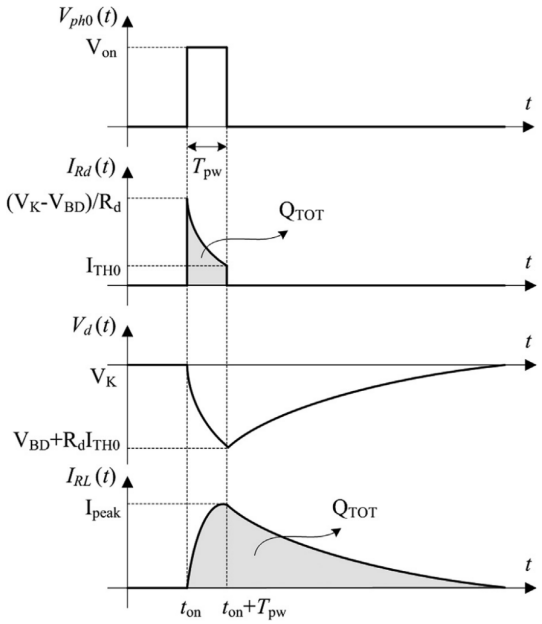

Figure 3.11: Transients of SPAD model during photon detection [12].

The operation principle for this simplest equivalent circuit is fairly straightforward. Overvoltage higher than V_{BD} is presented across SPAD's terminals: anode and cathode. At this stage, no significant current flows through the device. Transients of circuits voltages and currents are illustrated in figure 3.11. In the first transient graph, the closing of switch S_0 is represented by a step function. When voltage is brought to V_{on} level the switch S_0 closes. T_{pw} is the duration for which the switch S_0 stays closed.

The shorting of switch S_0 causes a rapid rise in current I_{Rd} flowing through resistance R_d from figure 3.10. This current is displayed as the second transient graph in figure 3.11. The current rises to the maximum peak that is given by the following equation

$$I_{Rd}(t_{on}) = \frac{V_K - V_{BD}}{R_d}. \tag{3.2}$$

Here V_K stands for the voltage present at the SPAD's terminals, V_{BD} the breakdown voltage from figure 3.10 and R_d the SPAD's internal resistance. The current flows through the resistor R_d for the duration of T_{pw}.

When the switch opens, the current is quenched. I_{TH0} is the threshold current at which the discharge can no longer sustain itself. If the current waveform is integrated across T_{pw}, it is possible to gain a value of Q_{TOT} which is the total charge released.

The third transient in the figure 3.11 represents the voltage drop across the SPAD cell falling while C_d is being discharged. Here the voltage drops to the sum of breakdown voltage V_{BD} and voltage created at the resistance R_d by the threshold current I_{TH0} which is flowing through it.

The last graph represents the current signal propagated to the SPAD's terminals. Here the current is represented as I_{RL} because it is a current flowing through loading resistance. This resistance is connected to the SPAD in series. It typically has a resistance value between 1 Ω and 50 Ω.

At the output signal in figure 3.11, it is important to notice that it can be simplified into two exponential transients. So it is possible to express the signal as a sum of two exponentials

$$V_{out} = \frac{Q}{C_q + C_d}\left(\frac{C_q}{C_d + C_q}e^{\frac{-t}{\tau_f}} + \frac{R_{load}}{R_q}\frac{C_d}{C_q + C_d}e^{\frac{-t}{\tau_s}}\right)[3]. \tag{3.3}$$

The Q denotes the total charge released by avalanche discharge and can be obtained from equation 3.1. τ_f is a time constant of the fast-rising exponential. It describes the discharge of capacity C_d through the resistor R_d and can be calculated as a time constant of a first-order system

$$\tau_f = R_d(C_d + C_q). \tag{3.4}$$

The second time constant τ_s describes the slow charge of capacitances that follow. It is given by a very similar equation

$$\tau_s = R_q(C_d + C_q), \tag{3.5}$$

where R_d is supplemented by R_q, which is usually two orders of magnitude higher, and therefore, the charging transient is much slower.

3.1.7 Improved equivalent circuit of single SPAD

An equivalent model of a single SPAD presented in figure 3.10 has one significant drawback. The timestep function in figure 3.11 controls the quenching of triggered discharge. Current flows as long as the switch S_0 is shorted. In reality, this is not the case. Avalanche in the PN junction stops flowing when the current flowing through the depletion region reaches its threshold value I_{TH0}, and the avalanche collapses due to a lack of sufficient generation of current carriers [12].

This behavior can be better modeled by introducing sensing of current that flows through resistor R_d. This sensing can be realized via a comparator

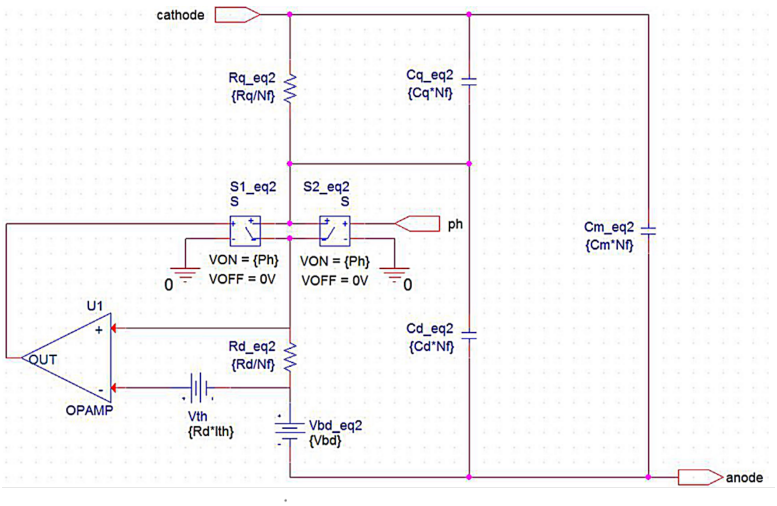

Figure 3.12: Equivalent model of SiPM used for simulation [12].

that senses the voltage across R_d and drives switch S_0. For simplicity of simulation, another switch, S_1, is introduced to act as an avalanche trigger and S_0 only turns off the discharge of C_d at a given current threshold value. This improved configuration can be seen as a part of the equivalent circuit in figure 3.12.

3.2 SiPM

Figure 3.13 depicts that SiPMs are semiconductor devices that are essentially a large array of SPADs. Consequently, they inherit all characteristics of SPADs that were discussed previously. SiPMs fall into two main categories depending on their quenching circuit: Digital SiPMs and Analog SiPMs.

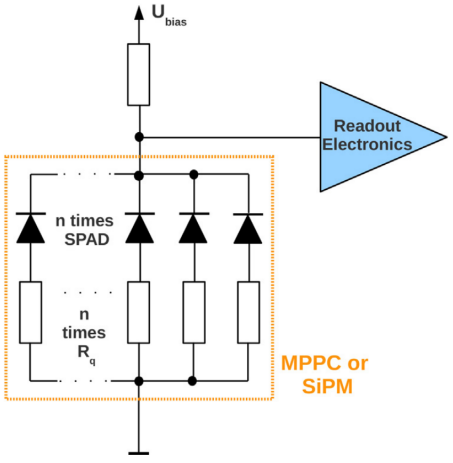

Figure 3.13: Simplified schematic of analog SiPM [13].

Figure 3.13 depicts a schematic of an analog SiPM. Digital SiPM differs in its terminal connections. Here the individual SPADs don't share a common cathode and anode, but each has its own connection for reading out signals. Thanks to this, digital SiPMs can identify which SPAD detected an incoming photon [13]. However, as the SiPM used in this thesis is analog, digital SiPMs will not be further discussed.

3.2.1 Analog SiPM output signal

All SPADs share a single cathode and anode in an analog SiPM. This means that analog SiPM cannot detect which SPAD in an array detected the incoming photon. On the other hand, it is still possible to detect several impacting photons simultaneously. To illustrate, in the last graph in the picture 3.11, the Q_{tot} denotes that the integral of the current output signal is equal to the charge released by a single avalanche [10]. So the number of impacting photons at one moment can be calculated from the total charge on the SiPM's output terminals by integrating [5].

3.2.2 Complete equivalent circuit of a SiPM

With comprehensive knowledge of SPADs and SiPM structure, it is possible to deduce that the complete equivalent circuit of a SiPM photodetector will be a set of SPAD equivalent circuits. This circuit of SPADs connected in parallel can be seen in figure 3.14. Here the SPADs are divided into active and passive cells.

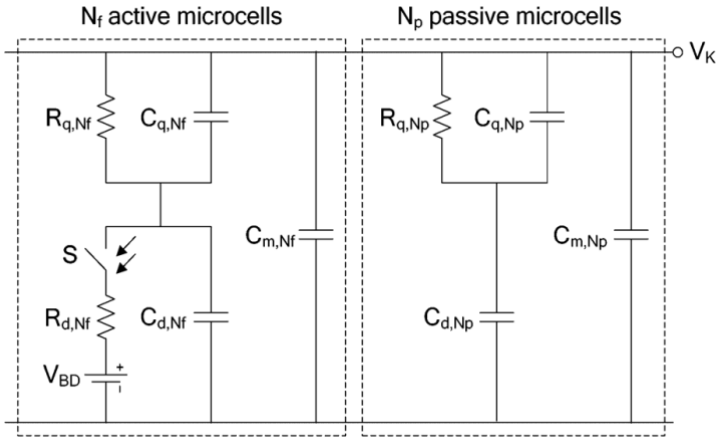

Figure 3.14: Equivalent model of SiPM [10].

A first part is a group of cells currently undergoing avalanche discharge. The number of these cells is N_f. This group of cells is in figure 3.14 described as N_f active microcells. These cells are to be modeled as complete SPAD equivalent circuits. The second part is made out of currently passive cells.

The number of these cells is represented by N_p. Model circuits of these can be simplified by removing SPAD's branch containing resistance R_d and voltage source V_bd because switch S_0 is constantly open [10].

It is possible to greatly simplify the complete schematic further by removing the quenching resistance R_q from the passive SPAD cells. We can do this under the assumption that

$$R_L << R_q, \tag{3.6}$$

where R_L stands for loading resistance that is connected to the SiPM. This assumption will hold because the transimpedance amplifier that was used has minimum input impedance. After resistance, R_q is removed, all the passive cells can be modeled as a simple capacitance C_{eq}. This capacitance can be obtained from the following equation for parallel and series combination of capacitances

$$C_{eq} = \frac{C_d N_p \cdot C_q N_p}{C_d N_p + C_q N_p} + C_m N_{tot}, \tag{3.7}$$

where N_p denotes the number of passive cells, and N_tot is the total number of SPAD cells present [10].

3.2.3 AFBR-S4K33C0125B equivalent model

It is impossible to gain complete information of the SiPM that is going to be used from its datasheet. This particular SiPM has the part designation AFBR-S4K33C0125B [7] and is produced by the Broadcom corporation. The construction of its equivalent circuit is far from straightforward. The manufacturer provides information about the SiPM's noise characteristics and performance but no information about its internal structure is available. It is, however, possible to deduce some information from the provided time constants and gain values.

If we put the value of gain provided by the manufacturer of $1.74 \cdot 10^6$ into equation 3.1 and rearrange it we gain

$$C_d = \frac{Gain \cdot q}{V_{ov}} = \frac{1.74 \cdot 10^6 \cdot 1.602 \cdot 10^{-}19}{5} = 55.75 \text{ fF}, \tag{3.8}$$

which is the value of internal capacitance C_d for all SPADs in the AFBR-S4K33C0125B SiPM. It is normally assumed that the value of capacity C_q is one order of magnitude smaller than C_d [12] and this equates to 5.57 fF.

With values for capacities C_d and C_q and knowledge of time constants from equations 3.4 and 3.5, it is possible to obtain a value for R_q that should be reasonably close to the real value. Values of time constants provided by the manufacturer for 1 Ω loading resistance R_L are

$$\tau_f = 5.2 \text{ ns} \tag{3.9}$$

and

$$\tau_s = 33 \text{ ns } [7]. \tag{3.10}$$

It is possible to use the analytical formula from 3.5 to calculate the value for R_q as

$$R_q = \frac{\tau_s}{C_d + C_q} = \frac{33 \cdot 10^{-9}}{55.75 \cdot 10^{-15} + 5.57 \cdot 10^{-12}} = 538.16 \text{ k}\Omega. \tag{3.11}$$

Resistance R_d cannot be set in this manner even though it could be calculated using equation 3.4. This is caused by the resistance value. Resistance R_d is two orders of magnitude lower than R_q, and parasitic resistances would present too big of an error. However, this value does not hold significant importance. Generally, its set in the range of single kilohms, and its value in this range doesn't influence the output signal very much [12]. Using stepping analysis the resistance of R_d was set to 6 kΩ.

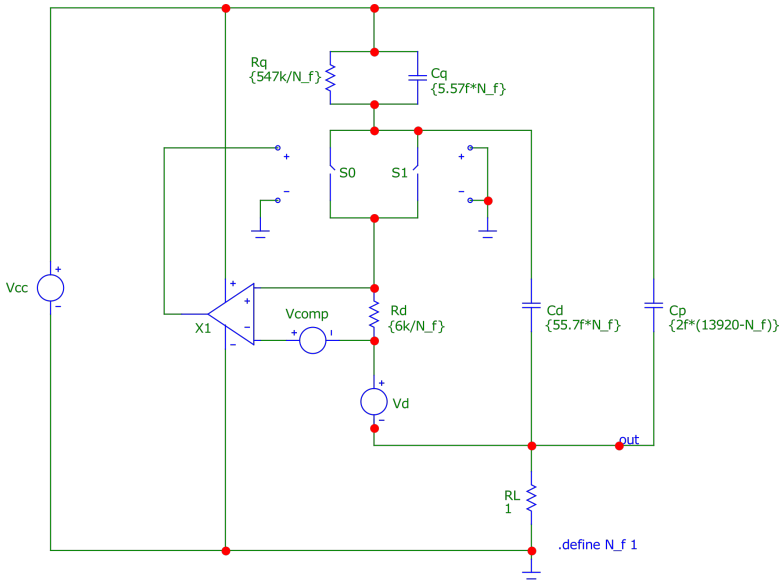

Figure 3.15: Complete equivalent model of SiPM used for simulation

Now the only circuit variable which is missing is C_p. It represents a parallel combination of capacitances C_{eq} and C_m. The analytical equation for obtaining C_{eq} is already mentioned in equation 3.7. This capacitance does not influence the output signal very much. It mainly acts as a low-pass filter on SiPM's output. Though it is possible to calculate capacitance C_p, the stepping analysis showed that this value is too large and doesn't allow propagation of fast enough signal to SiPMs output. For this reason, a smaller capacitance was chosen for this part of 2 fF.

Now that all equivalent circuit variables are set, it is possible to present the final equivalent circuit used for the simulation of the SiPM, see figure 3.15.

This equivalent circuit was constructed with the ability to simulate multiple SPAD cells outputting a signal at once. This was achieved by defining macro N_f for the number of cells currently undergoing an avalanche discharge. All component values are then derived from the number of firing SPADs as a multiplication of their base value calculated in the previous chapter. This approach was taken from: The Improved SPICE electrical model of silicon photomultipliers [12]. The cells which are not active are then calculated as a difference between total number of cells N_{tot} and the active cells. The number of all cells N_{tot} was taken from the SiPMs datasheet [7], and it is 13920.

The current at which the avalanche quenches was set to 100 μA the same way it was done in [12]. The avalanche discharge current waveform can be seen in the picture 3.16. It is apparent that the current rapidly rises to almost 1 mA, and then the quenching circuit limits the current flow. After 1.7 ns, the current is quenched when it reaches 100 μA thanks to the switch S_0 opening.

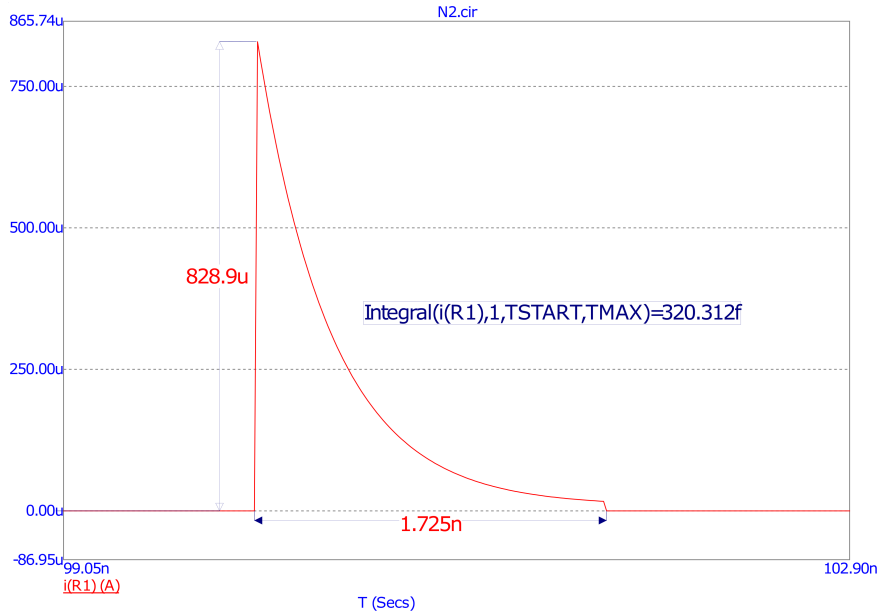

Figure 3.16: Current flowing through R_d during an avalanche discharge.

The integral of this simulated current was calculated using the simulation program to check for the correctness of the suggested equivalent model. The sum of charge released by a single avalanche discharge in the designed equivalent circuit was simulated as roughly 320 fC, see figure 3.16. If we use the gain equation 3.1 and the value for gain stated by the manufacturer to calculate the resulting released charge, we get

$$Q = Gain \cdot q = 1.74 \cdot 10^6 \cdot 1.602 \cdot 10^{-19} = 278.7 \text{ fC}. \tag{3.12}$$

The simulated value of the output charge is very close to the analytical value gained in equation 3.12 where the charge Q was calculated with the

gain declared by the manufacturer [7]. Therefore it is possible to state that the suggested equivalent circuit is a very good representation of the AFBR-S4K33C0125B SiPM detector.

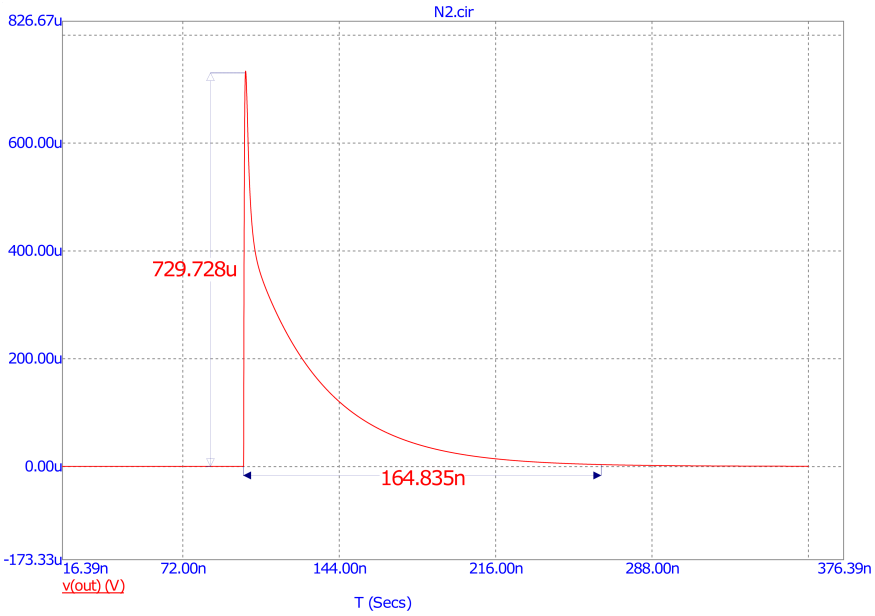

Figure 3.17: Output voltage signal waveform with loading resistance of 1 Ω

This circuit's resulting output voltage waveform is in the picture 3.17. The divide in the falling edge for the slow and fast time constants can be clearly seen here. The voltage amplitude is slightly lower than was expected. However, as the manufacturer did not supply this value, no comparison could be made.

Chapter 4

SiPM Readout board

In this chapter, the design and construction of the SiPM readout board will be described. At first, the biasing circuit for SiPM will be designed. The design and simulation of the amplifier chain follow. This chapter is concluded with details about the PCB design and information about its construction.

4.1 SiPM biasing circuit

Before the amplifying circuits can be designed and simulated, the problem of reverse biasing voltage present at the SiPM's terminals has to be addressed. In all calculations and simulations that were carried out, overvoltage of 5 V was used. To achieve this overvoltage, either 30 V has to be brought to SiPM's cathode or −30 V to the anode. For this system, the latter option was chosen. This was done in order to have the SiPMs cathode at a potential close to 0 V. The cathode can now be connected directly to a transimpedance amplifier without additional circuitry.

The biasing voltage should not exceed 30 V. Raising voltage above this level would only increase noise and would not lead to improved detection efficiency. So the goal was to design a circuit with an adjustable output voltage between −25 V and −30 V. This reverse voltage bias is described as V_{bias} in figure 4.2. After this voltage supply, there is a low-pass RC filter is placed in front of the SiPM. It is possible to use an RC filter because the quiescent current drawn by SiPM is around 1 μA.

The regulator LT3090 used for bias voltage does not provide a good option to adjust its output voltage safely. Because of this, another operational amplifier circuit had to be added, displayed in figure 4.1. This circuit is based on an operational amplifier in the inverting configuration. This provides a relatively low impedance, low noise voltage source that is fully adjustable in the SiPM's working voltage range. The gain of this circuit is based on the inverting amplifier gain and can be expressed as

$$V_o = -\frac{R_o}{R_i}(V_{cc} - V_{in+}) + V_{in+}. \tag{4.1}$$

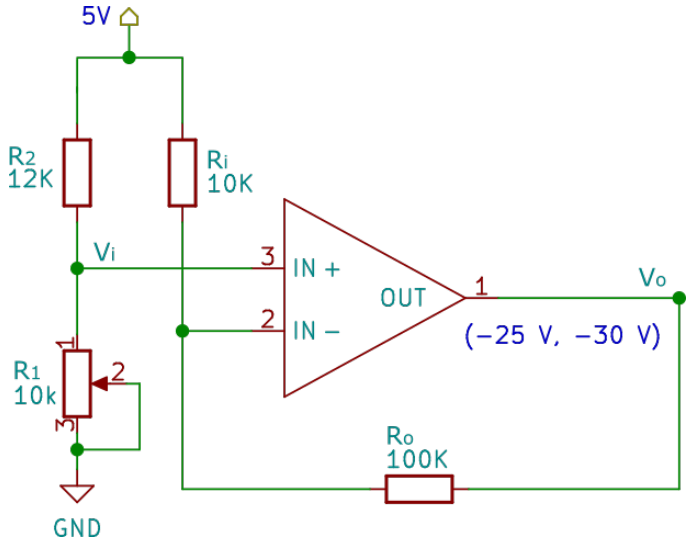

Figure 4.1: SiPM adjustable reverse voltage biasing circuit

In equation 4.1, V_o denotes the output voltage of the circuit, V_{cc} the supply voltage and V_{in+} voltage present at the non inverting terminal. The circuit with the corresponding components can be seen in figure 4.1. Given that we set an interval to which the output voltage can be set to $(-25\text{ V}, -30\text{ V})$, it is possible to rearrange equation 4.1 and gain an interval to which voltage V_{in+} can be brought to. The minimum and maximum voltage can be obtained from the same equation by substituting V_o by the intervals border values:

$$min(V_{in+(V_o=-30\text{ V})}) = \frac{V_o + \frac{R_o}{R_i}V_{cc}}{1 + \frac{R_o}{R_i}} = \frac{-30 + \frac{100\text{k}}{10\text{k}}5}{1 + \frac{100\text{k}}{10\text{k}}} = 1.82\text{ V} \tag{4.2}$$

$$max(V_{in+(V_o=-25\text{ V})}) = \frac{V_o + \frac{R_o}{R_i}V_{cc}}{1 + \frac{R_o}{R_i}} = \frac{-25 + \frac{100\text{k}}{10\text{k}}5}{1 + \frac{100\text{k}}{10\text{k}}} = 2.27\text{ V} \tag{4.3}$$

The minimum value for V_{in+} can be exceeded as the output of the operation amplifier won't exceed the voltage at its negative power supply pin. This voltage is set to -30 V by the lt3090 low drop voltage regulator. The other interval border condition can be set by the correct setting of the voltage divider present at the amplifier's noninverting input. For that, the voltage divider equation can be used

$$V_{in+} = V_{cc}\frac{R_2}{R_1 + R_2} \tag{4.4}$$

where R_2 and R_1 are the dividing resistances. To limit the current drawn by this divider and assure reasonable noise performance, the 10 kΩ trimmer was used for R_2. With this maximum lower resistance and the desired output voltage, it is possible to correctly set the resistance R_1 by rearranging the equation 4.4 to the following form

$$R_1 = R_2\left(\frac{V_{cc}}{V_i} - 1\right) = 10\text{k}\left(\frac{5}{2.27} - 1\right) = 12026\ \Omega. \tag{4.5}$$

This value for R_1 can be achieved by connecting 2k and 10k resistors in series. Now filtering capacitors can be added to this circuit, and the safe bias voltage supply circuit is complete. It allows only for voltages in the range from -30V to -25V, and SiPMs detectors should not operate in an unwanted region. Please refer to the schematic files attached to this thesis for the complete schematic.

4.2 Analog signal amplification chain

There are two basic ways of extracting a signal from a SiPM and amplifying it: voltage readout and current readout. The Voltage readout configuration was used to design SiPM's equivalent circuit, as seen in figure 3.14. This approach was chosen because the time constants provided by the manufacturer were derived from SiPM in series with loading resistance of 1 Ω [7]. However, during the analysis of SiPMs and SPADs in the previous chapter, it became apparent that the SiPM's output signal has mainly the character of a current pulse. This output pulse would have to be driven through loading resistance to obtain a voltage signal, and the voltage drop across that resistance would have to be read by a high input impedance amplifier. This approach introduces unnecessary complexity into the design and the loading resistance presents a compromise between signal steepness and bandwidth [5].

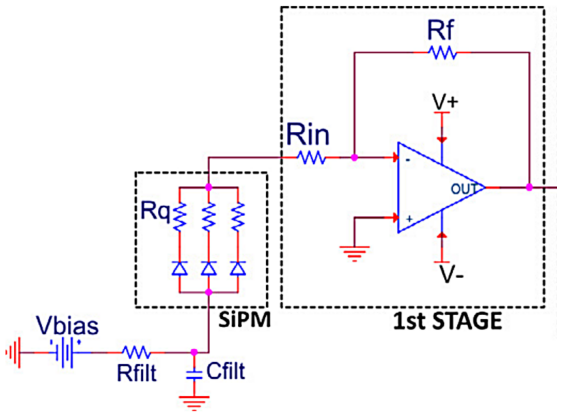

Figure 4.2: First stage transimpedance amplifier [5].

The other alternative is to read out the signal using a transimpedance amplifier. This type of amplifier presents very low impedance input for the signal directly at SiPMs terminals and therefore is ideal from the perspective of circuit

complexity. It is also advantageous as the losses at SiPM's inner parasitic inductance, and capacitance should not have that big of an influence [5]. This amplifier configuration can be seen in figure 4.2. Biasing reverse voltage is supplied at the SiPMs anode, and the cathode is driven close to the ground using the amplifier's feedback loop. Resistance R_{in} only suppresses any unwanted oscillations possibly caused by the amplifier's input capacitance. The gain of this stage is solely given by the value of resistance R_f.

4.2.1 First stage gain

The gain was determined by desired output voltage level and the SiPM output signal. The current output signal was analyzed in detail in the previous chapter. From the simulation, we can expect that the output signal from the SiPM will be in the range of single milliamps. However, we can expect multiple avalanche discharges in various SPADs to occur simultaneously [2]. The used simulation circuit in figure 3.14 has the capability for simulating these multiple discharges at the same time. It is stated in the manufacturer's datasheet that the biggest output signal is present for three photons being detected at the same time [7]. By simulating this event, we get that the maximum output current signal is roughly 2.2 mA. In reality, this signal will be significantly smaller due to parasitic low-pass filtering. However, it provides a good starting point for the gain calculation.

Output voltage swing depends on the used ADC. The chapter in which the choice was made follows this one. However, the input voltage range can already be used. Regarding the datasheet of LTC2175, the maximum safe analog input voltage is 1.8 V [14]. With this information, it is possible to calculate desired first-stage amplifier gain from the transimpedance output voltage formula

$$V_{out} = R_f \cdot I_{in} \tag{4.6}$$

and by reorganizing this formula, we get the desired value for resistance R_f and gain

$$R_f = \frac{V_{out}}{I_{in}} = \frac{1.8}{2.2 \cdot 10^{-3}} = 818.18\ \Omega. \tag{4.7}$$

This gain should ensure that the voltage signal at the output of this first-stage amplifier is maximized and, at the same time, it won't go above safe voltage levels. However, it doesn't offer any option for adjustments. For that reason, variable resistance in the form of a trimmer was used in the final circuit. In a later iteration of this design, it could be replaced by a fixed-value resistor.

4.2.2 Closed loop gain simulation

Closed loop gain analysis was carried out to verify the bandwidth of the designed amplifier. It was done using a standard AC analysis. SiPM was replaced by an ideal current source in parallel with SiPMs terminal capacitance. This capacitance C_i is necessary to include in the simulation because

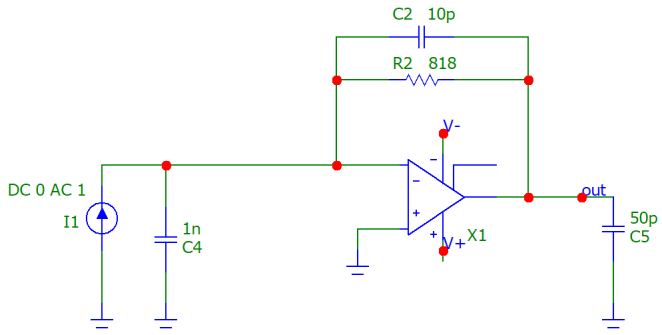

Figure 4.3: Fist stage closed gain simulation circuit.

it forms a pole in the feedback transfer function. As a consequence of this, it might cause instability. Other than that, additional capacitance loading of 50 pF was added to the amplifier's output. This capacitance represents the input capacitance of the second-stage amplifier.

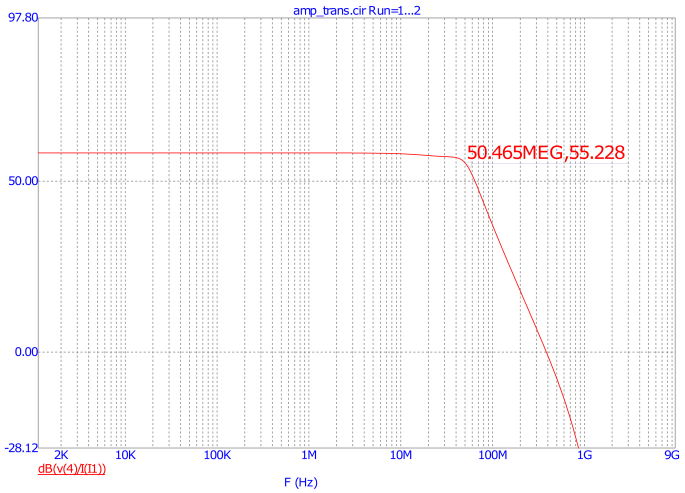

Figure 4.4: Closed gain amplitude Bode diagram.

The resulting closed gain simulation circuit can be seen in figure 4.3. For this circuit, the operation amplifier opa847 was chosen for its exceptionally wide bandwidth and noise performance. The resulting amplification is very flat through a very wide region and stays around the desired value. This value of gain can be calculated using the value of R_f from equation 4.7, and with this resistance, we get

$$Gain_{\mathrm{dB}} = 20 \log 818 = 58.25 \text{ dB}. \tag{4.8}$$

The bandwidth in the closed loop simulation can be seen in figure 4.4. The simulated bandwidth is higher than 50 MHz and the gain is within 3 dB of the analytically calculated value in 4.8. This is an excellent value because [5] states that for reading out the SiPMs signal 20 MHz bandwidth should be

sufficient. Although with this narrow bandwidth, some signal deformation is present in the rapidly rising edges [5].

4.2.3 First stage stability

With given gain and amplifier characteristics, it is possible to examine amplifier stability and design an adequate amplifier feedback loop. As the SiPM has a large terminal capacitance of 1 nF, the pole in the feedback loop transfer function

$$\beta_{(j,f)} = \frac{Z_{C_i}}{Z_{C_i} + R_f} = \frac{1}{1 + j2\pi f R_f C_i} \tag{4.9}$$

could be sufficiently low for the amplifier not to have a big enough phase margin and to oscillate. C_i in equation 4.9 denotes the capacitance present at the inverting input of the first stage amplifier. This capacitance can be approximated to 1 nF as the amplifier's input capacitance is only 3.7 pF and that is three orders of magnitude smaller than the SiPM's terminal capacitance [7]. β stands for the negative feedback loop transfer function and R_f for resistance present in the feedback loop. It is possible to rewrite equation 4.9 to

$$\beta_{(j,f)} = \frac{1}{1 + \frac{jf}{f_p}}, \tag{4.10}$$

where

$$f_p = \frac{1}{2\pi R C_n}. \tag{4.11}$$

The variable f_p represents a pole of feedback loop transfer function $\beta_{(j,f)}$. Because the transfer function of the used amplifier also contains a significant pole, the compound phaseshift of these two consecutive poles could reach 180 degrees and could validate the Barkhausen stability criterion. In that case, the amplifier would not be stable and would oscillate.

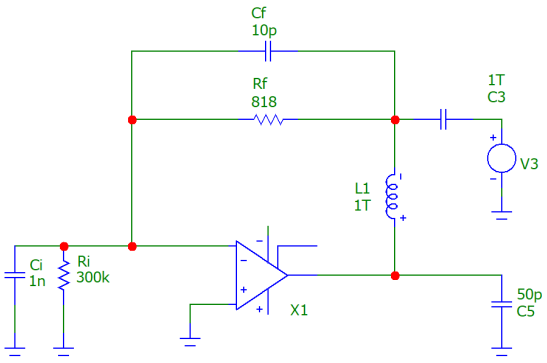

Figure 4.5: Circuit for simulation open loop frequency characteristics.

To prevent this scenario, we can introduce the capacitance C_f into the feedback network. This capacitance forms a zero in the transfer function $\beta_{(j,f)}$

and provides a phase shift in the opposite direction. It can negate the phase shift caused by the pole in a feedback loop. To set the zero frequency F_z correctly, the formula provided by the operational amplifier's manufacturer can be used. This equation is in the form of

$$\frac{1}{2\pi R_f C_f} = \sqrt{\frac{GBP}{4\pi R_f C_n}} [15], \tag{4.12}$$

where GBP stands for gain bandwidth product and all other variables were already described, see figure 4.3. This equation can be rearranged to get the required value for C_f:

$$C_f = \sqrt{\frac{C_n}{\pi R_f GBP}} = \sqrt{\frac{1\text{nF}}{\pi\, 818.18 \cdot 3900 \cdot 10^6}} = 9.99 \text{ pF}. \tag{4.13}$$

To approximate the $-3dB$ usable amplifier bandwidth, it is possible to calculate the square root of pole frequency and GBP:

$$f_{-3db} = \sqrt{\frac{GBP}{2\pi R_f C_n}} = \frac{3900\text{MHz}}{2\pi 818 \cdot 1\text{nF}} = 39 \text{ MHz}. \tag{4.14}$$

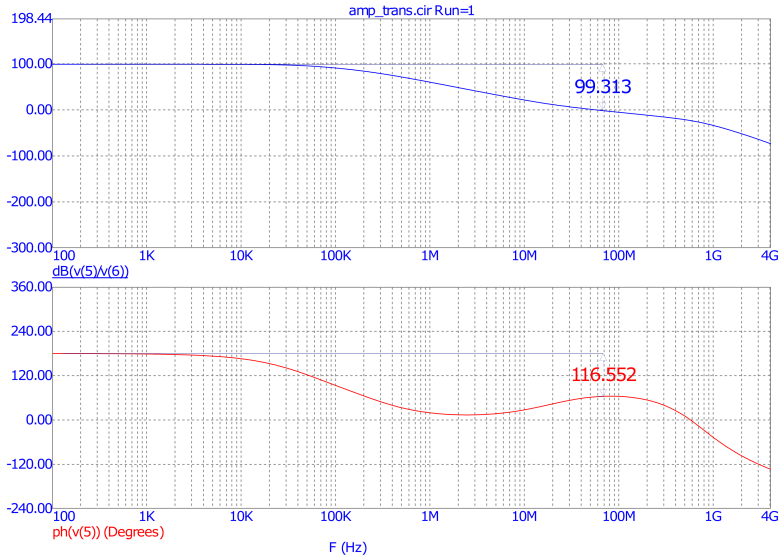

Figure 4.6: Open loop gain and phaseshift diagrams for circuit 4.5.

In [5], it is stated that a bandwidth of about 20 MHz should be sufficient to extract only a slightly distorted signal from SiPM. Given that the bandwidth of the suggested first-stage amplifier is almost twice as wide, it is a reasonable assumption that sufficient headroom is present. It was also confirmed in the closed-loop gain simulation. In this simulation, the resulting bandwidth came out at 50 MHz. This is a value even slightly higher than the analytically calculated value for bandwidth in equation 4.14.

An open loop gain simulation was performed to verify that sufficient phase margin is present and no oscillations will occur. Figure 4.5 displays the circuit used for this simulation. The closed feedback loop was broken up by large inductance $L1$ through which practically no signal flows. In addition, the signal source on the inverting terminal of the opamp was removed, and the signal was instead injected at the open loop end via the current source $V3$. To model the amplifier's internal resistance, a large resistance R_i was placed in parallel to capacity C_i. Other than these changes, all circuit components were used as calculated in the previous section.

The resulting graph of open-loop gain and phase shift can be viewed in figure 4.6. A sufficient phase margin is present at the point where open-loop gain crosses 0 dB. The phase shift only achieves 116 degrees of rotation, giving us a phase margin of more than 60 degrees. Therefore no oscillations should be apparent in the output signal.

4.2.4 Transient simulation

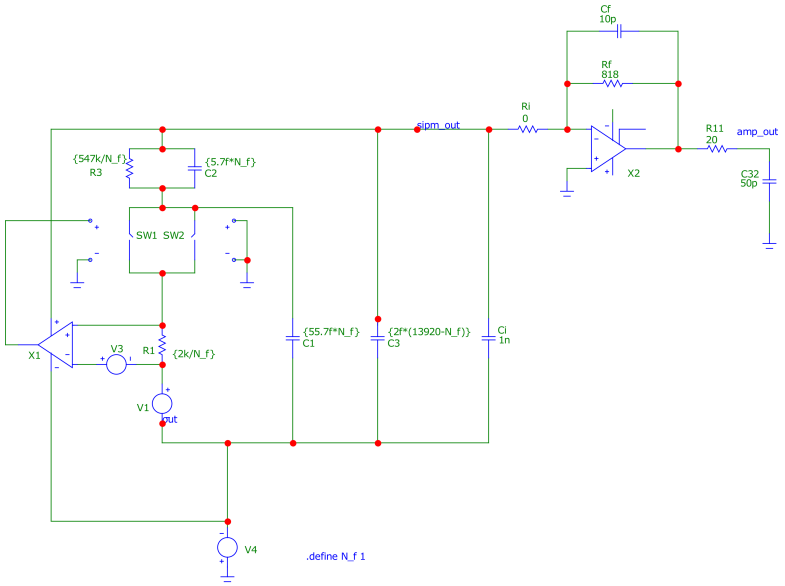

Figure 4.7: Circuit used for transient simulation.

For the transient simulation of the signal going through the first stage amplifier, a combination of schematics in figures 3.15 and 4.3 was used. Loading resistance was removed, and the SiPM's terminal was directly connected to the transimpedance amplifier. Capacitance C_i was added to the schematic as the manufacturer states this value as terminal capacitance [7]. This value might be lowered by the large biasing voltage of 30 V. However, the manufacturer did not mention this dependence, so the worst-case value was used. The resulting simulation circuit is in figure 4.7.

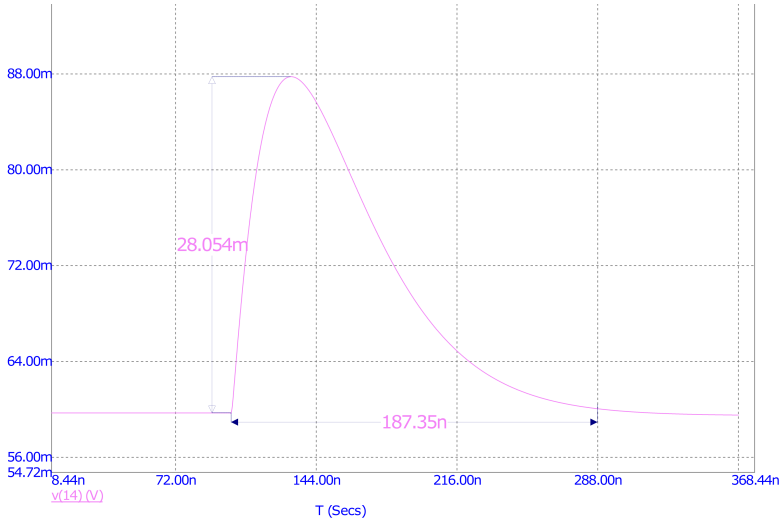

Figure 4.8: Transient output signal for circuit 4.7.

Using this circuit, the output signal was obtained. This waveform is depicted in figure 4.8. The waveform is significantly altered by the amplifier, mainly the rising edge of the pulse. The amplifier acts as a low-pass filter to the SiPM output signal from figure 3.17. As an effect of the amplifier's transfer function, the pulse on the amplifier's output is significantly widened. Also, the peak amplitude is not as high as it would be for an amplifier with an ideal transfer function.

4.2.5 Amplifier feedback T network

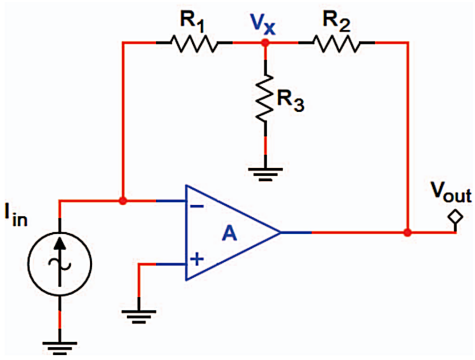

Figure 4.9: Amplifier T-network feedback loop [16].

To gain additional flexibility in the setting of the first stage amplifier gain approach of a T-network feedback resistance was chosen [16]. It is a method where the feedback resistance R_f of a transimpedance amplifier is replaced by a resistive network in the shape of a T, see figure 4.9. This configuration effectively acts as a combination of a transimpedance amplifier and a noninverting amplifier. The node in the middle of the three feedback resistances

will still have a voltage value of $R_1 \cdot I_{in}$. However, in contrast to a standard transimpedance amplifier, this voltage gets further amplified by the factor given by the noninverting configuration. This can be expressed as a set of two equations.

$$V_x = R1 \cdot I_{in}. \tag{4.15}$$

In equation 4.15, the variable V_x stands for the voltage in the middle of the T-shaped feedback loop. This is also illustrated in figure 4.9. The resulting output voltage can then be calculated as

$$V_{out} = V_x \cdot \left(1 + \frac{R_2}{R_1 || R_3}\right). \tag{4.16}$$

It is also possible to rewrite the extra amplification as

$$Gain = -m \cdot R_1 \tag{4.17}$$

where

$$m = 1 + \frac{R_2}{R_1} + \frac{R_2}{R_3}. \tag{4.18}$$

By this, we effectively gain the ability to increase gain without increasing the impedance in the feedback loop. Furthermore, it allows for better flexibility in setting precise amplification using of the shelf components.

4.2.6 ADC differential driver

For the purpose of signal digitalization, the LTC2175 ADC was selected. One characteristic of this ADC is that it has purely differential analog inputs [7]. The manufacturer of the ADC did not advise single-ended input. Due to this, a single-ended to differential driver had to be added to the amplifier chain. A highly integrated amplifier, LMH6553, was chosen. This particular option was selected because it is a white box solution for driving differential ADCs. In figure 4.10, there is a circuit that was used for the simulation of this stage. Voltage source V_9 serves as a common mode voltage supply. This source was replaced by ADC common voltage reference in the final design.

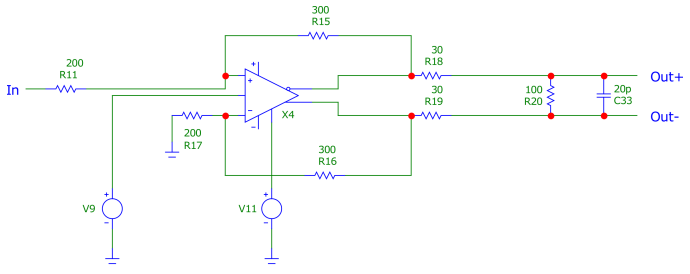

Figure 4.10: Differential driver simulation circuit.

With this design, there is no need to perform stability simulation because the manufacturer provides this data within the region where this amplifier will be

used. Thanks to this, no additional capacity was needed in the feedback, and no further stability analysis was necessary. Because this stage serves only for driving the ADC input, the desired gain for this stage is 1.5. Because of this, no significant nonlinearities are expected in the gain bandwidth.

A transient simulation was carried out with this second-stage driver. The designed SiPM model 3.14 from the previous chapter was used as a signal source. From the resulting signal shape in figure 4.11, we can assume that no significant distortion occurs at this stage, and thus, there should be no problem using this ADC driver.

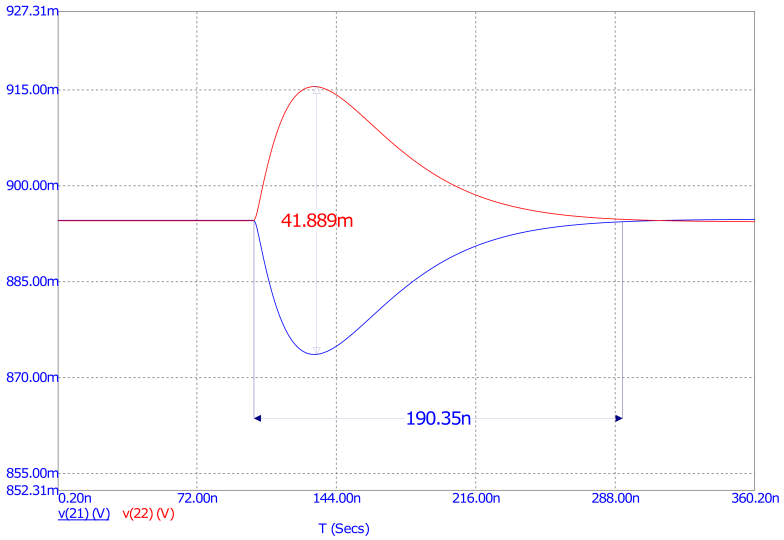

Figure 4.11: Differential stage transient analysis.

Another reason for the use of LMH6553 is the fact that it incorporates the clamping of the output signal. As the chosen ADC lacks this safety feature. Because SiPMs are sensors with relatively high voltage on their input, it is important to add overvoltage protection to the design. The clamping voltages are set by a voltage at the clamping pin of LMH6553. This voltage can be seen in the simulation circuit 4.10 as V11. The following equations give the Upper and lower limit of the output voltage:

$$V_{max} = V_{clamp} = 1.8 \text{ V} \tag{4.19}$$

$$V_{min} = 2 \cdot V_{CM} - V_{clamp} = 2 \cdot 0.9 - 1.8 = 0 \text{ V}. \tag{4.20}$$

Here V_{CM} stands for common mode output voltage, V_{min} for minimum output voltage, V_{max} for maximum output voltage, and V_{clamp} for voltage set at the pin setting the clamping voltage levels. As can be seen, if we set the common mode voltage V_{CM} in equations 4.19, 4.20 to $0.9V$ and V_{clamp} to $1.8V$, we get optimal output voltage swing. A very nice property of this output clamping operation is that no additional current flows through the pin through which

the clamping voltage is set. This allows the use of a relatively high-impedance voltage divider, and no extra components are necessary. Another important advantage is that external clamping diodes don't have to be used. These usually increase the capacitance present at the ADC input and introduce a significant leakage current.

4.3 Analog to digital converter

In most applications, ADC is chosen based on specific design requirements. In this particular case, the choice of ADC was also influenced by ongoing semiconductor shortages. Most converters suitable for this application were not available. In the end, LTC2175 from analog devices fulfilled all imposed requirements and was chosen for this readout system.

4.3.1 Converter requirements

The primary requirement was that the converter must have a digital LVDS interface. This requirement was given by choice of FPGA interface and its board design. However, the maximum number of channels was exceeded. The FPGA breakout board only has 8 LVDS pairs that can be used as FPGA inputs. The LTC2175 uses 8 pairs for data transfer and 2 additional pairs for clocking signals. This meant that not all 4 channels might be usable, and to make them all available, another FPGA board would have to be used in the future. In the end, the solution was to modify the FPGA board to gain extra 2 LVDS pairs on the board's input. This will be described in detail in FPGA board chapter.

Table 4.1: ADC requirements.

Metric	Required	LTC2175	Unit
Sampling rate	50.16	125	Msps
N. of analog channels	4	4	-
Interface type	LVDS	LVDS	-
N. of LVDS channels	<8	10	-
Bit resolution	8	14	bit

The next item in the requirement table 4.1 was the number of analog input channels. This requirement was not an important one as simply more ADCs with a smaller number of input channels could be used. However, in the end, it was possible to source a converter with all 4 channels.

The sampling rate played also a major role in the ADC selection. The signal that is read out is not periodical, so the Nyquist theorem could not be used. An arbitrary requirement was set that at least 8 samples should be taken during each SiPM output pulse. This amount was chosen with the knowledge

that part of SiPM signal post-processing is an integration of pulse waveform [5]. With at least 8 samples per pulse, a reasonable integration estimate could be carried out and therefore the number of detected photons estimated. If we use the length of signal calculated from the SiPM slow time constant 3.5 the minimum sample rate can be then calculated as

$$f_{min} = \frac{1}{\frac{5 \cdot \tau_s}{N_s}} = \frac{1}{\frac{5 \cdot 33 \cdot 10^{-9}}{8}} = 51.6 \text{ Msps} \tag{4.21}$$

where f_{min} stands for minimum sampling rate, N_s for required number of samples per segnal pulse, τ_s for timeconstant of output pulses slow exponential fall. The time constant τ_s is multiplied by 5 as that is the value when the exponential signal of a first-order system falls below 5 % of its value. By equation 4.21, the minimum sample rate was established. However, the FTDI interface between FPGA and PC has the capacity for sample transfer with the frequency of 100 MHz. A higher sample count is better for signal reconstruction, and thats why this maximum sample rate of 100 MHz was ultimately used.

4.3.2 LTC2175

As can be seen in the table 4.1, LTC2175 does fulfill almost all the main requirements imposed by this application. The fact that not all channels can be used with the FPGA board that was chosen is acceptable. In the future, a different FPGA board could be used. This would enable reading out data for all channels and with higher frequency. For the purpose of this diploma thesis, small modifications were made to the FPGA board. These are visible in figure 5.2. The modifications consist of 2 extra PCBs placed on the board to connect the FPGA to floating pins on the connecter. Ultimately this modification was not successful and the data transfer on these channels could work only on lower frequencies. However, with these additional LVDS channels, the design procedure could go forward at the time.

Noteworthy is also the fact that the ADC exceeds the required sample rate and bit depth. Again because of limitations on the FPGA side, only 8-bit resolution with a sample rate of 100 Msps can be used. The FPGA SPARTAN-6 that was used does not support high enough frequencies on its LVDS inputs [17] to support 14-bit signal sampling at 100 Msps.

The use of different FPGA or SPARTAN-6 with higher speed grade could allow for higher sample rates. In the future, it provides some headroom for possible improvements, namely pairing this board with an FPGA capable of faster frequencies.

4.3.3 LTC2175 digital output

The simplified diagram of the LTC2175 ADC is displayed in picture 4.12. Data output is provided in 2 options: One LVDS pair for each analog input

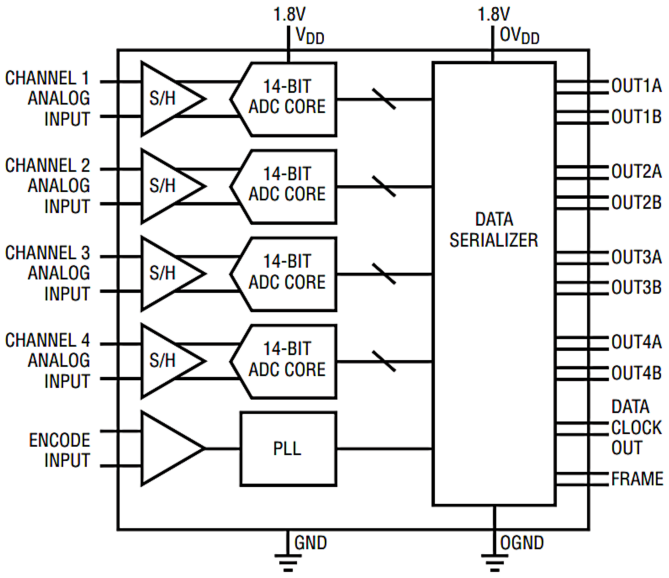

Figure 4.12: LTC2175 internal simplified diagram [14].

or there is the possibility of utilizing 2 LVDS pairs per analog input. In this case, dual LVDS output was chosen due to the effect on the frequency of the output signal. The usage of two channels allows us to effectively half output clock frequency. There is also no need for sampling the signal in any higher depth than 12 bits. The FTDI interface allows only for 8 bits per channel, so any bits beyond this value will not be used anyways. This leaves us with the choice of 2 LVDS lane 12-bit mode.

The output timing diagram of this mode is displayed in figure 4.13. In that diagram, ENC stands for ENCODE signal, which starts the analog to digital conversion and effectively determines the output data clock (DCO) frequency. The FRAME signal encapsulates the data bits that belong to one particular sample. The ADC is set to this mode via the SPI interface. For setting the ADC to this mode, a microcontroller ATTINY13-20SU was added to the design. An extra microcontroller was used in order to save IO for the readout system. The code for programming the ADC can be seen in the files attached to this thesis.

To further explain the choice of output data mode, we first need to consider the capabilities of the particular FPGA that will be used for running the readout system design. In this case, chosen FPGA is SPARTAN-6. The manufacturer states that the highest guaranteed bitrate of a given speed grade for input double data rate register (IDDR2) is

$$Bitrate_{max} = 625 \text{ Mbit/s[17]}. \tag{4.22}$$

This imposes limitations on LVDS frequency that can be used for DATA input. The 2-Lane,12-Bit serialization mode provides the lowest output data

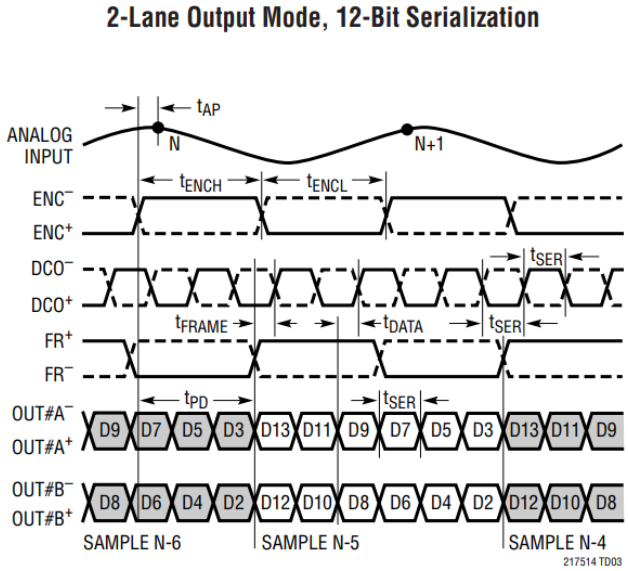

Figure 4.13: LTC2175 2-Lane 12-Bit mode timing diagram[14].

frequency of:

$$f_{out} = 3 \cdot f_s = 3 \cdot 100 \text{ MHz} = 300 \text{ MHz} \tag{4.23}$$

where f_s stands for the ADC sampling frequency. The 100 MHz sampling frequency was chosen specifically with the IDDR2 maximum bitrate in mind. Output data is latched after each rising and falling edge of DCO, and the resulting output bitrate can be therefore calculated to

$$Bitrate_{out} = f_{out} \cdot 2 = 600 \text{ Mbit/s} \tag{4.24}$$

In this mode, with this sampling frequency, it is possible to fulfill the sampling frequency requirement from table 4.1 and still have minimal headroom when it comes to the FPGA maximum input bitrate.

Another important fact to point out is allowed inter-signal delay. ADC timing diagram in figure 4.13 states that data signals are latched out with a 90-degree phase shift from the DCO clocking signal. This gives a safety interval of sorts to the FPGA to latch the incoming data on the DCO edge without any signal hazards occurring. This safety interval is described as t_{DATA} in figure 4.13 and can be calculated with the following equation

$$t_{DATA} = \frac{1}{4 \cdot f_{out}} = \frac{1}{4 \cdot 300 \cdot 10^6} = 0.83 \text{ ns}, \tag{4.25}$$

where f_{out} is DCO frequency. This gives us a safety interval to read data of 1.67 ns if we consider the time margin on both sides of the DCO edge. The difference in signal delays should not be close to this value, but it provides boundary conditions for the PCB design. This value will be referenced for designing LVDS microstrip connections in the board design section that follows.

4.4 PCB design

As a part of the readout system, a PCB with the amplifier chain and ADC had to be designed. The whole design of the PCB was done using the open-source Kicad software. This software offers industry-grade design possibilities. It is freely available and, under its license agreement, virtually free to use [18].

For all the circuits that were simulated in previous chapters, power supplies had to be added to the design. Their architecture will be briefly summarized. However, their design will not be discussed in detail because it is beyond the scope of this work. Please refer to the complete schematic for more details.

The design of the PCB was carried out in reverse compared to the signal chain. First, the connection to the FPGA board was chosen. This was done because the connection to the FPGA board was already given and could not be altered. The rest of the board layout could be changed freely on the go. The design description within this chapter will therefore follow the same trajectory. It will start with the LVDS interface then the power supply architecture will follow.

4.4.1 Board material and stackup

The Stackup of the design board had to be at least 4 conductive layers because the design incorporates controlled impedance tracks. With 2 layer design, these tracks become highly impractical since they require unreasonable widths to reach desired characteristic impedance for LVDS.

In figure 4.14, the used stackup is shown. As mentioned before, it has 4 conductive copper layers. Layers 1 and 4 will be used for high-speed signals, and the inner layers will mostly be used for power lanes. This configuration is useful since it allows us to calculate all impedances only with one material in mind. The core's (Rodgers 4350) characteristics are therefore not as important as the characteristics of Rodgers 4450F which was used as a laminate for outer layers.

The used materials from the Rodgers family of products offer superior high-frequency performance to standard materials, for example FR4. They offer better fill factor and, therefore, lower inconsistencies in their impedance [19]. These materials also have lower electric permeability and allow for thinner impedance-controlled tracks.

4.4.2 LVDS trace length matching

The first matter that had to be addressed with the LVDS interface to the FPGA board was the pair length mismatch on the FPGA's board side. The FPGA board was not originally intended to receive signals with timing tied together. This could cause timing issues on FPGA's pins if not compensated

Figure 4.14: Used Rodgers material board stackup.

for. The length of individual traces on the FPGA board can be seen in table 4.2 in the second column.

However, firstly before any matching of length could be done, the maximum safe inter-signal delay had to be stated. Equation 4.25 states the delay of the clock edge from the data signal edge. Using this interval as a safe delay would cause problems because the signal edges could overlap and cause mistakes in data transfer. Therefore one-fifth of this time interval

$$t_{safe} = \frac{t_{DATA}}{5} = 166 \text{ ps} \tag{4.26}$$

was used as a safe inter-signal delay. Using this safe delay, it is possible to determine the maximum allowed difference in trace length. The equation for propagation delay

$$t_{PD} = 85\sqrt{0475 \cdot \epsilon_r + 0.67} \text{ [ps/in][20]} \tag{4.27}$$

can be used. Here t_{PD} stands for propagation delay in picoseconds per inch and ϵ_r for substrate relative permittivity. For this equation to be more usable, it has to be converted to the metric system

$$t_{PD} = \frac{85\sqrt{0475 \cdot \epsilon_r + 0.67}}{25.4} \text{ [ps/mm]} = \frac{85\sqrt{0475 \cdot 3.52 + 0.67}}{25.4} = 5.12 \text{ ps/mm} \tag{4.28}$$

With this altered equation 4.28, it's possible to get a value for signal delay per millimeter. With the knowledge of signal delay per trace millimeter, it is possible to proceed to length matching. The second signal for the fourth data channel was intentionally left out from this length matching as it goes through an additional LVDS driver, and that adds extra delay on top of the propagation delay. This driver delay is much larger, so this will have to be

Table 4.2: LVDS trace lengths and signal delays.

Signal	FPGA length	Length total	Mismatch	Delay
DATA1A	62.0 mm	102.7 mm	20.6 mm	105.5 ps
DATA1B	44.9 mm	83.7 mm	1.6 mm	8.2 ps
DATA2A	36.2 mm	71.5 mm	10.6 mm	54.3 ps
DATA2B	38.9 mm	71.2 mm	10.9 mm	55.8 ps
DATA3A	48.6 mm	81.6 mm	−0.5 mm	−2.56 ps
DATA3B	48.6 mm	85.9 mm	3.8 mm	19.5 ps
DATA4A	49.0 mm	78.9 mm	−3.2 mm	−16.4 ps
DCO	49.6 mm	82.1 mm	0.0 mm	0.0 ps
FRAME	33.8 mm	83.2 mm	1.1 mm	5.6 ps

addressed within the FPGA readout code.

As previously stated in table 4.2, in the second column, there are the signal trace lengths for the FPGA board. The third column of the table contains the signal trace lengths with the SiPM readout board traces incorporated. As can be seen in 4.13, the DCO and FRAME signals determine when DATA signals are sampled and assembled into individual measurements. That is why extra care was taken in order to make these signal traces longer. This was done using the meandering of the signal trace. In figure 4.15 this is apparent for the traces in the middle.

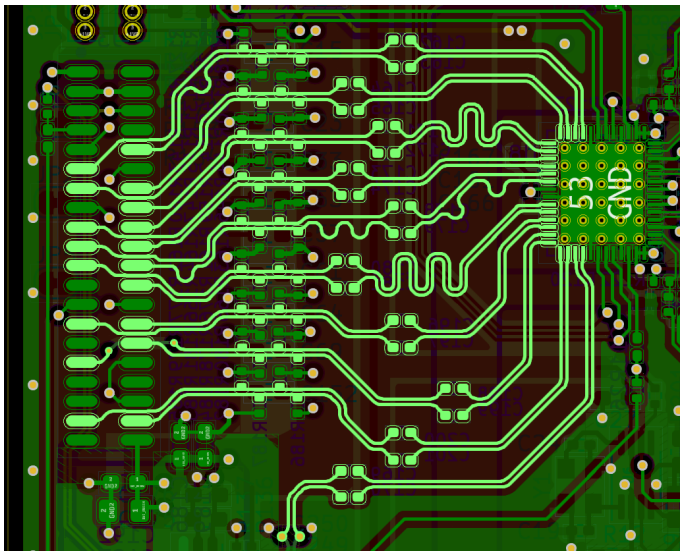

Figure 4.15: SiPM Readout board LVDS trace layout

The mismatch of the other signals is then derived from the length of the DCO signal. The signal with the largest amount of skew is DATA1A. Using the value for propagation delay from equation 4.28, the skew between DCO and

DATA1A can be calculated by the following equation

$$\Delta t_{DATA1A} = (l_{\text{DATA1A}} - l_{DCO}) \cdot t_{PD} = (102.7 - 82.1) \cdot 5.12 = 105.47 \text{ ps}, \quad (4.29)$$

where l_{DATA1A} stand for length of first data LVDS lane, l_{DCO} for length of clocking signal trace and t_{PD} for propagation delay. This delay of 105 ps is approximately 1/8 of the time delay between the data signal and clocking DCO edge, from 4.25. From this, we can assume that even for the most mismatched LVDS data channel, no incorrect reading of signal should occur due to inter-signal delay.

After inspecting the delay between LVDS signals, the delay caused by length mismatch inside individual pairs had to be done. Due to the connector positioning, this was an issue only for the DCO signal trace. As shown in figure 4.15, this mismatch was mitigated using the meandering of the shorter LVDS trace. Using this technique, this mismatch was shortened to a value well below an acceptable level.

4.4.3 LVDS isolation and biasing network

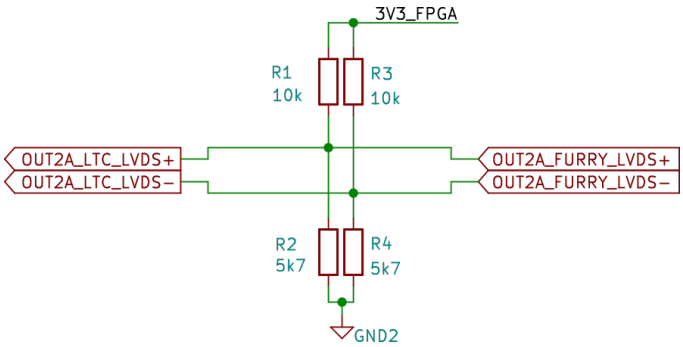

Figure 4.16: LVDS biasing resistor network

As shown in figure 4.15, each LVDS pair is equipped with isolation capacitors. This allowed for ground isolation of the FPGA board from the SiPM board ground. This feature might be practical if power supplies with different ground potentials were used, and that's why it was incorporated into the design.

However, the FPGA board cannot drive the LVDS channels to the nominal common mode voltage of 1.2 V [21]. To mitigate this problem, voltage dividers were put after the isolation capacitors to every LVDS trace. The schematic of this biasing network is in figure 4.16. These voltage dividers are driven from the FPGA board power supply and connected also to its ground. Normally these resistors would be placed close to the LVDS receiver, but this option was not available. The FPGA board does not have any option of incorporating voltage dividers in its LVDS lines.

Because these resistors are in the middle of the LVDS signal trace, their resistances had to be relatively high not to alter the controlled LVDS impedance too much. For this reason, the combination of 10 kΩ and 5.7 kΩ resistors was chosen as it was done in [22]. This drives the LVDS common voltage to

$$V_{cm} = V_{cc}\frac{R_2}{R_2 + R_1} = 3.3\frac{5.7\text{ k}\Omega}{5.7\text{k} + 10\text{k}} = 1.198\text{ V}. \tag{4.30}$$

This value is close to 1.2 V common mode voltage specified by the LVDS standard [21]. This circuit allows for data transfer even when the grounds of the boards need to be isolated. The resistance pads were placed on top of LVDS traces to minimize stub sizes which could cause impedance mismatch [23]. A detail of the resistor placement is in figure 4.17.

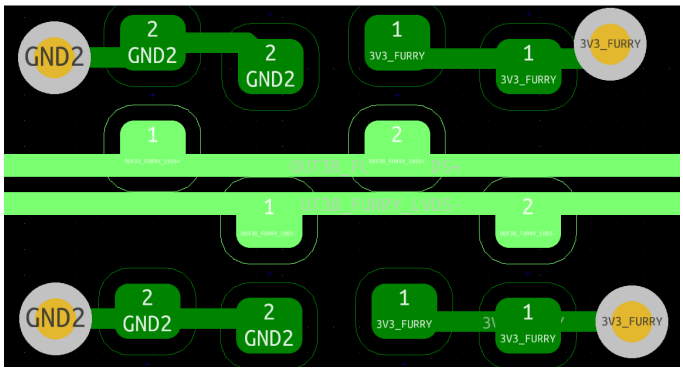

Figure 4.17: LVDS biasing network layout

4.5 Power supply architecture

Because power supply design is not a part of this thesis, the design procedure will not be discussed in detail. But the whole architecture will be presented to offer insight into how the SiPM readout board functions. All the designed power supplies were thoroughly simulated and should function without serious problems. For more detail, the reader can refer to the complete schematic.

The power supply diagram is sketched in figure 4.18. The figure shows that the external power connector accepts only one voltage in the range of $3 - 8$ V. All the other supplied voltages are generated within the board. This approach was chosen to allow for simple use of this readout system. It can be powered via a USB power adapter or a commercially available power bank.

Another important fact to note is that the designed amplifier chain and ADC should be operated under low noise conditions. To address this problem, all switching regulators were paired with low dropout regulators (LDOs) that provide a high power supply rejection ratio (PSRR). On top of that,

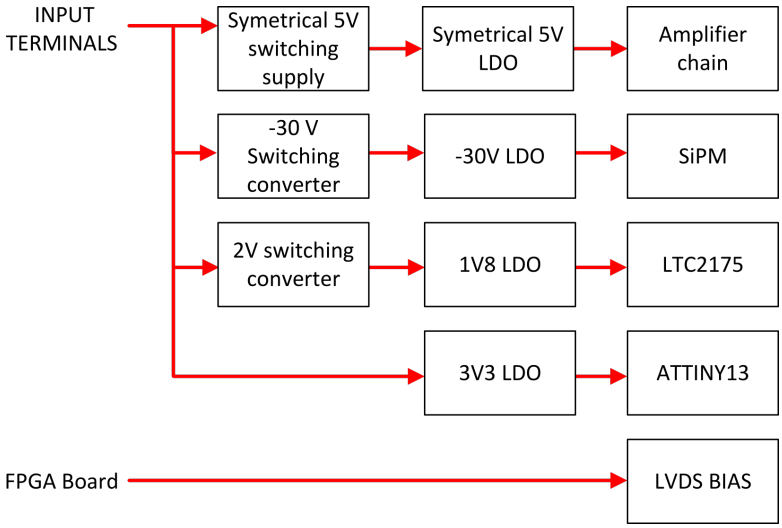

Figure 4.18: SiPM board supply diagram

low-pass filters were added on all power lines using ferrite beads in combination with low ESR ceramic capacitors. These decoupling low-pass filters were provided for all components directly connected to the analog signal chain.

One power line is taken directly from the FPGA board. The FPGA power supply has enough overhead so it can be used to power biasing circuits and TTL signal isolators. Under normal use of the SiPM readout board, this supply is not used. But to be capable of complete isolation, one power line from the receiving system must be supplied. This power line is displayed at the bottom of figure 4.18.

4.6 Complete PCB model

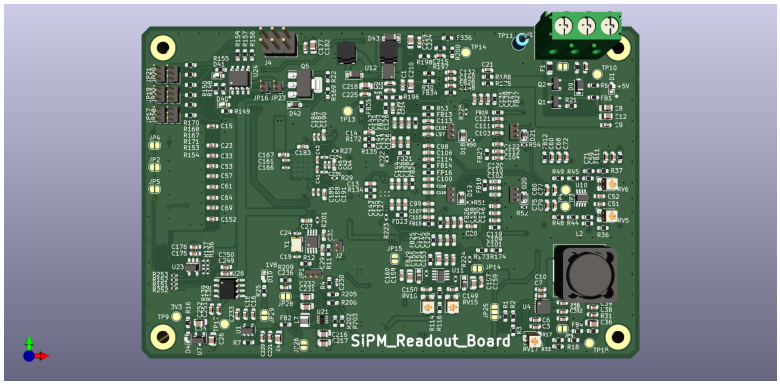

Figure 4.19: 3D render of SiPM readout board's front side

The 3D rendered model of the complete board design is in figure 4.19 and 4.20. A few unconventional decisions were made during the design process of this

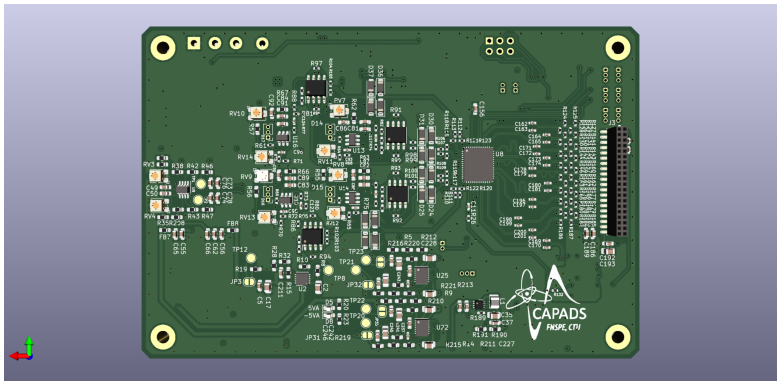

Figure 4.20: 3D render of SiPM readout board's back side

board. From figure 4.20, it is visible that the LVDS connector and the ADC are placed on the bottom side of the board. These components were placed on the bottom side with the connection to the FPGA board in mind. The FPGA board has its LVDS connector on the top, and putting the connector and ADC on the bottom side provides a convenient way to connect the boards without any additional cables. This connection can be seen in detail in the render in figure 4.21. This render was produced to make sure no components on the

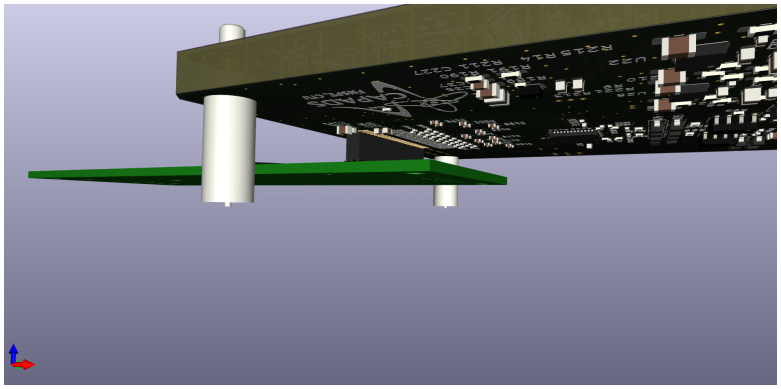

Figure 4.21: FPGA board connection

boards would collide with each other. Unfortunately, the FPGA board was designed in a different software environment, and rendering with all present components would be too time-consuming to produce. However, rendering the board's physical dimensions with the corresponding connector is more than enough to verify that the connection is possible without any issues.

Chapter 5

FPGA board

This chapter covers the readout system that was implemented within FPGA logic. The block diagram of the readout system is depicted in 5.1. All the functional blocks encapsulated by the red line are integrated inside the FPGA. The systems input data comes from the SiPM readout board covered in the previous chapter.

Firstly the input data enters the deserializer block. Here samples are assembled from the data incoming over the serial LVDS interface. The serialized sample bits are put into a register and latched out at once. These complete samples then enter the FIFO controller logic block. In short, this block puts the data in the communication FIFO buffer based on its internal state. The underlying communication is then carried out using the IP block: FTDI controller, which was taken from another project. This block controls the communication on the lower level and provides the data to the FT601 block. The FT601 integrated circuit provides a FIFO bridge over USB 3.1 and allows for high-speed communication up to 5 Gbps [24].

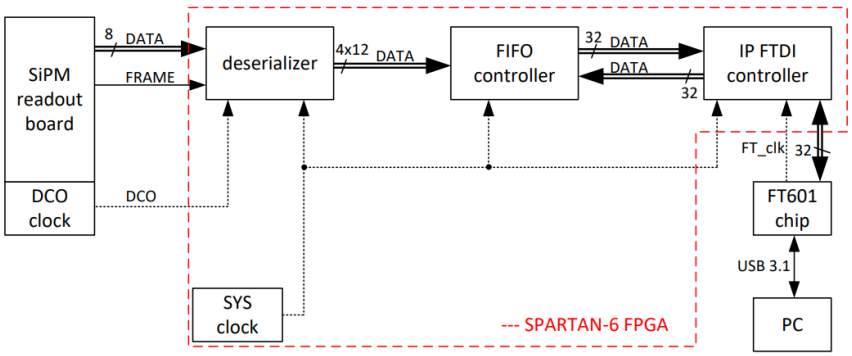

Figure 5.1: Readout system top-level diagram

5.1 FPGA board modifications

An FPGA on a PCB that was already available was used. This used PCB is shown in figure 5.2. The FPGA board had to be modified to fit this application. The following modifications were done to allow for proper connection to the SiPM readout board.

First modification is a different voltage supplied to one of the FPGA's IO banks. It is visible in figure 5.2 as a red jumper wire on the left. Through this jumper wire 3.3 V supply rail was brought to the IO bank. This supply rail does not require significant current flowing through it so a thin jumper wire was a suitable solution.

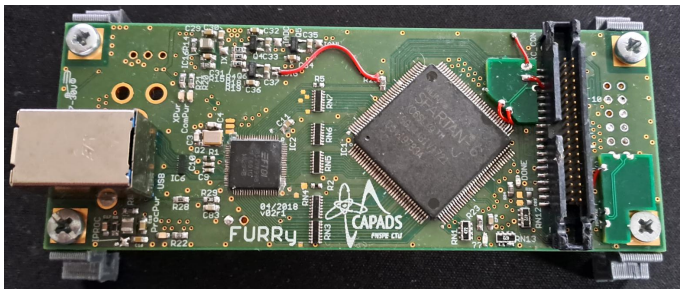

Figure 5.2: FPGA board

Another modification was needed to connect the fourth data channel to the FPGA. These LVDS connections were missing, and to avoid direct crossing of LVDS signals set of 2 extra PCBs was added. These provide impedance-matched traces on their surface, and thanks to the inner ground layer, they are shielded from signals underneath them.

This solution is far from perfect, and a drop in the data transfer performance occurred. However, at the time, it was an option that offered the best solution to gain extra LVDS connections that were required to test the proper functionality of the system.

5.2 Spartan-6

Spartan-6 is the FPGA that was used for this readout system. It is an FPGA produced by the 45 nm process. It incorporates IO logic regions connected directly to its digital IO pins. This enables the FPGAs from the Spartan family to be used for high-speed digital communication. The devices with the highest speed grade can achieve data rates up to 1080 Mbit/s [25]. This makes the spartan FPGAs perfect for a fast readout system like the one designed within this diploma thesis. All logic blocks were designed using the hardware description language Verilog-2001.

5.2.1 Deserializer

The deserializer logic is located in the IO region of Spartan-6. It is a logic region that provides high-speed clocking resources and logic primitives precisely for applications that work with serialized high-speed data [26].

The complete schematic which accurately describes this block's function is depicted in figure 5.3. The main difference from the implemented logic is that only one dual data channel is displayed here. In real design, all four analog channels are implemented. So there are 8 input LVDS data channels present. Besides the data channels, there is also 1 LVDS channel for the FRAME signal and one for the DCO.

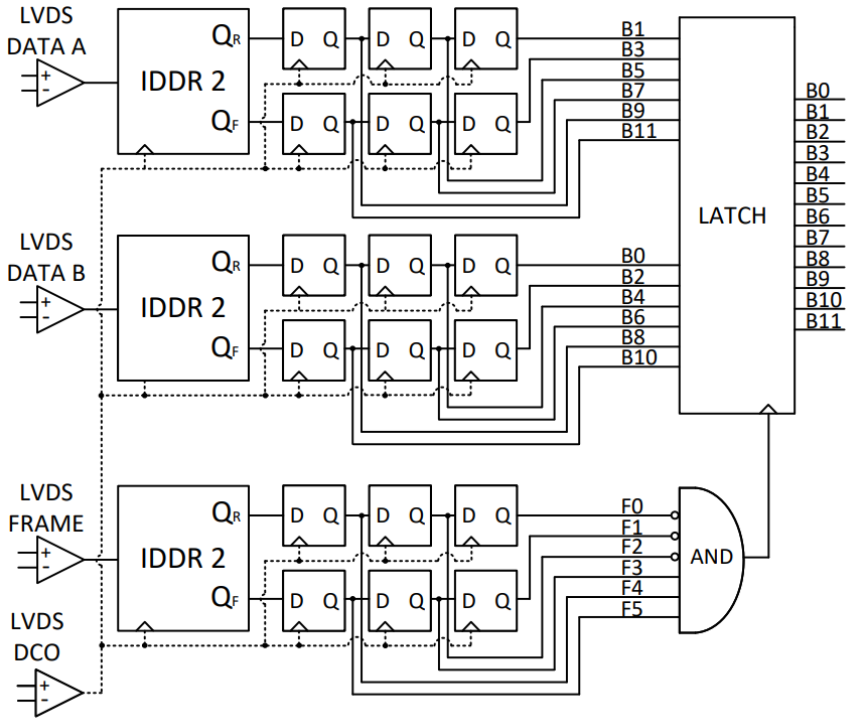

Figure 5.3: Single channel deserializer schematic

The first triangular block in all signal paths is called IBUFDS. This abbreviation stands for input buffer differential signal. Its only function is to convert differential signals to single-ended CMOS logic signals. It also allows for the configuration of various differential signal standards, and in this particular use case, the LVDS standard was used.

After the conversion, the data and frame signals enter the IDDR2 logic block. IDDR stands for input double data rate. IDDR2 is an improved version of IDDR in that it has two clocking inputs [26]. It is a logic primitive block that the manufacturer provides and it enables signal sampling on both clocking

edges. Therefore it effectively doubles the data rate of the incoming signal, and the name is derived from that. The output signals Q_R and Q_F in figure 5.3 stand for data sampled on the rising and falling edge of the incoming signal, respectively.

In the SPARTAN-6 FPGA, a primitive for data serialization exists. It is called ISERDES2 [26]. During the initial design of deserializer logic, this primitive was to be used. However, major problems with the design prevented that. The serializer logic could not fit into the IO region for all four channels. In the IO region, IO pins share resources in the SPARTAN-6, and the design with serializer blocks failed to be packed into the FPGA. However, IDDR2 primitive offer more than adequate alternative. Its guaranteed data rate is 625 Mbit/s, and within this readout system, data will be read out with the rate of 600 Mbit/s. For the calculation, see equation 4.24.

DATA signals and the FRAME signal sampled this way enter double 3-bit shift register memory, which is controlled by DCO. This approach allows to store all 12 bits of incoming data from the ADC in each data sample cycle. After all the bits from a particular sample enter the shift register, the frame signal pattern is examined.

The frame signal encapsulates each sample in its single period. To see the incoming signal waveform, refer to figure 4.13. To look for the desired frame waveform simple AND gate can be utilized. For the lower 3 frame bit inputs, negations are inserted on the AND gate input. This way, simple square waveform detection is achieved. Bits that are brought to the AND gate without negation are expected to be logical 1 and the negated bits represent the low half of the FRAME signal period. When encapsulating frame signal appears in the shift register, all the data bits are latched to the main FPGA logic. This latch serves as a synchronization element between the fast readout system and the main fabric, which uses a slower clock of 100 MHz.

Deserializer logic is also the only clocking region that uses its dedicated clock provided by the ADC. This clock is supplied by the ADC and can be tied to the system clock within the FPGA using extra outputs. Thanks to this safety feature, all conflicts caused by clock mismatch should be avoided.

5.2.2 FIFO controller

The output of the deserializer is 12-bit wide parallel bus, that is connected to FIFO controler block. The data enters the FIFO controller block synchronized with the system clock. The first alteration to data is that the four least significant bits must be dropped in each sample. The FIFO communication that follows supports only data width up to 32 bits, and that fits four 8-bit samples, one from each SiPM channel [24].

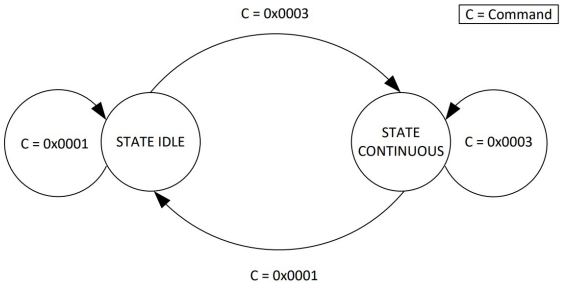

Figure 5.4: FIFO controller state machine diagram

The core of the FIFO controller block is a state machine that controls the operation of the readout system. This enables the PC program to effectively control the flow of data sent by the readout system. A simple diagram of the said state machine is in figure 5.4. The implemented state machine changes only between two states. If the FIFO controller is idle, no data samples are sent to the PC program. If its state is changed to continuous, it sends data out continuously. From the state diagram in figure 5.4, it is apparent that the only variable that controls the state change is the command. It is a message delivered from the program. Because the FIFO bridge is optimized for high data throughput applications [24] and not short command messages, a 4-byte value for state control had to be used. A basic communication protocol was developed to ensure communication without any mistakes in state-changing messages.

5.2.3 FIFO command message protocol

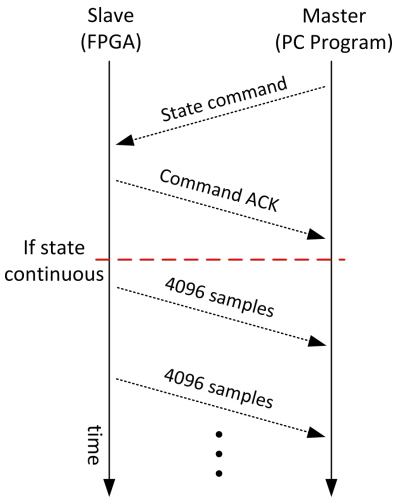

Figure 5.5: FIFO communication protocol flow graph

This message exchange protocol was implemented to improve communication reliability over the FIFO bridge and achieve a better communication structure. Because the communication has only two points, the roles of master and

slave were assigned. On the underlying communication, the FT601 chip and, thus, the FPGA controller act as master. Here the roles were assigned in reverse. This choice allowed the PC program to dictate data transfer flow and to control the measurements using software and user input.

Table 5.1: Table of command message formatting

Message	Byte[0]	Byte[1]	Byte[2]	Byte[3]
State Continuous	0x00	0x00	0x00	0x03
State Idle	0x00	0x00	0x00	0x01
State Idle ACK	0x00	0x00	0x0A	0x01
State Continuous ACK	0x00	0x00	0x0A	0x03

In figure 5.5, the y-axes act as time, and the arrows denote messages that go back and forward between master and slave. As in figure 5.5, each message transaction is initiated by the PC program, and an acknowledgment (ACK) message is expected from the slave. The way these messages are constructed on the bit level is presented in table 5.1. They are sent as 4-byte messages because the FT601 FIFO bridge does not allow for shorter data transfers. Command payload is carried by the last byte. The acknowledgment message sent by the slave FPGA is crafted from the command message by putting the 0xA hexadecimal value in the second to last byte. The last byte is taken from the command message, and this ACK message is sent back to mater. This message exchange is sent each time a PC application request a state change from the FIFO controller.

5.3 FTDI communication layer

FTDI communication is controlled by an IP block called FTDI controller taken over from a different project. This IP block, in combination with FT 601 chip, is used as a communication layer, on top of which the FIFO communication protocol is implemented.

It effectively acts as an interface between the FPGA and the PC program. It creates a pipeline of FIFO-style communication in both directions. This can be seen in figure 5.1. This FIFO is buffered on both sides with buffer lengths of 4092 samples. These samples have the same width of 32 bits and are supplied to the FT601 chip via CMOS 32-bit parallel interface. This data is translated into USB 3.1 communication by the FT601 chip. On the PC side, it can be retrieved using the dynamically linked library provided by the FT chip's manufacturer. The library has functions that can be called, but the codebase is not open. This conversion between communication layers is proprietary and, therefore, cannot be described further in detail [24].

Chapter 6

Readout program

The program that reads out data was implemented using the C++ language. An object-oriented approach was chosen for better code clarity and functionality separation. The object architecture is displayed in picture 6.1. Here it is visible that the program contains only three base classes: User Interface, FT Driver and Output Interface. Every object contains one functionality of the program, which will be described in the following sections.

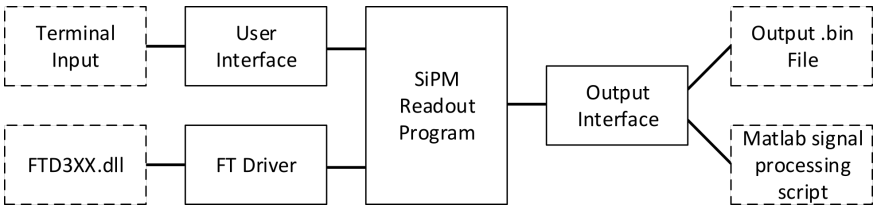

Figure 6.1: Readout program object architecture.

6.1 User Interface

At the start of program execution, the User Interface object is created. It processes all the arguments supplied by the user. Table 6.1 contains all the supported user arguments. After the user arguments processing, the primary function of the program can start.

Table 6.1: Table of supported user arguments

Argument	Description
-h	Display help.
-g	Run graph script.
-f	Output data to a specified binary file.

6.2 FT driver

FTDI communication is executed within the FT driver object. This object contains all the FTDI functionality and reference to the FTD3XX.dll library.

The function calls it contains are described within the programmer's reference guide [27]. All the FTDI calls are encapsulated within functions that are members of the FT driver. This approach allows for easy swapping of the underlying FT communication layer in the future.

When FT Driver successfully receives measured data samples, it calls the output interface object to save the captured data to a file.

6.3 Output interface

This object provides a layer for handling and writing to output binary files. The argument passed by the user specifies the filename. Data is written to this file in raw bytes in large buffers to optimize for writing speed performance.

After a specified number of bytes is written to the file, a call to a higher-level graph script is performed. This call is controlled by the -g argument, see table 6.1. This higher-level script is an optional step for further signal processing and presentation. In this thesis, Matlab script was used for plotting the results. However, it could be replaced by any other open-source option in the future.

Chapter 7

Measurements

As a part of the readout system development, a prototype of the SiPM board was manufactured and assembled. Initially, the performance of the LVDS interface between the two boards was examined. After that measurements of SiPM signals could be carried out.

The used workspace is shown in figure 7.1. A 4-channel power supply Rhode and Schwarz HMP4040 was used to power the SiPM board. Measurements of the analog signal were done with the Teledyne LeCroy WavePro 404HD-MS oscilloscope. In the configuration displayed in figure 7.1 the SiPM board is coupled to the FPGA boards via LVDS connectors on the PCB. The FPGA board is then connected to a laptop on which the readout program runs. The oscilloscope probe is placed on the ADC analog input. This point of the signal chain was chosen because the analog signal should correspond to the data measured with the readout system.

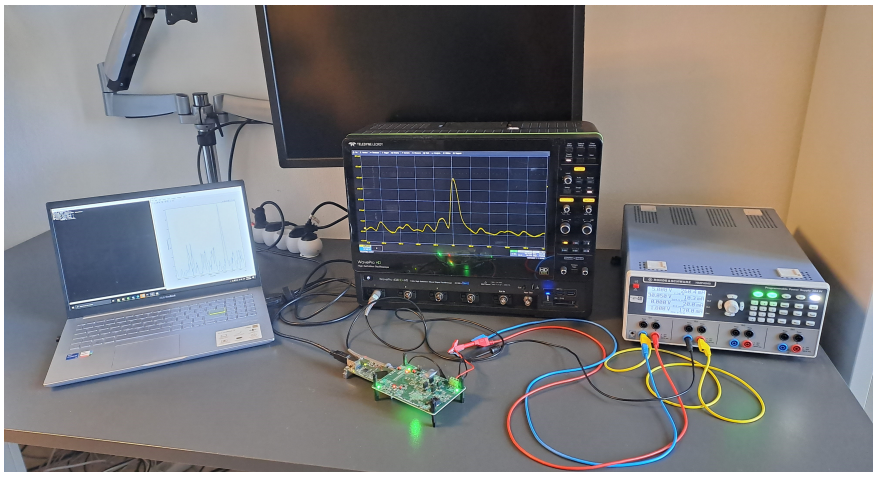

Figure 7.1: Measurement workspace setup.

7.1 LVDS interface

The LVDS interface between the boards was described in chapters 4 and 5. Because 2 LVDS traces were missing on the FPGA board two extra PCBs had to be placed on the board's surface. These modifications are displayed in figure 5.2. The PCBs placed on top of the FPGA board had properly impedance-matched LVDS traces. However, the cables connecting the PCBs to the connector pins were not.

Because of this, communication was not possible for the full sampling frequency of 100 MHz. With this sampling rate, the DCO reaches a frequency of 300 MHz. At this frequency, no data could be reliably transferred over this LVDS channel. However, communication was possible at 25 MHz sampling frequency. Therefore the proper function of other parts of the signal chain could be verified even for this channel.

In addition, communication was not possible for the first LVDS channel. To find the cause of this issue the common mode voltage and the signal were examined. The common mode voltage was measured to be exactly at 1.2 V, which is the correct value as stated by the SPARTAN-6 datasheet [17]. To inspect the signal a known bit pattern of 0b000001 was sent over the interface to measure the signal. The waveform in figure 7.2 was measured using a differential probe at the FPGA pins. The voltage swing is well above the minimum value stated in the electrical characteristics of SPARTAN-6. The measured swing was close to $0,85$ V and the minimum for correct signal reading is $0,25$ V [17]. In conclusion, the correct signal was entering the FPGA. However, no data was received by the system. The routed FPGA design was also examined and was confirmed to be correct. This indicates that the input buffer of the FPGA possibly suffered damage and is faulty.

Figure 7.2: Fits LVDS channel voltage at FPGA termination.

Due to these problems, only 2 SiPM channels could be used in the prototype board at full speed of 100 MHz data sampling rate. However, as the readout system's function could be verified with only two channels, this was not a

blocking issue for the testing of the prototype. In the future, the SiPM board is intended to be paired with different FPGA boards to alleviate these problems.

7.2 Capture of analog signal

For measurement of the SiPM pulses, a Plutonium-238 radiation source in combination with a scintillation crystal was used. A scintillation crystal serves as a converter of gamma rays to visible light as illustrated by figure 7.3. When the crystal is directly placed on a SiPM chip, the generated photons which are induced by gamma rays in the scintillation crystal are detected by the SiPM sensor. This technique is often used in medical imaging [28].

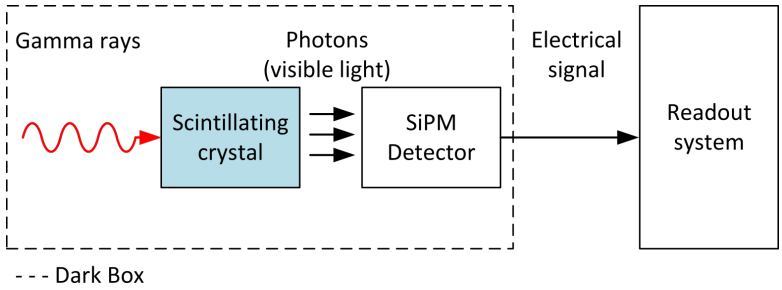

Figure 7.3: Schematic diagram of measurement configuration with Plutonium 238 radiation source.

The signal waveform measured using a high-frequency differential oscilloscope probe is depicted in figure 7.4. It contains one SiPM output pulse. The detected signal peak rises to 202 mV.

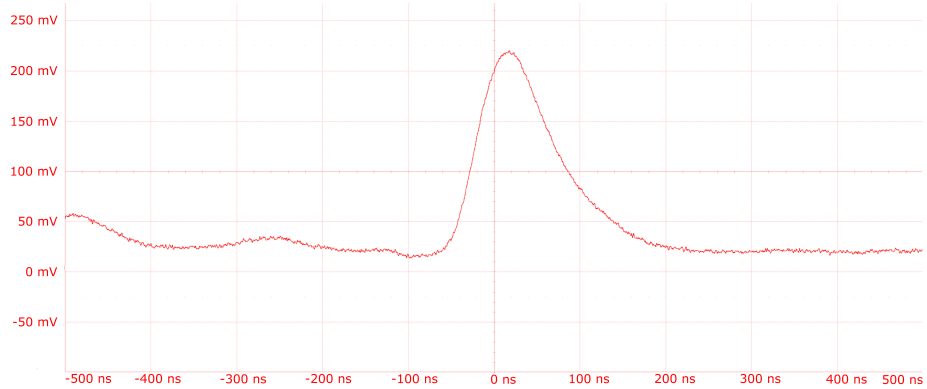

Figure 7.4: Captured analog signal pulse.

The measured pulse in figure 7.4 is wider than in the simulation. The measured pulse is approximately 240 ns wide. This increase in the pulse width can be attributed to the transimpedance amplifier's parasitic capacitances in the feedback loop.

From the waveform in figure 7.4, it is apparent that high-frequency noise is present in the amplified signal. This noise has a sinusoidal character and frequency close to 100 MHz. At first, the ENCODE signal of the ADC was suspected as a source of this noise. However, after the circuit was turned off, the noise persisted. This indicates that this noise comes from an external source and the FM radio broadcast is the most likely source. Although this noise is not significant enough to influence the SiPM signal, in a later iteration of the readout system, a filter could be added to the analog signal chain to suppress it.

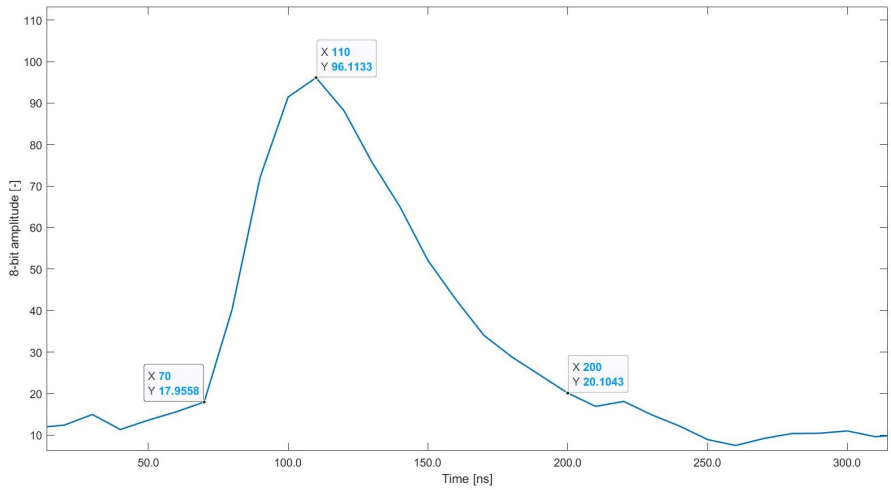

Figure 7.5: Signal pulse captured using the readout system.

When the signal was captured using the high-speed oscilloscope, it was also read out using the readout system itself. A segment of 25 ms of the SiPM signal was captured. This short signal segment was captured to keep the signal file size manageable. Because the frequency of output SiPM pulses is in the order of hundreds of kilohertz, a large number of SiPM pulses were present even in this short segment.

Figure 7.5 shows one captured pulse. The amplitude of the captured pulse is approximately 110 points out of the 8-bit resolution of 255. In this case, the voltage corresponding to a single bit V_{bit} is 1.9 mV. After multiplying the pulse bit height h_{bit} with this value, the resulting peak voltage is equal to

$$V_{peak} = h_{bit} \cdot V_{bit} = 110 \cdot 1.9\,\text{mV} = 209\ \text{mV}. \tag{7.1}$$

This means that this peak captured using the readout system has approximately the same amplitude as the peak captured using the oscilloscope, which had an amplitude of 202 mV.

7.3 Long time period measurements

To verify that the readout system is capable of detecting specific high-energy signal impulses, a measurement of the SiPM signal over a long time period was carried out. Within this measurement, all SiPM pulses above the threshold value of 0.4 V are detected. This relatively high threshold value was set to limit the number of low-energy peaks detected and to avoid false detections due to noise.

From all the detected pulses, a histogram was constructed. This was done by dividing the output pulses by their amplitude into bins of 10 mV. These values were put into a logarithmic scale and normalized. The histograms are displayed in figure 7.6. Two are present because capturing of the SiPM signal was divided into two phases:

1. At first, a number of SiPM pulses over 15 minutes were measured in totally dark conditions. This was done to determine the background noise present at the SiPM and also its DCR. In figure 7.6, this is represented by the histogram on the top.

2. As a second step, an identical measurement was taken with the Plutonium-238 radiation source combined with a scintillation crystal. The scintillation crystal was placed in contact with the SiPM chip, and the radiation source was pointed at the crystal. A schematic diagram of this configuration is in figure 7.3. The resulting histogram of this measurement is at the bottom of figure 7.6.

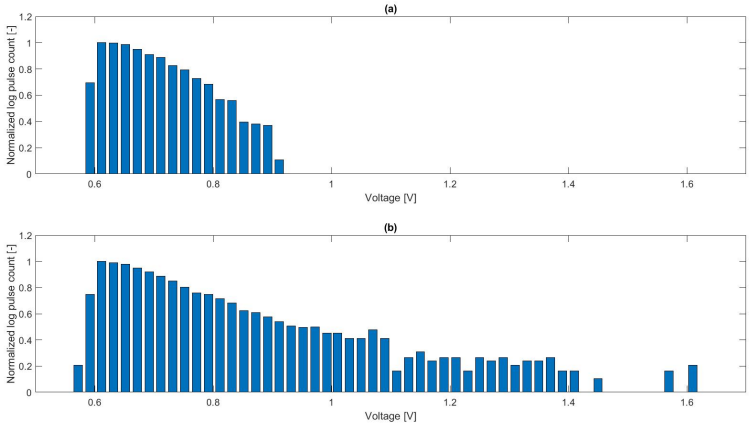

Figure 7.6: Histograms of captured SiPM pulses: **(a)** SiPM background noise, **(b)** SiPM with Plutonium-238 radiation source and scintillation crystal.

If we compare the histograms, the measurement with the radiation source contains a number of pulses with very high amplitude. The biggest one exceeded 1.6 V. These high-voltage pulses are completely absent in the

background noise measurement. Therefore we can attribute these high-energy pulses to the photons that were created in the scintillation crystal as an effect of the gamma radiation. The background noise measurement also contains a significantly lower number of pulses in total. In conclusion, this experiment confirms that the readout system is capable of detecting specific high-energy pulses.

Chapter 8

Conclusion

This diploma thesis aimed to design a readout system for SiPM detectors. In the first chapter, the SiPM's working principle was explored. SPAD's structure was examined, and its equivalent circuit was suggested. Afterward, the equivalent circuit of the utilized SiPM was designed and verified using transient simulation. The waveform obtained this way was very close in shape to the waveform stated by the SiPM's manufacturer.

With a complete equivalent circuit of the SiPM, an extensive simulation of the amplifier chain was carried out. For the first stage amplifier, the stability was examined and assured as a result of properly sizing the capacitance C_f in the feedback loop. The gain was derived from the maximum amplitude of the signal that was expected on the SiPMs output. Because an ADC with purely differential input was chosen, a secondary driver stage had to be added to the amplifier chain. For this stage, a highly integrated amplifier, LMH6653, was chosen.

Next, SiPM readout PCB was designed. A composite material for high-frequency designs, Rodgers 4450F, was chosen as a laminate for the PCB construction. Impedance matching had to be performed for the LVDS traces on the board. Because of this, a 4-layer stackup was chosen, and impedance and length matching was performed for the LVDS interface. The board was also designed to be used in an isolated configuration.

The fifth chapter presented the part of the readout system that was implemented in the FPGA logic. Initially, the FPGA board was modified to allow communication on all four channels available in the readout board. The deserializer logic was implemented using the IDDR2 logic primitives and shift registers for assembling the bits of samples. The communication between the FPGA and PC program is controlled by the FIFO controller block. A rudimentary protocol was developed for the FIFO style communication.

The following part was dedicated to the readout program. It was implemented using C++ language. An object-oriented approach was used to allow for the easy future development of the program. Communication with the readout

system was implemented using the dynamic library provided by the FTDI company. At the end of data capture, the program saves the data of chosen length into a binary file and optionally can call higher language script for further signal processing.

In the last chapter, the prototype of the readout system was presented, and its functionality was verified. The output signal was measured, and the SiPM characteristic pulses were found at the amplifier chain's output. This signal had a larger amplitude than was simulated. A noticeable high-frequency noise was also found in the signal. The proper function of the readout system was verified by finding the characteristic SiPM signal pulses in the data that was saved to a binary file. The bit amplitude of this pulse corresponds to 209 mV, which is approximately the same peak as the pulse captured using the oscilloscope. The proper function of the SiPM was also verified by long signal measurements. SiPM peaks were detected in these measurements and histograms based on their amplitude were constructed. It was verified that the SiPM readout system is capable of detecting specific high-energy pulses. This was done by comparing measured histograms for background noise and for radiation Source Plutonium 238 in combination with scintillating crystal.

8.1 Discussion

During the development of the readout system, multiple complications arose. The most significant problem was the poor performance of the LVDS interface between the two PCBs. The fourth channel was expected not to work at 100 MHz sampling rate from the early stages of the design procedure. However, the communication over the first LVDS channel also did not work. The correct electrical signal was measured at the FPGA pins. Correct routing of the system within the FPGA was also assured. As a result, a faulty LVDS receiver of the FPGA was suspected. However, at this time, this conjecture cannot be verified.

Contrary to the problems mentioned, the development of the readout system was a success. The LVDS communication was successfully tested for DCO speed of 300 MHz on the 2 working SiPM channels. The proper function of the analog amplifier chain was verified by capturing the signal with a high-speed oscilloscope. Finally, the complete system's proper function was confirmed by capturing the characteristic SiPM signal.

In the future, this readout system is intended to be used with a different FPGA board. Therefore at this stage of development, it is not crucial all channels can operate. The proper function of the designed signal amplifier chain and readout system was successfully verified using only two channels.

8.2 Future development

To enable the readout system's full functionality, it must be paired with a different FPGA board. For future development, this should be the first step. It would allow for all four channels' proper function. After this, other minor issues with the design could be resolved.

The first of these is that the analog signal measured at the amplifier chain's output contains high-frequency noise. Because of this, an additional filter circuit may be added to the amplifier chain.

Lastly, the system could be modified to fit the particular application where it would be used. For example, the signal processing could be moved to the C++ application to allow for better integration with other programs. As a part of these modifications, the program output should be redirected from the standard console to a logging file to simplify its integration into a higher-level system.

Appendix A

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Appendix B

List of abbreviations

Abbreviation	Meaning
AC	Alternating Current
ACK	Acknowledgment
ADC	Analog-To-Digital Converter
APD	Avalanche Photo Diode
CMOS	Complementary Metal–Oxide–Semiconductor
DCO	Data Clock Out
DCR	Dark Count Rate
ENC	Encode
FIFO	First In First Out
FPGA	Field Programmable Gate Array
FTDI	Future Technology Devices International
GBP	Gain Bandwidth Product
IC	Integrated Circuit
IDDR	Input Double Data Rate
IO	Input Output
IP	Intelectual Property
LDO	Low Drop Out Regulator
LIDAR	Light Detection and Ranging
LVDS	Low Voltage Differential Signal
PC	Personal COmputer
PCB	Printed Circuit Board
PDE	Photon Emission Efficiency
PMT	Photo Multiplier Tube
PSRR	Power Supply Rejection Ratio
SPAD	Single Photon Avalanche Diode
SPI	Serial Peripheral Interface
SPICE	Scientific Personal Integrated Computing Environment
SiPM	Silicon Photo-Multiplier
TOF-PET	Time of Flight Positron Emission Tomography
TTL	Transistor-Transistor-Logic
USB	Universal Serial Bus

Appendix C

Structure of attached files

```
attached_files
├── adc_reg_write
├── readout_board
│   └── kicad_project
├── readout_program
│   ├── build
│   ├── matlab
│   └── lib
└── verilog
```