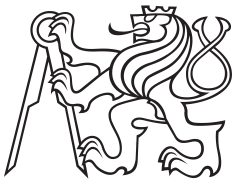
Master Thesis



Czech Technical University in Prague

F3

Faculty of Electrical Engineering
Department of Microelectronics

High Voltage Pulse Generation for CMTI Testing

Bc. Tomáš Nekvapil

Supervisor: Ing. Vít Záhlava, CSc.
Field of study: Electronics and Communication
Subfield: Electronics
August 2022

TEXAS INSTRUMENTS
DEUTSCHLAND GmbH
Personalabteilung
Haggertystraße 1 • D-85356 Freising

MASTER‘S THESIS ASSIGNMENT

I. Personal and study details

Student's name: **Nekvapil Tomáš** Personal ID number: **466138**

Faculty / Institute: **Faculty of Electrical Engineering**

Department / Institute: **Department of Microelectronics**

Study program: **Electronics and Communications**

Specialisation: **Electronics**

II. Master’s thesis details

Master’s thesis title in English:

High Voltage Pulse Generation for CMTI Testing

Master’s thesis title in Czech:

Generování vysokonapěťových pulzů pro testování CMTI

Guidelines:

1. Get acquainted with the issue of generating high voltage pulses and the methodology of Common Mode Transient Immunity (CMTI) testing.
2. Design a solution for generation of high voltage pulses with a possibility of slew rate variation.
3. Design a printed circuit board.
4. Verify the system functionality.
5. Evaluate the achieved results.

Bibliography / sources:

1. Bluhm, Hansjoachim: Pulsed Power Systems: Principles and Applications, Springer Science & Business Media 2006
2. Vobejcký J., Záhlava V.: Elektronika - součástky a obvody, principy a příklady, Třetí rozšířené vydání, Grada Publishing, Praha 2005
3. Záhlava, V: Návrh a konstrukce desek plošných spojů, BEN, Praha 2011
4. Datasheets and Application Notes of used electronic components

Name and workplace of master’s thesis supervisor:

Ing. Vít Záhlava, CSc. Department of Microelectronics FEE

Name and workplace of second master’s thesis supervisor or consultant:

Date of master’s thesis assignment: **19.01.2022** Deadline for master's thesis submission: **20.05.2022**

Assignment valid until: **30.09.2023**

Ing. Vít Záhlava, CSc.	prof. Ing. Pavel Hazdra, CSc.	prof. Mgr. Petr Páta, Ph.D.
Supervisor’s signature	Head of department’s signature	Dean’s signature

III. Assignment receipt

The student acknowledges that the master’s thesis is an individual work. The student must produce his thesis without the assistance of others, with the exception of provided consultations. Within the master’s thesis, the author must state the names of consultants and include a list of references.

. | Date of assignment receipt | Student’s signature

Acknowledgements

I would like to thank my supervisor, Ing. Vít Záhlava, CSc., for his effort and provided guidance, that helped me in the process of creating this thesis. Also I would like to express my gratitude to Texas Instruments for allowing me to work on this project and providing me with the necessary support to complete it. Special thanks goes to Mr. Luke Goetzke for his mentorship during my time at Texas Instruments. Most of all, I would like to thank my family, friends and most importantly my wife for their unwavering support throughout my studies.

Declaration

I hereby declare that I created the presented thesis independently and that all used sources are quoted in accordance with the Methodological instructions that cover the ethical principles for writing an academic thesis.

In Prague, 14. August 2022

Prohlašuji, že jsem předloženou práci vypracoval samostatně a uvedl jsem veškerou použitou literaturu v souladu s Metodickým pokynem o dodržování etických principů při přípravě vysokoškolských prací.

V Praze, 14. August 2022

Abstract

The goal of this thesis is to design a solution that would allow to generate voltage transients with the possibility of changing slew-rate, in order to validate the performance of isolated analog to digital converters.

This solution will be used to characterize the maximum allowable slew-rate that the tested isolation barrier can withstand between the grounds of the device as a part of the standardized Common-Mode Transient Immunity test, CMTI.

It was therefore necessary to design, assemble and verify a system that consists of two printed circuit boards, mother board and daughter board, which will be responsible for the generation of variable slew-rate voltage pulses.

Keywords: ADC, CMTI, Isolation, testing, Pulse, Variable Slew-Rate, MOSFET, SiC, Driver, half-bridge

Supervisor: Ing. Vít Záhlava, CSc.

Abstrakt

Cílem této práce je navrhnutí systému, který bude generovat napěťové pulzy s variabilní rychlostí přeběhu. Ten bude použit k ověření vlastností izolovaných analogově-digitálních převodníků.

Tento systém bude sloužit k charakterizování izolační bariéry, konkrétně k testování Common-Mode Transient Immunity, CMTI. Tedy ověření schopnosti odolat náhlým napěťovým přechodům, přicházejícím mezi oddělené země daného zařízení, s určitou rychlostí přeběhu.

Budou tedy navrhnuty, osazeny a otestovány dvě desky, základní a dceřiná deska, které budou zodpovědné za vytváření napěťových pulzů s možností změny rychlosti přeběhu.

Klíčová slova: ADC, CMTI, Izolace, testování, pulzy, proměnná rychlost přeběhu, MOSFET, SiC, Driver, half-bridge

Překlad názvu: Generování vysokonapěťových impulzů pro testování CMTI

Contents

Figures

Tables

List of used shortcuts and abbreviations

Symbol	Meaning (jednotka)
C	Capacitance (F)
I	Electrical current (A)
T	Temperature (°C)
K	Kelvin (K)
P	Power (W)
R	Electrical resistance (Ω)
V	Voltage (V)

Shortcut	Meaning
IEEE	Institute of Electrical and Electronics Engineers
IEC	International Electrotechnical Commission
VDE	Verband der Elektrotechnik, Elektronik und Informationstechnik e.V.
USB	Universal Serial Bus
DC	Direct Current
AC	Alernating Current
PCB	Printed Circuit Board
FEE	Faculty of Electrical Engineering
LDO	Low Drop-Out Linear Regulator
TVS	Transient Voltage Suppression
SPI	Serial Peripheral Interface
I^2C	Inter-Integrated Circuit
ADC	Analog to Digital Converter
CMTI	Common-Mode Transient Immunity
LED	Light Emitting Diode
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
GaN	Gallium Nitride
SiC	Silicon Carbide
Si	Silicon
RMS	Root Mean Square
WBG	Wide-BandGap
GaAs	Gallium Arsenide
CTR	Current Transfer Ratio
PC	Poly-Carbonate
DUT	Device under Test
BNC	Bayonet Neill–Concelman Connector
HEMT	High Electron Mobility Transistor

Chapter 1

Introduction

Isolated data converters are an essential part of today's electronic devices. They offer protection against unexpected events such as voltage transients, which could harm or even destroy sensitive electronics that may be responsible for critical functions of the system. The power semiconductor market is experiencing rapid growth, and can often make use of high voltage or high frequency switching semiconductors. The interference caused by the rapidly changing currents and voltages in these systems can pose a challenge to the system designer, thus increasing the demand for isolated products and isolated testing.

It is then essential, when designing such a system, to choose the desired parts carefully and it is the job of the semiconductor manufacturers to provide sufficient information about their parts and therefore characterize them thoroughly. One of the important characterization parameter is the Common-Mode Transient Immunity test, CMTI. This metric measures the ability of the IC's isolation barrier to withstand certain slew-rate of voltage transient across its isolation barrier, while if exceeded the device may temporarily lose function.

The goal of this thesis is to design a solution that would allow a user to generate these transients with the possibility to change slew-rates and therefore validate the performance of tested device, in this case isolated ADCs. In the first part of this thesis, the theoretical background about types of isolated data converters will be presented alongside with the parameters that characterize the barrier. As the key element of the system is a high voltage transistor, different high voltage transistor technologies will be discussed and

compared.

In the second part, the overview of the created setup is presented. Then the design of both the layout and schematic of high-voltage fast-transient pulse board, which consists of a larger mother board, and a smaller plug in daughter board, will be described. In the last part, the boards will be assembled and their functioning verified. Lastly, the performance of the daughter board will be evaluated against the previously used solution.

Chapter 2

Theoretical Part

In this chapter, the theoretical side of this thesis will be discussed. Firstly, the matter of galvanic isolation will be introduced alongside a summary of the most used principles of isolation technology within integrated circuits. Secondly the standardized testing and classification of isolation barriers will be defined, including the focus of this thesis, the Common-Mode Transient Immunity test, which will be discussed in further detail.

Lastly, the transistor principle will be described and followed with an overview about new emerging wide-bandgap transistor technologies, including silicon carbide (SiC) and gallium nitride (GaN) MOSFET's for comparison.

2.1 Galvanic Isolation

Galvanic Isolation means a separation of sections of an electrical system that prevents current flow through a direct conductive path. Information can still be exchanged between isolated sections through other means, such as capacitive, inductive or optical. In this section a brief overview of these types will be presented.

Galvanic Isolation is used in the case when two parts of electrical system must remain electrically isolated. A simple example provides one "high-side" or the active side, and a "low-side" or the controller side. An Isolated IC

device that bridges these two sides must still effectively communicate over this isolation barrier, even though the two ground domains could be at very different voltages.

This example may be illustrated with the isolated half-bridge driver shown in fig. 2.1. The goal for the isolator is to shield the controller from any backslash voltage transients that may happen either on the ground or at the gate, which may happen during the change of state of the transistor when high current would be switched. As the grounds are not connected the controller is protected.

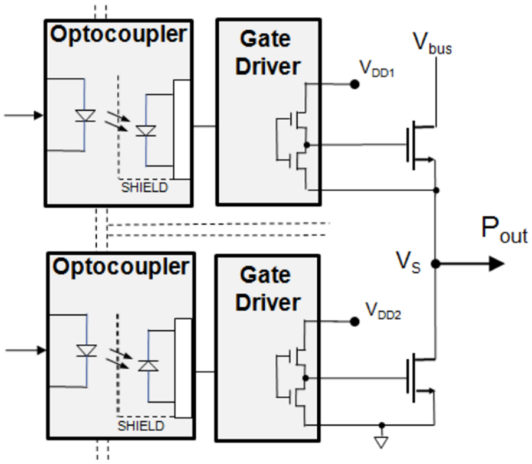


Figure 2.1: Example of the application of galvanic isolation [1]

Generally, isolation is employed whenever there is a need to break ground loops by preventing unwanted current disturbing sensitive circuits in the system. In many cases, this noise generated from high di/dt currents may severely corrupt, damage, or even destroy the sensitive controller and digital processing portion of the system. In many cases galvanic isolation is also used for safety reasons, mainly to prevent accidental currents from reaching ground through a person's body. [2]

2.1.1 Optocoupler

Optical isolators, or optocoupling, is one of the most common and low-cost methods of transferring information through an isolation barrier. Optical isolators are achieving this using beam of light to transmit a signal between separated electrical systems. They usually offer protection against voltage spikes between input and output up to 10 kV, which can prevent destruction

of sensitive electronics.[3] The schematic diagram of an optocoupler is shown in fig. 2.2.

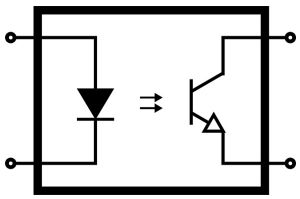


Figure 2.2: Schematic symbol of an optical isolator [4]

The first optocouplers, based on a photoresistor, were introduced in 1968. They are one of the slowest optical isolators, but remain one of the most linear ones, which are still in use in audio and music markets. With the development and commercialization of LEDs between 1968-1970 the opto-electronics market experienced a boom and various different types of optical isolators emerged. [5]

In principle the information is transmitted through a flow of photons. On one side, there is a source of the light, in most cases gallium arsenide, GaAs, light emitting diode (LED), and on the opposite side is a detector, usually in a form of photoresistor, photodiode or phototransistor. The efficiency of an optical isolator is determined with a metric called Current Transfer Ratio (CTR), which describes a relationship between input and output current.

The speed is mainly influenced by the selection of the detector. For a fast transmission of a digital signal, an amplifier is integrated on the chip together with a photodiode. Performance examples of commonly used optical isolators is shown in tab. 2.1. [4]

Table 2.1: Performance of commonly used types of optical isolators with GaAs LED as a source [4]

Type of the detector	CTR Value
Photodiode	0.2-0.3 %
Photodiode and transistor	10-20 %
Phototransistor	10-100 %

There are two physical topologies of these optical isolators, both are shown in the fig. 2.3. These depend primarily on the desired isolation voltage. Devices that have ratings for less than couple of kV usually employ planar structure, when the source lies on the detector and between them, there is a layer of transparent material acting as a photoconductor. This thickness is made as thin as possible, so that the device satisfies the rated voltage. [6]

For higher voltage ratings, optical isolators employ a horizontal architecture, known as a silicon dome. In this case, the source fires the light to a detector, which is placed on the other side of the package. The optical channel, usually made from transparent silicon, retains all the light and redirects it into the sensor. [6]

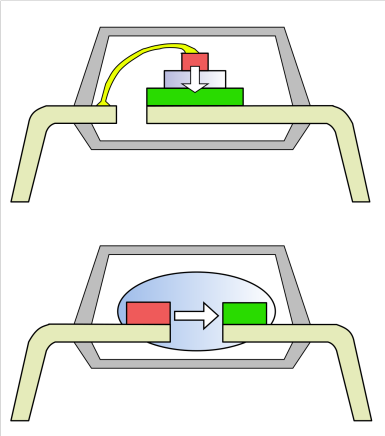


Figure 2.3: Topologies of an optical isolator [6]

2.1.2 Transformer

A transformer is a passive component that uses magnetic flux in order to transfer energy or information from one side of an electrically isolated circuit to the other without the need of the different supply grounds being on the same potential and therefore without direct connection. Since its introduction in the early 1880's, the transformer shaped and enabled the invention and development of various other feats of engineering such as telephone, television or airplane. [7]

Its main purpose is to transform AC voltage. It can convert a high voltage low current electricity into high current low voltage one with minimal loss in energy throughout the process. Nowadays, it has been most commonly used in the electrical grid to transport the energy over long distances, which happens on much larger voltages to lower the conduction losses. [7]

The other major use case for the transformer is also in consumer electronics. In portable power supplies it provides the isolation of the personal device from the grid and therefore provides a protection for the device and its user. They vary in size from small RF transformers to the huge ones used in the electrical grid. [7]

A transformer uses the principle of induced voltage effect in a coil, which is exposed to a changing magnetic flux that is encircled by the coil, known as Faraday's law of induction, which was discovered in 1831, shown in the fig. 2.4. Magnetic flux is generated when any alternating current is passing through a conductor, for example a coil, then the magnetic field will be created and the lines of force look like the ones depicted in fig. 2.5.

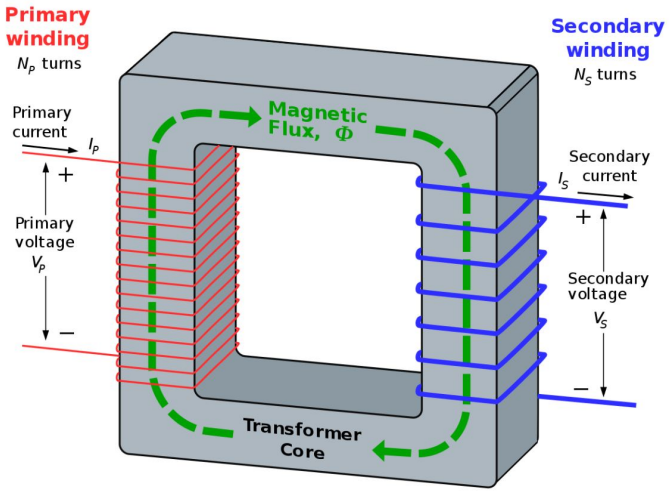


Figure 2.4: Principle of an ideal transformer [8]

The current going through the primary coil creates a magnetic field, the magnetic flux flows through the transformer core and induces a current flow through the secondary coil. The secondary voltage is proportional to the ratio between turns in primary and the secondary. [7] The relationship between the number of coil turns and the voltage on both sides may be written as:

$$\frac{V_P}{V_S} = \frac{N_P}{N_S} = \alpha. \tag{2.1}$$

For $\alpha >= 1$ the transformer is called step-down and for $\alpha < 1$ it is step-up transformer. [8]

To transfer this energy, the transformer requires a core to channel the magnetic flux through. The configuration with the coil and core in a transformer may be seen in fig. 2.4. The current going through the primary coil is inducing magnetic flux flowing through the core, which in return creates voltage at the secondary coil and therefore current. In an ideal transformer the core should have high magnetic permeability and winding inductance to minimize losses. In fig. 2.6, the schematic symbol alongside with the values from eq. 2.1 are illustrated.

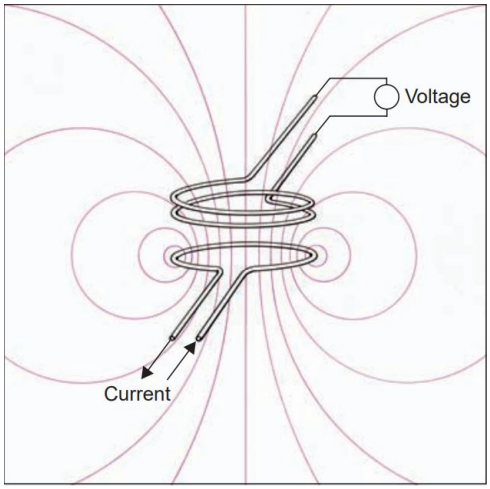


Figure 2.5: Lines of force that describe magnetic field of a coil [7]

The important part of a transformer is also the insulation, as the coils have to be isolated both from themselves and the core itself. This isolation also have to provide tranfer of the heat out of the transformer. The first transformers used oil as an insulator as is doubles as a great coolant. Unfortunately it is flammable, so it gradually started to be replaced with chlorinated polycarbonate liquids, which are fire-retardant, but were later proven toxic and their usage was banned. More recent solutions use air, nitrogen or glass-based insulators. Some other dry-cooled transformers use cast-resin insulation made of polymerizing liquid, that harden into high-integrity solids. [7]

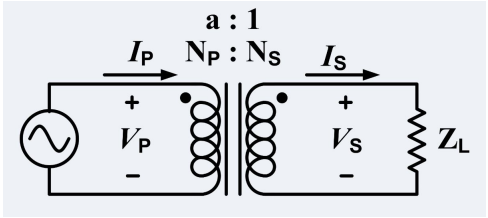


Figure 2.6: Schematic symbol of an ideal transformer [8]

In the fig. 2.7, the difference between integrated versions of capacitive and magnetic based coupling is presented. Transformers provide excellent common-mode transient immunity in contrast to the optocouplers, $100\,\mathrm{kV\,\mu s^{-1}}$ versus $15\,\mathrm{kV\,\mu s^{-1}}$. [9]

Magnetic coupling is also much less dependent on the distance between the coils than capacitor, which will be discussed in section 2.1.3, with distance over its electrodes. This allows for thicker insulation and therefore higher rated isolation capability. Capacitors have also much higher susceptibility to common-mode transients. This may be compensated with differential pair of

capacitors used for the coupling, but that increases cost and size. [9]

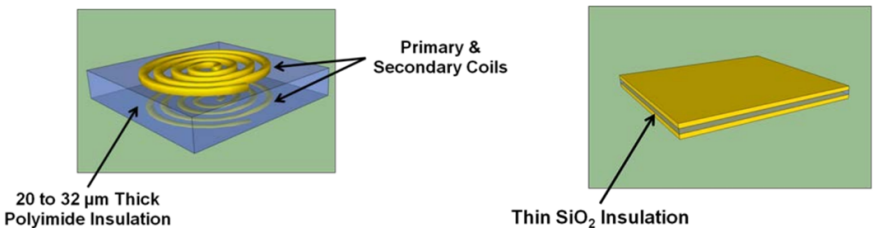


Figure 2.7: Transformer vs. Capacitor based isolators in integrated circuits [9]

2.1.3 Capacitive coupling

Many of today's digital isolators use capacitive coupling to transfer information over the barrier. Capacitors have an inherent nature of blocking DC currents and letting only AC current pass through. Thanks to the relatively small dimensions, isolators using capacitors may be easily integrated into small packages onto an integrated circuit, and thus can be more appealing to many applications. These parts then may be used for example in electric motor drive applications or various power inverter applications.[9]

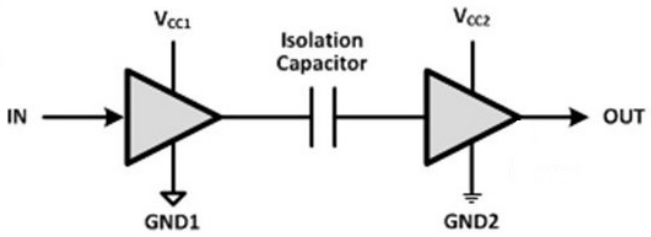


Figure 2.8: Capacitor-based Isolator [10]

A capacitive digital isolator consists of several individual circuits that are shown together with the working principle in fig. 2.9. The incoming input signal is split with an inverter and a buffer into two parallel differential branches representing a differential signal. This is done in order to improve resistance to common-mode transients. [9]

Then comes the capacitor-resistor network, in which the capacitor serves as the isolation barrier. This network transforms the signal into transients, these are then converted into differential pulses with two comparators at the output, which then drive a NOR-gate flip-flop at the output to create desired square wave. For reliability purposes, there is a low pass filter at the output to suppress false changes. [10]

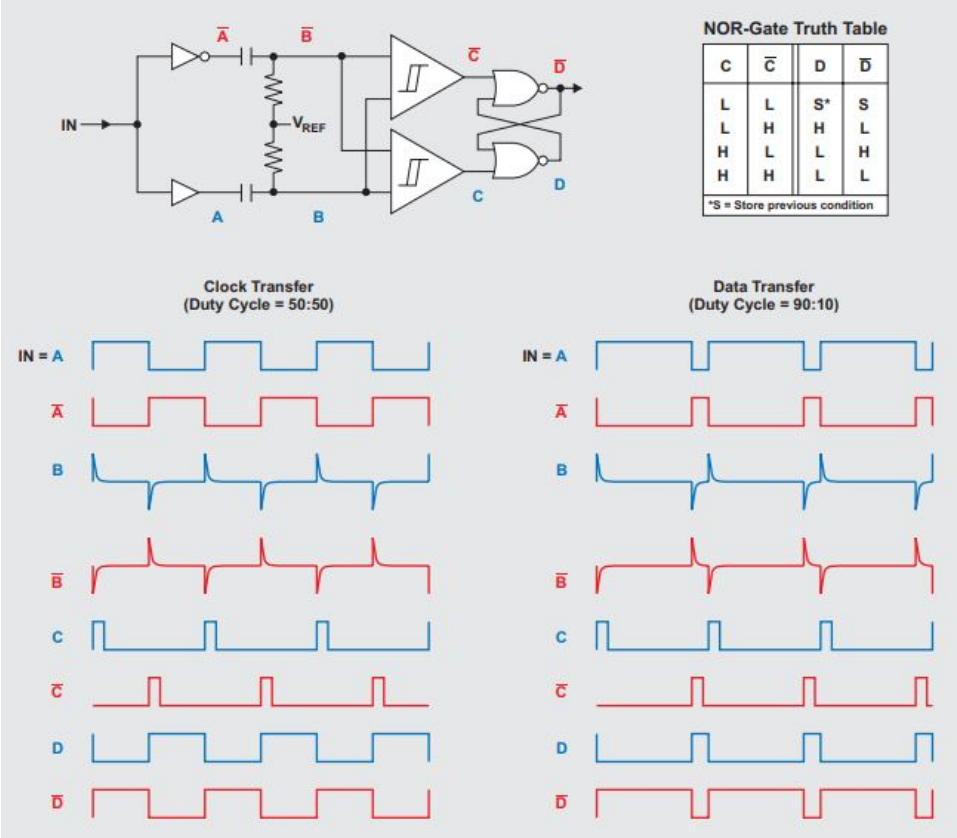


Figure 2.9: Digital isolator using capacitive coupling - principle [10]

To lower the costs and enable manufacturing with existing commonly found materials in a factory. Integrated digital isolators, utilizing capacitive coupling, often use SiO_2 as an insulator between the capacitors nodes. [9]

These capacitive digital isolators are commonly used for high speed data busses like SPI, I^2C, RS-232, RS-485 and other digital signals with speeds up to $150\,\mathrm{MBit\,s^{-1}}$. [10] In comparison with the optocoupler, which is the other common method of isolating digital signals, the capacitive isolators have following advantages: [11]

- Faster propagation time and better parametric stability over supply voltage and over operating temperature.
- Lower failure rate than optocouplers with broader temperature range. The isolation barrier lifetime is also higher than that of optocouplers.
- Provides true only-high or low states. This is linked to their ability to reliably maintain a threshold voltage over time.

- Faster and more precise timing. Other advantages include lower power requirements for operation and better CMTI specifications. [11]

2.2 Key isolation specifications

As described in the previous sections, electrical isolation represents a way of preventing DC and uncontrolled AC currents to travel freely between two separated parts of a system. To transfer signal or power over this isolation barrier, devices use methods described in section 2.1. Isolation may be required in order to protect operators of the device and also to prevent damage to the components inside or even outside of it, for example sensitive processors or precision measurement devices.

There are three different levels for classification of isolation: functional, basic and reinforced. They may be described as: [12]

- Functional isolation - Allows the system to function properly, by for example separating grounds to prevent damage to sensitive components, but does not serve as a shock barrier.
- Basic isolation - When the isolation also provides sufficient protection against the shock, it is called basic isolation. As safety regulations require basic isolation to be supplemented with a secondary isolation barrier to act as a safety guard and providing redundancy. When the second layer is added to a basic one it is then called double isolation.
- Reinforced Isolation - If the two barriers in the double isolation are combined into just one, that has the strength, reliability and shock protection of the two levels of basic isolation, it is called reinforced isolation. Its drawbacks may include for example increased size, reduced coupling, lower efficiency or decreased manufacturing capacity. [13]

When choosing the right digital isolator, it is important to identify the requirements presented by the application and design decisions. With these in mind, it is necessary to understand how to determine the right isolator that is well suited for the intended application. This involves information about the strengths and capabilities of the isolation barrier. It is therefore important to know how to interpret the provided specifications in the datasheet.

High-voltage performance of the digital isolator is determined with the internal layout and materials used. It may be described with the following parameters such as maximum transient isolation voltage, V_{IOTM}, isolation withstand voltage, V_{ISO}, maximum surge voltage, V_{IOSM}, maximum peak repetitive voltage, V_{IORM}, working voltage, V_{IOWM}, and finally common-mode transient immunity (CMTI). These specified parameters represent the ability of the isolator in handling high-voltage stresses, with the different tests representing various scenarios replicating real applications.[14]

2.2.1 Characterization of isolation

All of these parameters represent results of various test profiles that have direct mapping to realistic operating situations, which may happen during the product's lifetime. These definitions and test methodologies are thoroughly defined in the following standards such as IEC 60747-5-5, IEC 60747-5-17, VDE 0884-10 and UL 1577. Test methodologies differ for reinforced and basic isolation, where reinforced are understandably more strict.

2.2.1.1 Maximum transient isolation voltage

The maximum transient isolation voltage (VIOTM) and the isolation withstanding voltage (VISO) intend to quantify the ability of an isolation barrier to handle high voltage applied across the device for very short periods of time. When in normal operational mode, the device sees ideally only up to maximum system voltage that it should be rated for. On the other hand, when any unintentional disturbances to the system happen, either as a result of a failure or external influence, it could bring the voltage across the device to several times higher than the device is rated for.

V_{IOTM} is defined by both IEC 60747-5-5 and VDE 0884-10 as the peak transient voltage that the isolator can handle without breaking down. This may be tested in two different ways. Method A is done during certification and it stresses the isolator on V_{IOTM} fro 60 s, following shorty with partial discharge test at 1.6 times the V_{IORM} for 10 seconds. This is a method that is designed to test the device to breakdown.

Method B is applied in production and it is the non-destructive one. It involves stressing every device at V_{IOTM} for one second followed by partial discharge at 1.875 times V_{IORM}.[15] These waveforms are shown in fig.

2.10. Partial discharge tests localized discharge inside the insulation and it represents the integrity of the insulation.

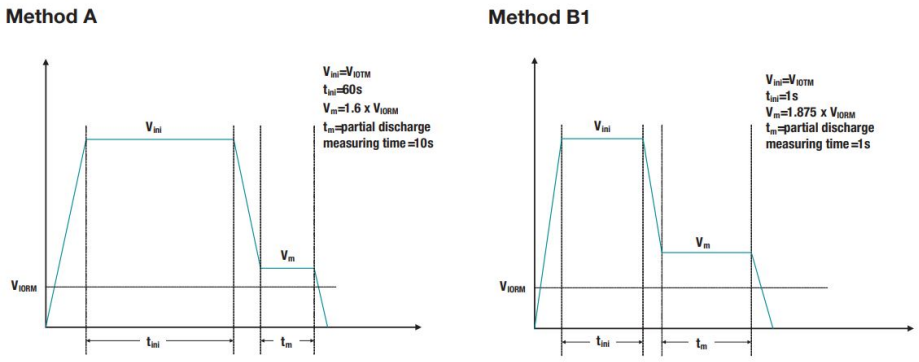


Figure 2.10: V_{IOTM} testing waveform [15]

2.2.1.2 Isolation withstand voltage

V_{ISO} is defined in UL 1577 as the RMS voltage that the isolator can handle without breakdown for 60 s. Testing of this characteristic is done during the certification process with applying a sinusoidal stress of V_{ISO} for 60 seconds. To speed up the testing in production, the device is instead equivalently stressed at 1.2 times VISO for one second. [15] V_{ISO} and V_{IOTM} are equivalent for sinusoidal stress.

2.2.1.3 Maximum surge isolation voltage

The maximum surge voltage is a parameter that describes the ability of a digital isolator to survive high voltage pulses of a certain transient profile, shown in fig. 2.11. Surge voltages in general may be caused by various factors in the lifetime of the device, mainly with the lightning strikes, failures in the system, unexpected short circuit or ESD events. The surge voltage is defined in IEC 60747-5-5 and VDE 0884-10. [16]

An isolator, which is labeled to withstand certain V_{IOSM}, must be able to pass the application of the test waveform with peak voltage of 1.3 times the claimed V_{IOSM} for basic isolation and 1.6 times V_{IOSM} for reinforced one. Also to be called a reinforced isolator, it must pass this surge test at a minimum of 10 kV.

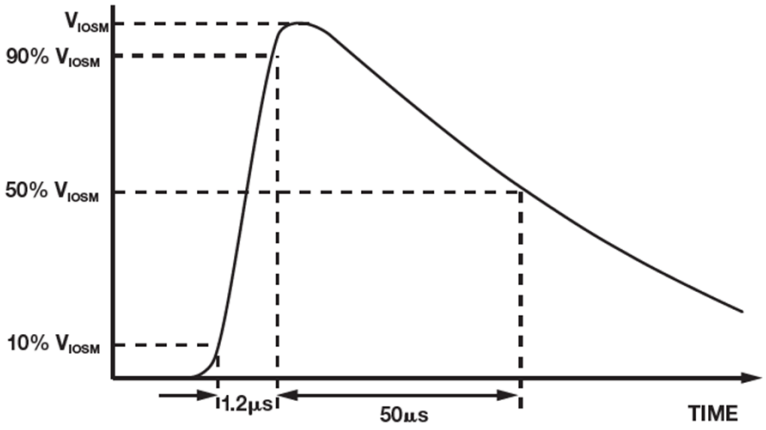


Figure 2.11: Surge test waveform [16]

Surge test may also serve to determine compliance to other system-level standards, which require a certain level of surge capability for a given system voltage such as IEC 61800-5-1.[15]

The factor that has the biggest influence on success rate of this test is the insulation thickness, otherwise known as the Distance Through Isolation (DTI), and the quality of the material. That is because the electric field tends to concentrate at the weakest points of the dielectric. These are centered around the defects as they provide imperfections that the charge can go through. [16]

2.2.1.4 Maximum peak repetitive voltage and working voltage

Together with the working voltage, V_{IOWM}, the maximum repetitive peak voltage, V_{IORM}, provides a way to determine the ability of the isolator to handle high voltage across its barrier on a continuous basis over its lifetime. This may happen in applications that deal with high current and voltage changes, for example gate drivers of the transistors, which may experience this over-voltage event every time, when the transistor is switched.

Both of these parameters are defined in IEC 60747-5-5 and the VDE 0884-10. V_{IORM} is specified as the maximum peak repetitive voltage that the isolator can tolerate. On the other hand, V_{IOWM} is defined as the maximum V_{RMS}, or equivalent DC voltage, that the isolator can withstand over specified longer period of time. If the stress would be sinusoidal, both of these parameters are equivalent. [15]

To test for both of these parameters a partial discharge test, which looks for degradation in the insulation, is performed. The waveform, that is being applied, is depicted in fig. 2.10. It uses both Method A for certification and Method B1 to test during production test. [15]

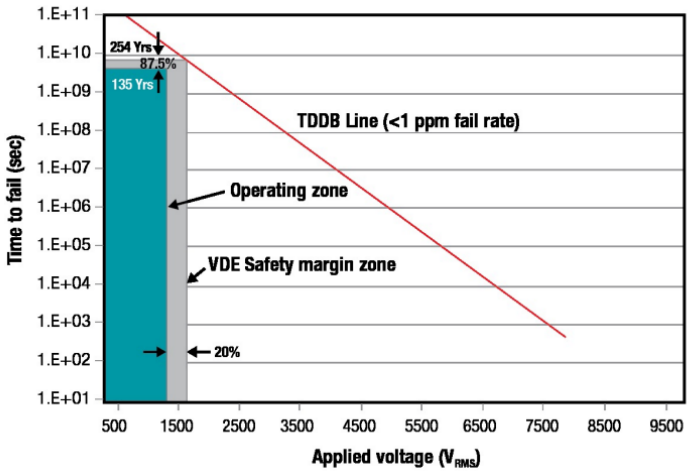


Figure 2.12: TDDB extrapolated result chart [17]

With the second edition of the VDE 0884-10, additional requirements for the V_{IORM} and V_{IOWM} are presented. Manufacturer of devices with reinforced isolation must prove that the part can handle 1.2 times V_{IOWM} or V_{IORM} for more than 37.5 years. This is achieved through an accelerated stress test, during which the isolator is exposed to varying levels of high voltage and corresponding times to breakdown are recorder. [18]

These results are logged and then represented on a voltage-versus-time curve and then extrapolated to predict the behavior of the device over its lifetime. This may be seen in fig. 2.12. The Time Dependent Dielectric breakdown (TDDB) test is used to verify the lifetime of the dielectric. It stresses parts at a constant AC or DC voltage for an extended period of time, usually until failure or severe degradation. [18]

2.2.1.5 Common-Mode Transient Immunity - CMTI

Common-mode transient immunity (CMTI) represents the ability of the isolator to tolerate high slew-rate voltage transients between its two grounds without corrupting the output signal. This distortion may occur as an unexpected change in output voltage for isolators with analog output or a false voltage level in the output waveform of a digital one. Higher CMTI

specification indicates more robust device.

This specification is becoming more and more crucial as the development of the MOSFET transistors advances forward and the new SiC and GaN types of transistors increase the switching performance up to 5 times the di/dt and 2 times dV/dt compared to traditional silicon transistors. This will indirectly impact the gate driver of these transistors and they will experience higher levels of stress compared to the drivers of traditional Si MOSFETs or IGBTs. [19]

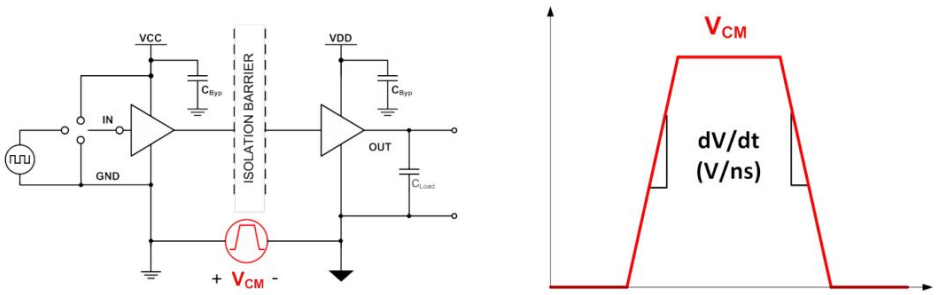


Figure 2.13: Common-mode transient immunity: Simplified setup [19]

CMTI specification is defined as the maximum tolerable rate of rise or fall of the voltage across the grounds of the device under test. These grounds represent two isolated circuits. The results are usually defined in the range of $\mathrm{V\,ns^{-1}}$. In the fig. 2.13, the simplified setup of a CMTI test bench is shown. When the CMTI pulse reaches the DUT, the output of the device must be measured to determine if there has been any disruptions to the signal. [19]

There are two different types of CMTI testing methodology. The first one is the static CMTI, which tests the reaction of the device when driven with static defined, non-moving inputs. Deviations from the determined output are then observed in the time window of the CMTI pulse. The threshold for CMTI failure is different for each type of the device. For example gate drivers define the CMTI fail event as observing deviation of more that 20% of the V_{DD} from either logic level. This methodology may be also used to test analog output isolators and it is illustrated in the fig. 2.14. [19]

The second testing methodology is the dynamic CMTI. In this case the device under test has its inputs being switched from high to low. The switching is centered so that it happens at or near the point of the rising or the falling edges of the CMTI input pulse. The passing criteria remain the same as with the static test, so the device should follow the input.

The failures to look for are, for example, missing pulses, excessive propa-

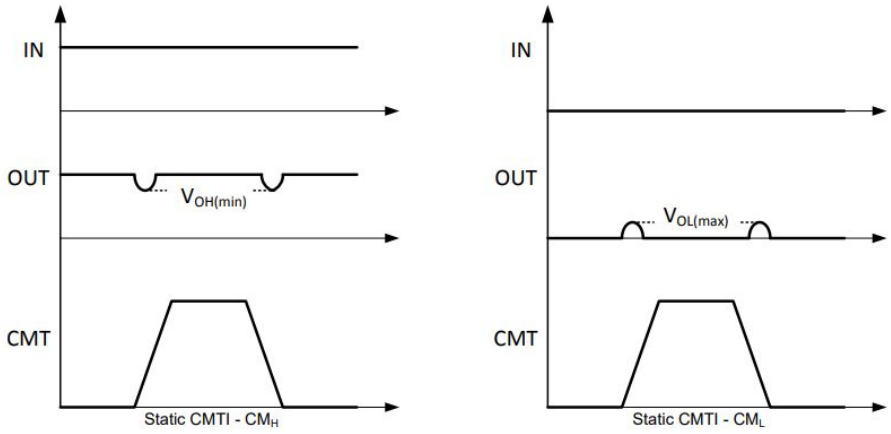


Figure 2.14: Static CMTI test waveform [19]

gation delays, different latches of the output and so on. Examples of these states are shown in fig. 2.15. In the case of isolated data converters, static CMTI may not apply, as the device may be continuously converting and only dynamic CMTI applies as a specification. [19]

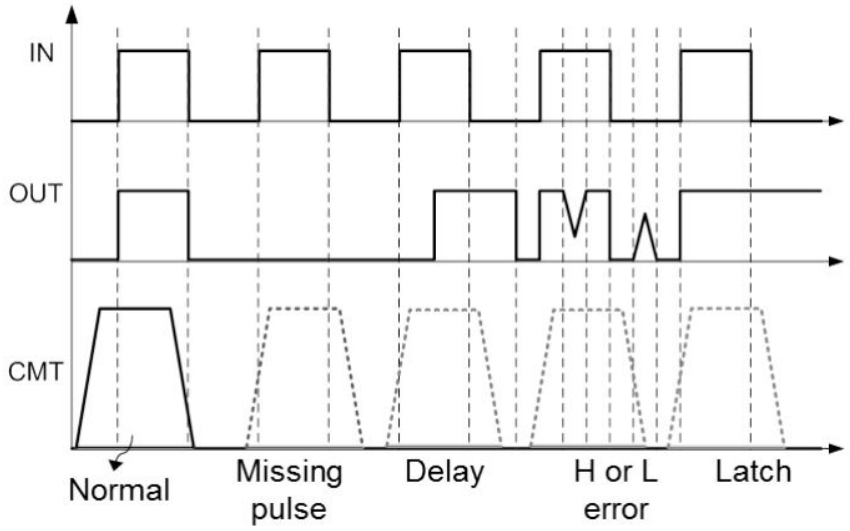


Figure 2.15: Dynamic CMTI test waveform [19]

Even though the VDE 0884-10 recommends measuring slew-rate at 10% to 90% of the common-mode voltage of the pulse, this approach may not be representative as the performance in the upper and lower regions of the pulse's edge is hugely influenced by the parasitics of the board and the generator, for example the capacitances of the MOSFETs generating the pulse. Therefore the slew-rate calculation would not represent the real value that the device experiences. [19]

To illustrate this, waveform, from the early evaluation of this thesis's pulse board performance, is presented the fig. 2.16. The slew-rate noted with the cursors representing the value for the 20% to 80% calculated from the V_{pp}. It may be observed that, when the measurement would be taken at recommended 10% to 90% of the common-mode voltage, the lower part of this waveform would have an influence on the final value.

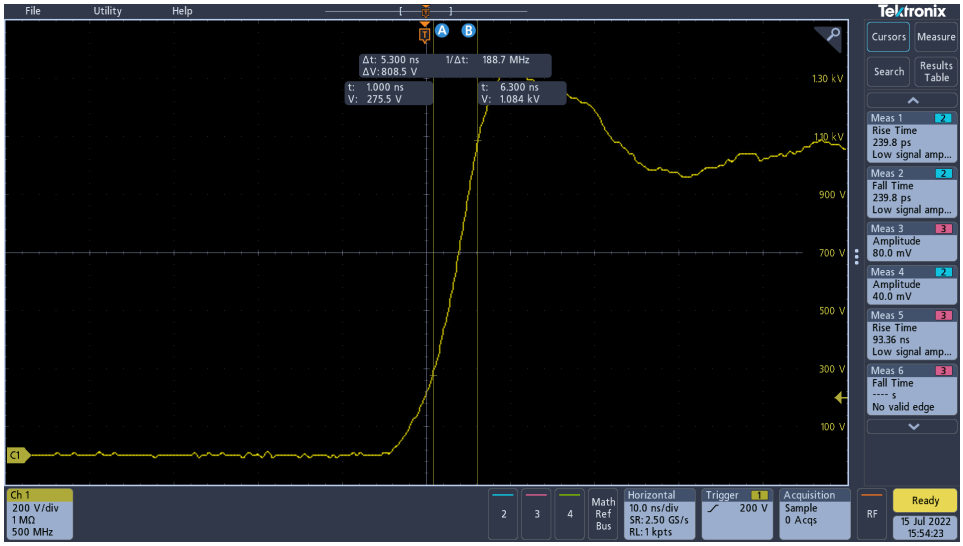


Figure 2.16: CMTI Pulse Rising Edge

For example, measurement at 20-80% of the peak voltage is in this case approximately $150\,\mathrm{V\,ns^{-1}}$. When the slew-rate would be taken at 20-80% of common-mode voltage, the value lowers to circa $130\,\mathrm{V\,ns^{-1}}$. If the slew-rate would be measured according to the VDE standard from 10-90% of the common-mode voltage, it could lower the result as low as $90\,\mathrm{V\,ns^{-1}}$. This means that the result would not be representative of the device's true performance. Therefore it was decided to measure the slew-rate at the 20-80% of the pulse's peak voltage.

2.3 MOSFET Transistors

Metal-Oxide-Semiconductor Field-Effect-Transistor, or MOSFET for short, is a common transistor that has its conductivity between source and drain controlled by an electrical field, which is induced by applying voltage between the gate and source nodes. The isolation between the channel and the gate is provided usually with a SiO_2. MOSFETs then allow switching or amplification of a signal, which is controlled with voltage rather than current as is the case with Bipolar Junction Transistors, or BJTs for short. [4]

Using this principle allows them to use much less power to switch the same signal. Therefore they can achieve much higher integration density or lower the total input power required for the system operation. This has been regarded as the biggest advantage of the MOSFET transistors. There are two major types of MOSFETs enhancement-type and depletion-type.[4]

If the transistor is of the enhancement type then, when the voltage is applied between source and gate terminal, there is an increase in conductivity with rising voltage. These are often referred to as normally-off transistors. On the other hand, for the depletion mode transistors, when voltage is applied at the gate, the conductivity decreases. This may be also called normally-on type. [4] The schematic symbols may be seen in fig. 2.17.

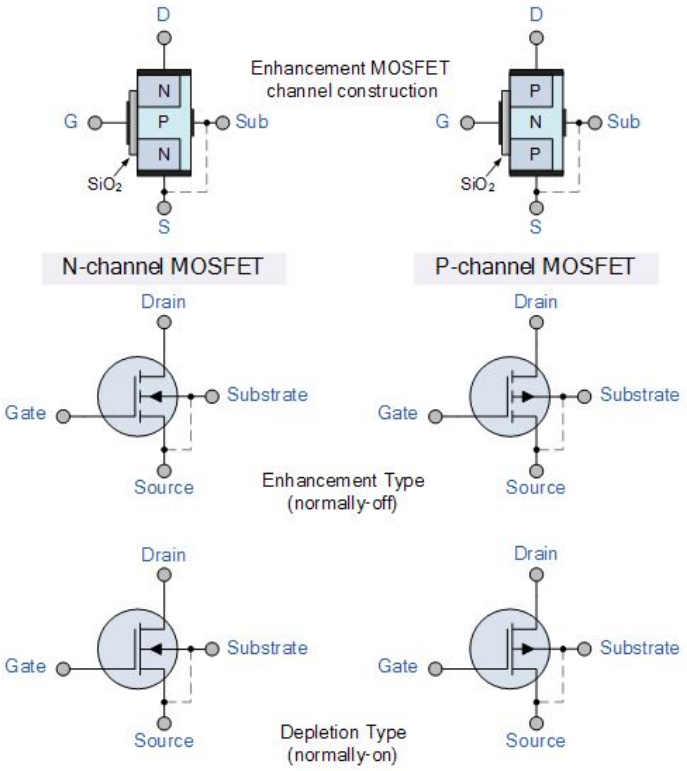


Figure 2.17: MOSFET transistor: Depletion vs Enhancement type [20]

MOSFETs may be build as either N-types or P-types, depending on the polarities of the bulk, source and drain regions as depicted in fig. 2.18. In the case of the N-type, otherwise known as NMOS, the majority of carriers are electrons. The device is built on a p-doped silicon substrate with regions of n-typed doped material, which are created using ion implantation. The n-type regions are called source and drain. This situation is reversed in the case of the P-type transistor, known as PMOS, which uses holes as the majority carrier.[21]

The region between the source and drain underneath the gate is called the channel. It represents the place where the conductivity region is formed and the electrons may travel through. Above this channel there is a thin layer of insulator, formed usually out of the SiO_2. It isolates the channel from the gate terminal which sits on top of it. This creates the three terminal structure of the MOSFET, shown in fig. 2.18. [21]

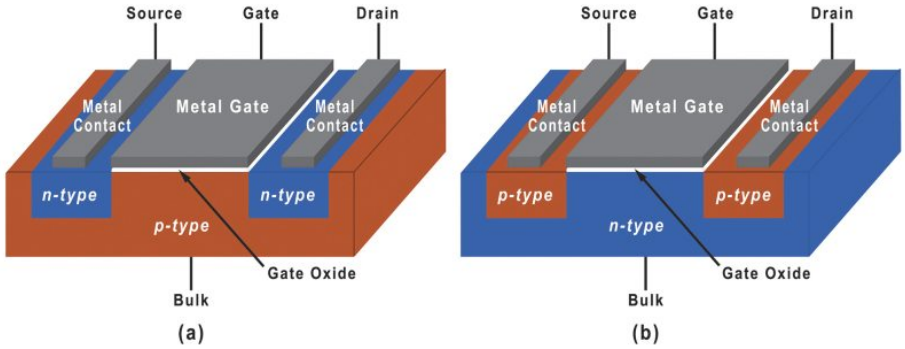


Figure 2.18: MOSFET transistor: P-type (b) vs N-type (a) [21]

The working principle is illustrated in fig. 2.19. The inner mechanics and functioning of the MOSFET transistor is given with the behavior of the capacitor formed around the thin insulation layer between the gate terminal and the doped substrate, which should be connected, for the n-type MOSFET, either to the source terminal or the lowest potential in the integrated circuit. [4]

With the context of the NMOS transistor, the basic operating principle is shown in fig. 2.19. In the part (a) the device is in its "off" state with all terminals at 0 V and the bulk is connected to the ground. There are two P-N junctions between to n-type source or drain an the bulk p-type substrate.

When a small voltage is applied between the gate and source terminals, the field induced by this voltage repels the charge carrying holes away from the substrate surface. When V_{GS} reaches the threshold voltage the region under the gate terminal becomes almost depleted, which forms an area know as the depletion zone.

If the voltage across the gate and source is increased above this threshold, the electrons are attracted from the electron-rich areas of source and gate into the region under the gate electrode, producing an n+ region that is called inversion layer. This is shown in the (b) part of the fig. 2.19. This inversion layer forms a conducting channel, which bridges over the two n-type areas of drain and source and allows the electrons to flow according to what polarity is the drain-source voltage. [21]

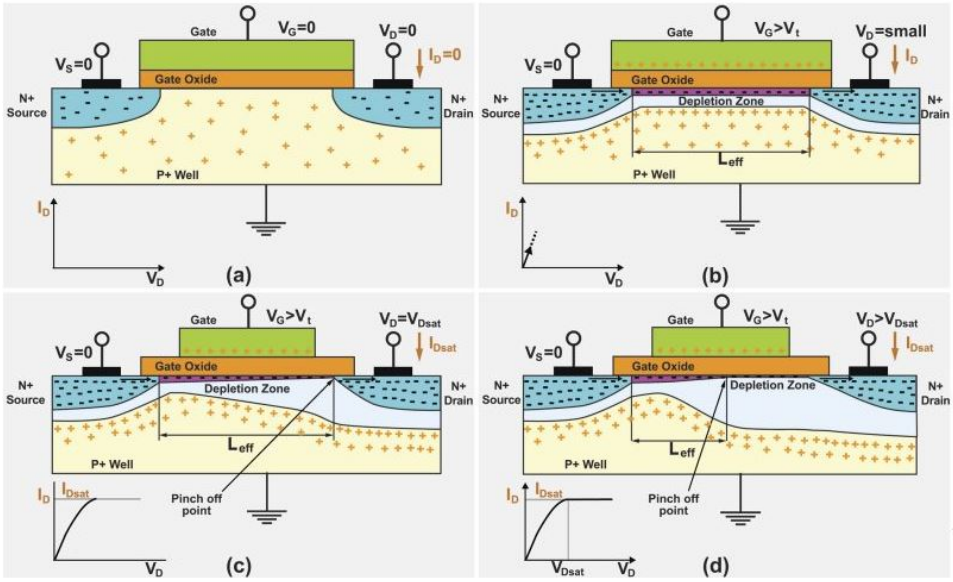


Figure 2.19: MOSFET transistor working principle [21]

As it is shown in the fig. 2.20, the I-V characteristic of a N-MOSFET, when applying small drain to source bias voltage in the above threshold conducting state the electrons may move in the inversion layer between drain ans source. When the values of V_{DS} are relatively small the the characteristic is close to linear and the current going through the transistor increases with the voltage across drain and source.

When the V_{GS} is altered, the concentration of the electrons in the inversion layer is changing and therefore the conductivity is different, which leads to a change in the current through the transistor. This is presented in fig. 2.20 with the multiple curves for different gate voltages. [21]

If the drain source voltage is increased above other threshold, known as the saturation voltage of the channel, depletion zone and the inversion layer starts to change. The conduction characteristic starts to change as with the rising V_{DS} the current is not following anymore. The inversion layer on the drain side is becoming thinner and eventually disappears. This phenomenon is known as a "pinch-off" and the point of the inversion layer disappearing at the gate is called "pinch-off point". This change is illustrated in the (c) part of fig. 2.19.

The pinch-off appears because, when the voltage across the drain and sources reaches V_{SAT}, the effective potential between the gate and the substrate at the source is greater than the one between the gate and the substrate at the drain end of the channel. If the voltage is turned up beyond V_{SAT}, the

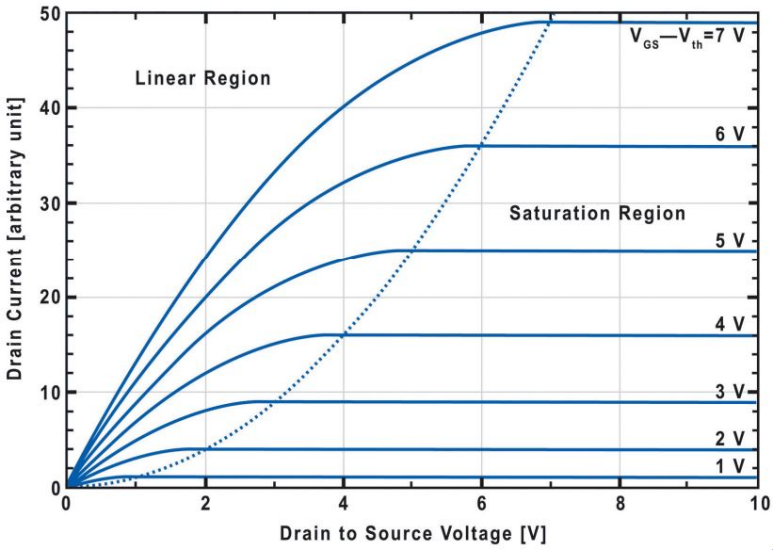


Figure 2.20: N-MOSFET I-V characteristic [21]

pinch-off point is moving away from the drain, reducing the channel length as shown in the part (d) of the fig. 2.19. At this point the current through the transistor is controlled solely with the gate voltage. [21]

With a standard Si MOSFET principle described, the next sections will be focusing on modern wide-bandgap transistors that provide unique capabilities in terms of drain-source voltage and the switching speed.

2.3.1 Wide-bandgap devices

The majority of today's power electronics applications, with voltage ratings between 1.2 kV and 6.5 kV, is dominated by silicon IGBT transistors, which were developed almost 30 years ago. As their performance have been improved and developed for a long time, the next step in device performance would require both material change and a new device structure. The promising device group are the wide-bandgap (WBG) semiconductors with the likes of silicon carbide (SiC) or gallium nitride (GaN). Due to their intrinsic material properties, these semiconductor devices have potential to be, or in some way already are, superior than their Si counterparts.[22]

These properties include: [22]

- Wider energy bandgap - results in much lower leakage currents and

significantly higher operating temperatures.

- Higher critical electric field - results in the blocking layer of WBG devices being comparatively thinner and with higher doping concentrations - this results in huge reductions in on-resistances.
- Higher electron saturation velocity - impacts the switching speed, which is comparably higher than the Si counterparts.
- Higher thermal conductivity - this improves the ability to remove heat from the silicon to the package and allows operation in higher power densities.

These characteristics are quantified in tab. 2.2.

Table 2.2: Summary of the key material properties of semiconductors [22]

Parameter	Si	4H-SiC	GaN
Energy bandgap, $E_g(eV)$	1.1	3.3	3.4
Critical electric field, $E_c(\mathrm{MV\,cm^{-1}})$	0.25	2.2	3
Electron drift velocity, $v_{sat}(\mathrm{cm\,s^{-1}})$	$1 \cdot 10^7$	$2 \cdot 10^7$	$2.2 \cdot 10^7$
Thermal conductivity, $\lambda(\mathrm{W\,cm^{-1}\,K^{-1}})$	1.5	4.9	1.3

For these reasons the WBG devices are considered as one of the future replacements and promising step forward in the development of semiconductor devices for power applications. With especially SiC MOSFETs edging out IGBT transistors in application like DC/DC converters for solar technologies, on-board chargers for EVs and other power application in the 1 kV - 3 kV range. Where their high power capability, high switching frequency, low switching losses and high temperature tolerance is providing an edge over traditional Si based semiconductors. [23]

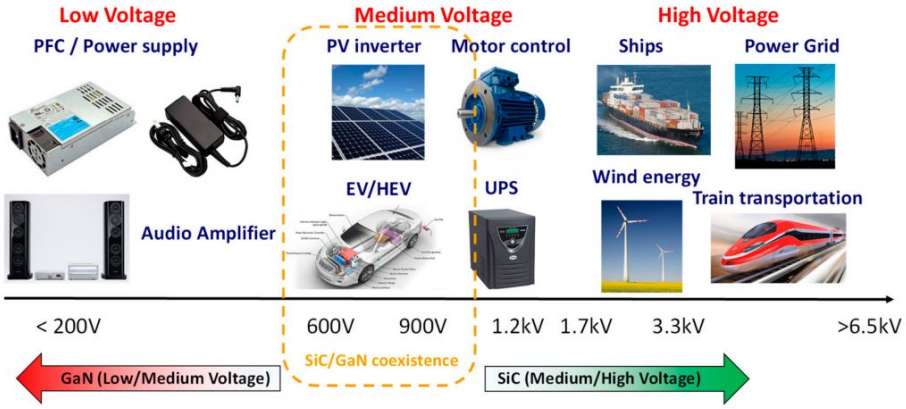


Figure 2.21: Applications of new WBG semiconductor devices [24]

In the fig. 2.21, the possible applications for each presented wide-bandgap power device are shown. The main potential market for the GaN based HEMTs presents the low to medium voltage range of applications, which may include consumer electronics, like for example power supplies, audio amplifiers. They may also compete with SiC transistors in the field of solar inverters as the voltages around 600 V fall into both of these WBG devices categories.

2.3.1.1 SiC MOSFET

The SiC devices have been around for more than 20 years with Cree launching first SiC Schottky diode back in 2001. This validated the feasibility and intensified the research and development efforts. The key roadblock to serializing SiC MOSFET production was the reliability of the gate oxide, which, in the early samples and first generation of the SiC devices, produced poor results and may have discouraged some. But in later years, these obstacles were overcome and various newer types of SiC transistors emerged. [22]

The key advantage of silicon carbide as a semiconductor material is derived from the fact that the bonds between the atoms are much stronger. This characteristic is quantified in the tab. 2.2. The main feature is the critical electric field which enables the design of transistors with much lower on-resistances and smaller parasitic capacitances for the same blocking voltage as the traditional ones. [25]

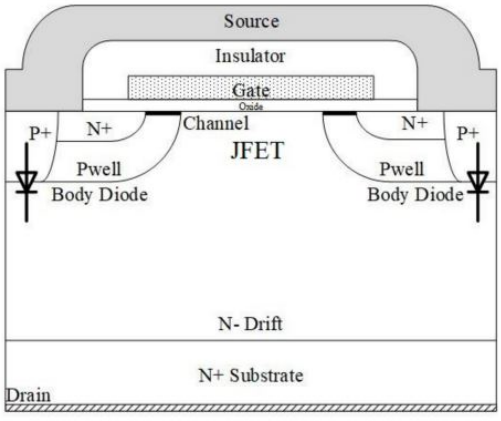


Figure 2.22: Cell structure of SiC MOSFET [23]

Compared with the silicon one, SiC MOSFETs have higher bandgap, high thermal conductivity and high saturation speed. This makes them more

suitable for high voltage, high temperature and high switching frequency applications. SiC devices are available commercially in voltage ranges of up to 1.7 kV. This makes them ideal for switching application in around 1 kV like automotive on-board chargers and converters in solar applications.

In the fig. 2.22, the cell structure of an commercially available SiC MOSFET from Cree is shown. It is a vertical structure, with the source being on top, while the drain is at the bottom of the device in contact with the N+ substrate region. Alongside with the source electrode, there is also a gate terminal underneath the source, separated with an insulator. The channel is located in the P-well regions nearest to the gate terminal and between the N+ source region and N- drift region. The P regions around the source and N- drift region form the MOSFETs body diode with their P-N junctions. [23]

2.3.1.2 GaN MOSFET

Gallium Nitride, GaN, field effect transistors are wide-bandgap semiconductors whose stable crystalline structure is the hexagonal wurtzite. As described in tab. 2.2, GaN transistors have even wider energy bandgap than SiC semiconductors and that results in intrinsic carrier concentration that is several orders of magnitude higher than of the silicon ones. Because of that, GaN devices should have much lower leakage currents and much higher operational temperature.[24]

As the critical filed value is way higher, so is the maximum reachable breakdown voltage, which makes them promising devices for high-voltage applications. The higher maximum breakdown voltage also means that transistors with thinner drift layers may be manufactured, which means significant reduction in on-resistances with respect to Si devices. This also indirectly impacts the efficiency as more compact devices lead to minimized static and dynamic losses. [24]

On top of that, due to the high saturation electron velocity of the material, the GaN switches have a potential to reach much higher switching frequencies as both their SiC and Si counterparts. This is also due to the presence of two-dimensional electron gas (2DEG) layer in AlGaN/GaN heterostructures, which has electron mobility values over $1000\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$. [24]

The presence of the 2DEG in GaN-based heterostructure makes HEMT devices normally-on by nature. The layer is acting as conduction channel,

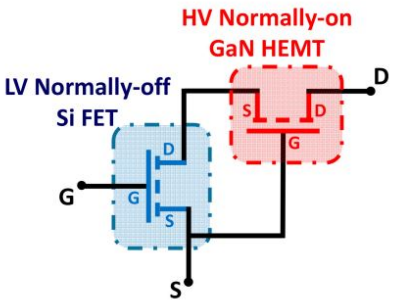


Figure 2.23: Cascode configuration of normally-off GaN device [24]

which means that the current will flow between the drain and source even at 0 V gate bias voltage. Although using normally-on HEMTs is possible, in power application for safety reasons the normally-off device are preferred. This lead to the development of a configuration that would provide the normally-off functionality, as the demands of today's market are leaning towards it.

Nowadays, there are few solutions overcoming this to create normally-off GaN transistor. The first is the "cascode" configuration, which is obtained when GaN normally-on transistor is combined with normally-off Si traditional MOSFET. This configuration is showed in fig. 2.23.[24]

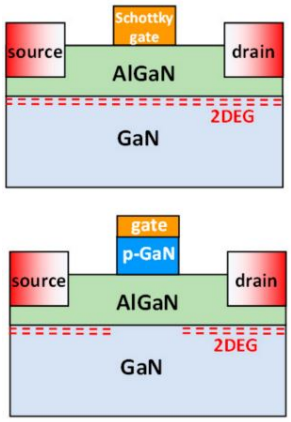


Figure 2.24: Normally-on GaN HEMT (a) and normally-off HEMT with p-GaN gate (b) [24]

The standard Si transistor's purpose is to control the gate source voltage across the GaN. In this way, when voltage is applied to the Si FET, the drain-source voltage of the GaN is zero, which means that the device is on. On the other hand, when this gate voltage is removed, Si MOSFET is turned-off and the applied negative bias will create negative voltage between the gate and source electrodes of the GaN, which will force the GaN transistor to turn-off.[24]

The limitations of this approach are in the addition of the Si transistor. It adds complexity to packaging, increases parasitics and moreover high temperature operation is limited because of it. To overcome these disadvantages, true normally-off GaN is in development. The p-GaN Gate is one of the most promising solutions to achieve this. The structure of a normally-on and normally-off GaN transistor, using this approach, is shown in fig. 2.24. [24]

In this case, the p-GaN layer is placed on the AlGaN/GaN heterostructure under the gate contact region. The p-GaN layer lifts up the band diagram, which results in the depletion of the 2DEG channel underneath the region even in the absence of the externally applied gate bias voltage. This makes the transistor switched off in default state. The p-GaN HEMT is in fact the only "real" normally-off GaN HEMT technology that is commercially available on the market to date. [26]

Chapter 3

Practical Part

This chapter will focus on realization of the pulse board, whose main purpose is to generate voltage pulse of desired slew-rate. It will reach the tested device on dedicated DUT board that the pulse board is to be mated with. The pulse board will consist of two separate PCBs, the mother board, which forms the platform that houses necessary safety and power circuits, and the daughter board, which is designed as a half-bridge switch module.

First part of this chapter will show high level overview of the whole setup used for the CMTI testing. Then design of each board will be thoroughly described with presenting the schematics and individual circuits, followed by a section focusing on the layouts. In the next chapter, these boards will be evaluated and compared against an integrated half-bridge module that is a part of the previous solution.

Schematic design is a first step in the process of making a PCB, where the designer defines the connections between different parts of the circuits to control their interactions and gain the required function, which the board should provide. For the design of these PCBs, Altium Designer 22 was used as it provides excellent functions and capabilities to make the PCB design process effective.

3.1 Overview of the setup

In this section, high-level overview of the setup, that is being used to test Common-Mode Transient Immunity, will be shown in order to provide background for the CMTI testing procedure and for further design decisions.

In the fig. 3.1, the high level overview of the CMTI setup is presented. It makes use of various laboratory equipment alongside with software control to automate the measurements. It makes the data collection efficient as many samples must be collected and processed. Setup is controlled from the PC via control software, which commands bench instruments to form a test sequence and acquire the necessary data.

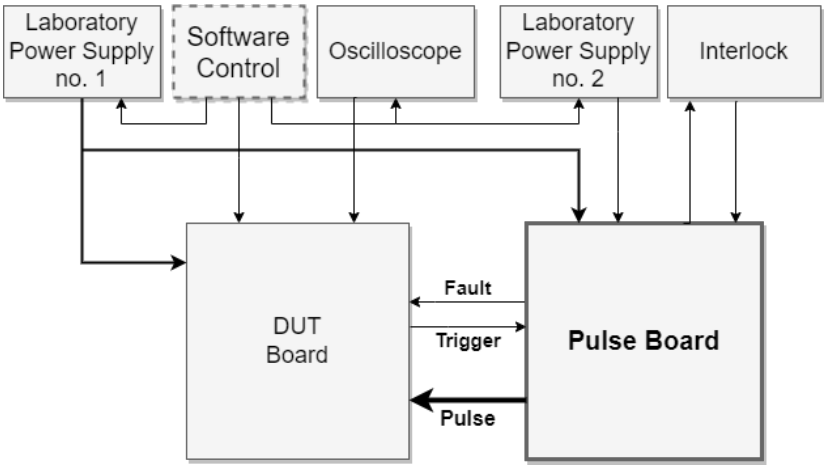


Figure 3.1: High-level overview of the CMTI Setup

All of these blocks together are providing necessary conditions for the device to function properly as well as generate and measure voltage pulses coming between the grounds of the tested isolated device. At the same time, the output of the device under test, DUT for short, is measured to observe any changes that would be induced by applying such pulse. Setup utilizes following equipment:

1. Laboratory Power Supply no. 1 - Provides the main 5 V power to the entire setup. This includes all other auxiliary isolated and non-isolated power supplies as well as all the support circuits on both the DUT board and the Pulse Board.

2. Oscilloscope - Measures the incoming voltage pulse to obtain exact dV/dt impacting the device.
3. Laboratory Power Supply no. 2 - Provides variable input voltage for the high voltage DC/DC present on the Pulse Board. This allows the variation of the high voltage and therefore the slew-rate.
4. Interlock - Comes from mechanical switches on the safety-box in order to detect the accessibility of the board and securely switch-off any higher voltage to protect the user.
5. DUT Board - Device Under Test Board, which serves as a platform to house every necessary circuit to allow the right functioning of the device, which is being tested. This is done in order to test its behaviour, when applying the pulse between its isolated grounds, while in normal operation.
6. Software Control - Using a PC and control software to allow easier data acquisition and processing.

The DUT Board is tailored to the type of the tested device. For the purpose of this thesis, it is assumed that the device under test is an isolated converter with either digital or analog output. With the analog option a voltage on the output is observed in order to detect any changes happening in the window, when the high voltage pulse impacts the device. In case of digital output, the output waveform is analyzed for missing or corrupted bits. In the following chapters, design of the Pulse Board will be presented.

3.2 Mother board

Mother board, also known as the Pulse Board, is responsible for creating a voltage pulse with variable slew-rate or dV/dt. It houses all necessary safety and protection circuits in order to detect the presence of high voltage and safely discharge it when the safety enclosure would be open. There are also control and power circuits, which support the used switch with the right input signal and power. The main requirements for this board are to:

- generate voltage pulses,
- handle voltages up to 4 kV on the high voltage side,
- provide slew-rate variation,

- detection of the applied voltage to provide visual warning,
- utilize discharge circuit to safely discharge capacitors on the high voltage line,
- fit into current setup, so that it can be interchangeable with the current solution,
- provide compatibility for various switches (All-in-one Half-Bridge module and new custom SiC based switch).

Other auxiliary features include for example I^2C expander to provide the ability to read-out the state of the board with the control software and, if needed, interrupt the testing sequence when deemed appropriate.

3.2.1 Overview

In the fig. 3.2, the overview of the circuits on the Pulse Board may be seen. The center of this board is a housing for the switch, which will be discussed later, in section 3.2.2. The connection for the switch is made out of pin sockets, which may fit standard pin-headers to provide interface for current or future modules. Slew-rate is defined as a ratio between difference of voltage divided by the time difference:

$$SR = \frac{\Delta V}{\Delta t} \mathrm{V/s}. \tag{3.1}$$

The board provides variable slew-rate with changing the dV component of the formula in eq. 3.1.

This is achieved with changing the output voltage on a remotely controlled laboratory power supply ranging between 0 V to 24 V, which provides the input for the high voltage DC/DC, that adjusts its output voltage proportionally. The interlock signal provides information about the state of the safety enclosure. Such that when the enclosure is opened, all system voltages that may exceed 50 V are quickly and safely discharged, so as to not cause potential harm to the user.

Discharge circuit works together with the interlock switch and, when engaged, discharges the high-voltage capacitor bank by connecting it to the ground through a resistor network. The confirmation is provided in a form of detection circuit, which powers an LED indicator when the high-voltage

remains above 50 V, in order to make it clear that handling of the board is safe.

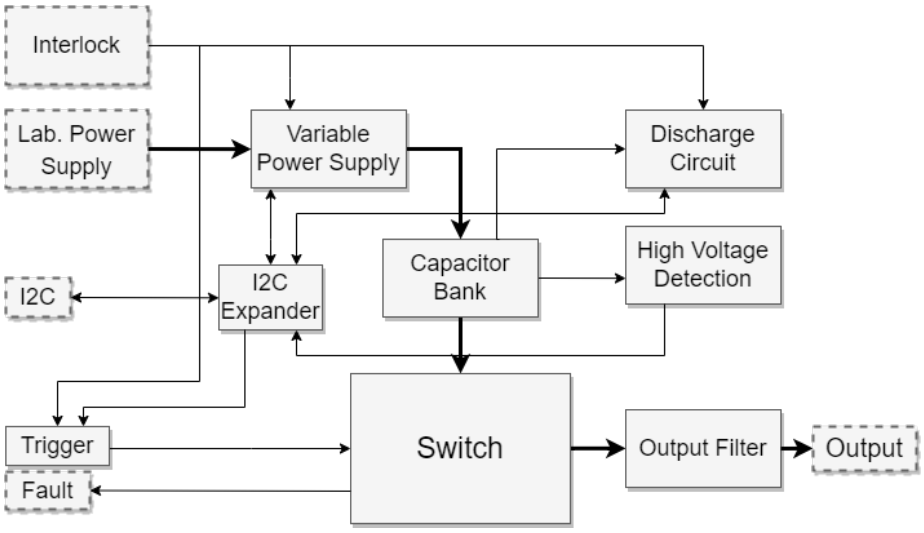


Figure 3.2: High-level overview of the Pulse Board

3.2.2 Switch

The high-voltage half-bridge switch is one of the key components in this setup which influences the performance. This board has to generate pulses with rising and falling edges in the range of single digit ns and the switches have to withstand voltages beyond 1 kV with switching frequency of more than 100 Hz. The pool from which the solution might be chosen is rather small. The design of the mother board will be centered around two selected types of switches:

1. Integrated half-bridge module using combination of Si MOSFETs,
2. SiC MOSFET Daughter Board - Self-made half-bridge module board using SiC MOSFETs as switches. It will serve as a slot-in pin-to-pin compatible replacement for the integrated half-bridge module.

The board is designed to support both of these solutions. The integrated half-bridge module, which has been a part of previous solution, and the newly designed daughter board that should be evaluated with the same conditions and analyzed as a possible long-term replacement.

3.2.2.1 Integrated half-bridge switch

The integrated half-bridge switch is the first solution to be discussed. It has been in use in current setup for some time. It acts as an integrated push-pull high-voltage switch and is critical to the function of the pulse board used for testing CMTI. Some key parameters are shown in tab. 3.1. As this is a custom made solution, there are no publicly available datasheets, only the information provided by the manufacturer for PCB design purposes.

Table 3.1: Characteristics of the integrated half-bridge module

Characteristic	Value
Max. Voltage	2 kV
Max. Peak Current	60 A
Turn-on/off rise time	15 ns

It is controlled by single positive logic control signal with a capability of creating square wave pulses into predominantly capacitive or resistive loads. The rise and fall time are being kept almost identical. It supports also bi-polar pulsing if needed. It provides a protection for overheating in medium to long-term time scale together with fault indication signal.

The disadvantage of this approach is that there is no control over what is happening inside the integrated switch and also, with the price above 1000€ per unit and long lead time of over 12 weeks, the flexibility in the case of malfunction is fairly limited. As a result, it was decided to explore other more cost-effective options and design a replacement, that would fit into the same supporting hardware and might offer more flexibility in terms of slew-rate control, using Silicon Carbide MOSFETs.

3.2.2.2 SiC MOSFET Daughter board

The alternative solution, which will be the main focus of the thesis, is a self-made half-bridge module in form of a daughter board. This module employs latest wide-bandgap Silicon Carbide MOSFETs, which offer superior combination of switching speed, efficiency and blocking voltage to the traditional Si transistors. The implementation and description of designed solution will be shown detail in section 3.3.

3.2.3 Schematic of the Mother board

In this section, schematic design of the mother board will be shown and described. The schematic follows the block diagram shown in fig. 3.2. Each block will be explained in detail. Firstly, the low-voltage side will be described, which includes control and power circuitry. Then the high voltage side will be presented with the high voltage supply, switch protection circuitry and safety circuits. At the end, the design of auxiliary circuits will be explained.

3.2.3.1 Control circuitry

In this section, the control circuitry of the main board will be presented. There are various signals coming into this board that influence the behavior. The main control signals are:

1. TRIG IN - Trigger input signal coming from the DUT Board that this board is to mate with. Defines a positive logic control signal, which should be propagated into the output waveform.
2. Interlock - Logic signal coming from DC power supply that goes through mechanical switches on the board's safety enclosure. Indicates the open/closed state of safety enclosure box.
3. Discharge control - The discharge circuit may be controlled either automatically with the lid opening or externally as the control signal is connected to a I^2C expander.
4. I^2C - Board provides expander to read-out or set selected number of signals on the board. This allows to verify state of the board from the remote control and react accordingly.

In the fig. 3.3, the input side of the switch interface is shown. The main input is coming from a BNC that connects to existing DUT Board. The PCB has various options for connecting the trigger to this board to aid debugging, TRIG_IN1 and TRIG_IN2. To further improve it, there are also numerous probe points on the input side to verify signal integrity as the environment, that the setup operates in, may be noisy.

As a consequence of this, to strengthen the robustness of the power supply, ferrite beads (FB3, FB4) and bypassing capacitors (C40, C41) are used to

filter out unwanted disturbances. The input trigger is then gated with the interlock signal to block any triggering of the switch, when the lid of the safety box would be opened.

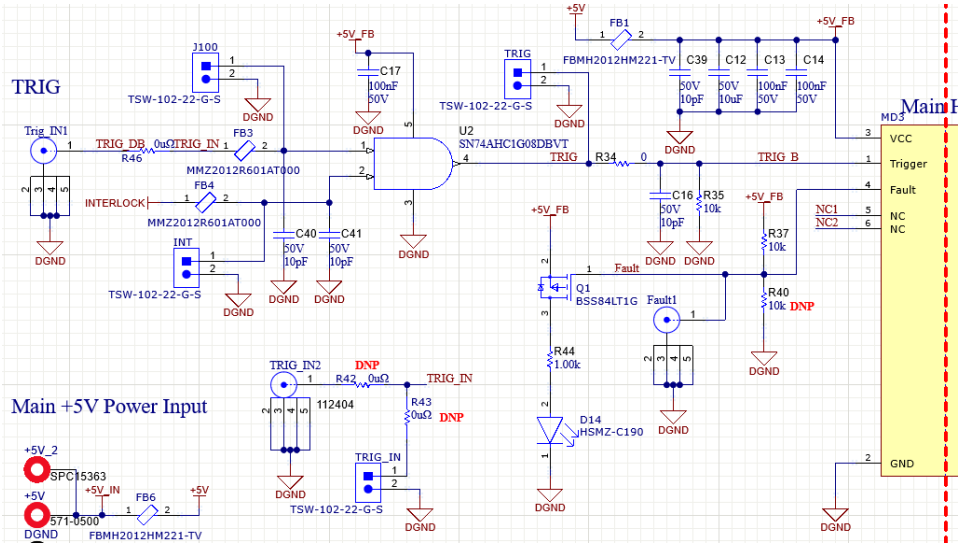


Figure 3.3: Input side of control circuitry on the Mother board

At the end of the trigger signal path, there is one more RC filter, that may be populated when the application would require it. Also a pull-down resistor is present to safely tie the input to ground if it is not being driven. This ensures safe condition of the switch and discharges the capacitors employed in the output filter, discussed in section 3.2.3.7.

The integrated half-bridge module also provides signalling which may indicate either overheating, undervoltage or overvoltage event on the input side. This is an active-low signal with limited drive capability so a P-type MOSFET, that switches a red diode, is used for indication. Fault signal is also connected to a BNC, which, as well as Trigger, mates with the DUT Board and may be then read with the software remote control.

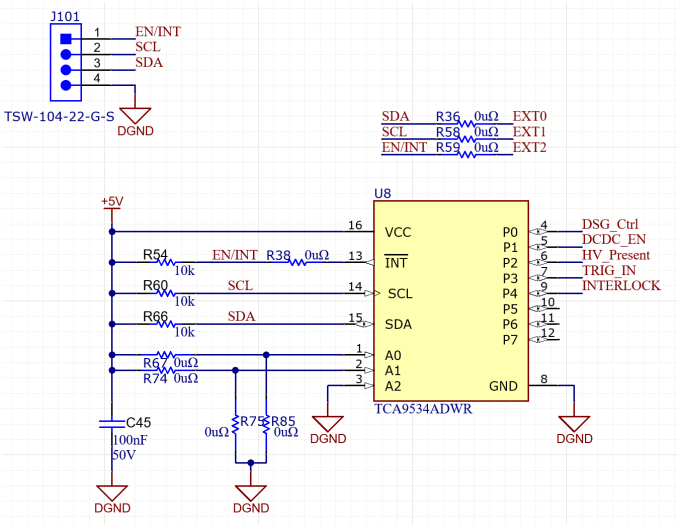


Figure 3.4: I^2C control circuit

In fig. 3.4, the I^2C circuitry is shown. Exploiting the TCA9534ADWR from Texas Instruments. This integrated circuit allows expansion for I^2C to general purpose parallel input and output pins to drive or read up to 8 signals with the option to utilize interrupt pin INT to notify about change of state on desired pin. The I^2C is capable of up to 400 kHz communication in the fast mode. [27]

With this, the software controlling the test sequence may use it to read out the state of the board with following information available:

- DSG_ CTRL - Control signal to drive the discharge circuit when deemed necessary.
- DCDC_EN - Allows for the verification of the state of the high voltage power supply. Provides option to independently turn-on and off or read out its status.
- HV_present - Informs the software about presence of the high voltage on the board. I may be used as a confirmation of correct behavior of the board for test sequence control.
- TRIG_IN - User may read out or set independently a trigger signal.
- INTERLOCK - Provides information about the state of the safety-enclosure.

3.2.3.2 High Voltage power supply

With the design decision that the variation of the slew-rate will be achieved with changing the input voltage therefore the dV of the signal, the high voltage power supply must be adjusted to allow this option. A DC/DC converter module 24VV4 from PICO Electronics was chosen.

This module will be driven with remotely controlled power supply and provides variable proportionate input-to-output voltage control with delivering up to 9 W of power in miniature plug-in or surface mount package. The module comes in many variants, of which the 15VV1, 15VV2 and 24VV4 are preferred to be used, depending on the scale of the desired slew-rate steps and lower threshold of it. [28]

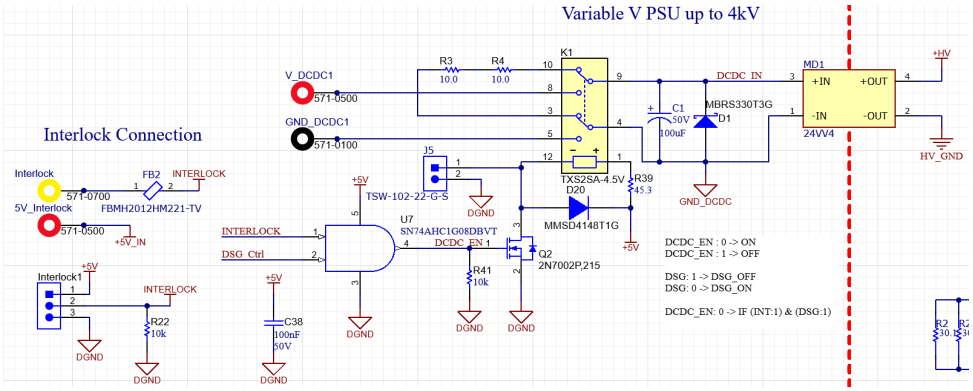


Figure 3.5: Variable high voltage power supply

The schematic of the input side to the high voltage DC/DC is shown in fig. 3.5. The power from the laboratory power supply goes through a relay, which is a TXS2SA-4.5V, capable of switching up to 1 A at 30 V with the coil current of only 11 mA. The high voltage DC/DC will be fed with up to 24 V with maximum current of 500 mA.

It is a single side stable non-latching, which means that it stays in default condition displayed in the schematic symbol when not driven. [29] At the inputs of the module, there is a large capacitor, C1, 100 µF and Schottky diode, D1, for over-voltage protection and to aid power supply robustness.

Figure 3.6: Relay used to switch the DC/DC input power [30]

In this default condition, the DC/DC inputs are shorted through a pair of resistors, R3 and R4 connected in series, in order to discharge the input capacitance and any power left in the inputs of the DC/DC module. Neither the resistors nor the DC/DC module have any pin connected to the source voltage in this default condition. This will result in turning-off of the output high voltage and therefore disable the ability to create pulses.

Switching of the relay is controlled with a single low-side N-type MOSFET, that is driven with an AND gate to account for various scenarios in which the power supply should be turned-off. The safe state is when DCDC_EN is at logic level 0, because of this there is a pull-down resistor, R41, at the gate of the transistor Q2. All logic states are illustrated in the tab. 3.2.

Table 3.2: Switching the power supply - logic table

Discharge	Interlock	DCDC_EN	HV_PSU
ON	OFF	0	OFF
ON	ON	0	OFF
OFF	OFF	0	OFF
OFF	ON	1	ON

With INTERLOCK signal being active high and DSG_Ctrl being active low. DCDC_EN should become logic 1 only if INTERLOCK is active and DSG_Ctrl is at logic level 0. This means that the lid is closed and discharge control disabled otherwise the power supply would be on at the same time that the quick discharge would be enabled, exceeding power capabilities of the PICO DC/DC Module.

3.2.3.3 High Voltage input

The output of the high-voltage DC/DC and thus the input power stage to the high-voltage half bridge switch provides necessary power for these high slew-rate pulses. Requirements for the board state that it has to be

able to handle up to 3 kV of common-mode voltage and some added margin. Board design then settles on adapting everything on the high-voltage side to withstand 4 kV.

This requirement has proven to be very challenging, mainly in choosing the capacitors that will provide necessary immediate current for the pulses as in simulation. In simulations, these transition currents had proven to be able to reach up to 30 A just for couple of ns.

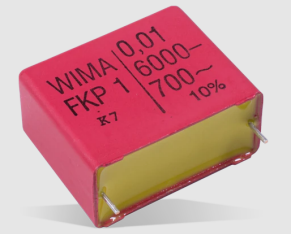


Figure 3.7: WIMA FKP1 pulse rated capacitor [31]

The capacitors have to be not only rated to survive the voltage, also they have to be specifically designed to be able to provide the required energy for many cycles. This means withstanding high discharge and charge rate over many cycles and over broad temperature range. The FKP1 family from WIMA GmbH, shown in fig. 3.7, was chosen to be employed in the capacitor bank.

These polypropylene capacitors are developed for extreme high pulse loads. They are fully self-healing, utilizing a floating electrode that is metallized on both sides. On top of that they have very low dissipation factor, which allows them to retain charge longer and are rated to operate between −50 °C to 100 °C. [32]

The advantage of these capacitors also is, that they come from a broad family, which provides opportunity to exchange capacitors as many of them have a similar pitch. For that reason there are two types of these capacitors in the capacitor supply bank. There are 15 nF and 10 nF rated at 4 kV, which represent a broad capability in adapting different size capacitors, for example at lower voltages around 2 kV, capacitance up to 330 nF may be placed to improve the power supply durability. [32] This exchange would be very favorable when testing the SiC daughter board, which supports maximum of 1.7 kV.

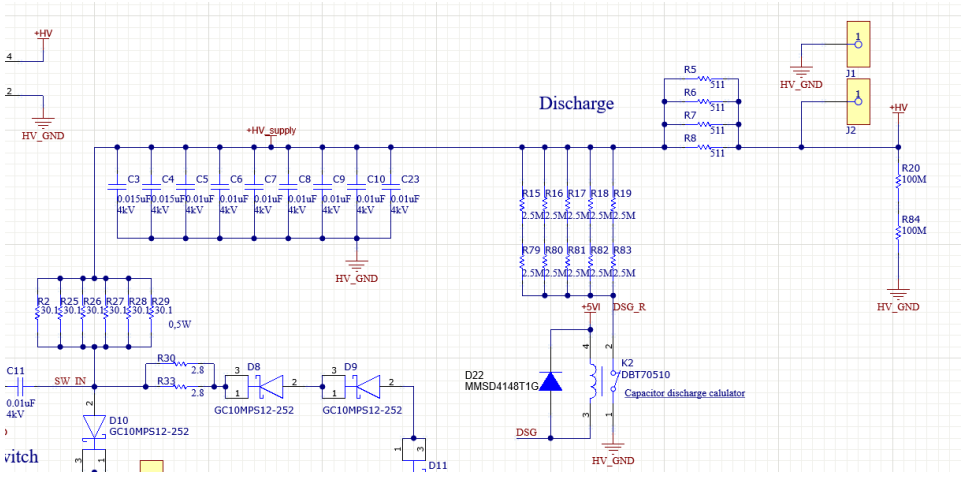


Figure 3.8: Input power stage for the switch

Aside from the capacitor bank, there is a discharge circuit, which will be described in detail in section 3.2.3.4. There are resistors R5, R6, R7, R8 to provide a current limitation for the DC/DC module to avoid putting excessive stress onto the DC/DC. Resistors R20 and R81 serve as a constant discharge, they are doubled with resistors R9 and R14 in the circuit that shows the presence of high voltage, shown in fig. 3.12. These resistors effectively form a constant discharge resistance of around 100 MΩ.

This constant discharge has an important role to discharge the high voltage capacitors when input power is removed from the high voltage DC/DC and provide a back-up to the main discharge circuit, which will be discussed in section 3.2.3.4. Lastly, there are probe points to enable verifying power supply integrity during the pulses.

3.2.3.4 Discharge circuit

Discharge circuit is the most important safety feature of this board as it eliminates the risk of user accidentally touching any higher voltage. Since the board may use voltages up to 4 kV. Discharge circuit must be able to get rid of this built up energy in timely manner so that the handling of the board may be as safe as possible. There are 2 discharge circuits implemented to consider. The first is a simple resistor for a constant slow discharge, which was described in previous section.

The second one is the fast discharge path, for which the requirements state

that it has to discharge the capacitor bank under 1 s, so that in the event of opening the lid with the power still on, the energy will be dissipated before the user may have a chance to touch it. Discharge circuit will work closely together with High-Voltage Indication circuit, which will be described in section 3.2.3.5.

In the fig. 3.9, the high voltage side of the discharge circuit is shown. There are two major components in this figure. The Relay K2 and the resistor network, which is comprised from five times two resistors in parallel, forming a five 5 MΩ parallel network, for which the final discharge resistance is:

$$R_{DSG} = R1||R2||R3||R4||R5 = 1\,\mathrm{M\Omega}. \tag{3.2}$$

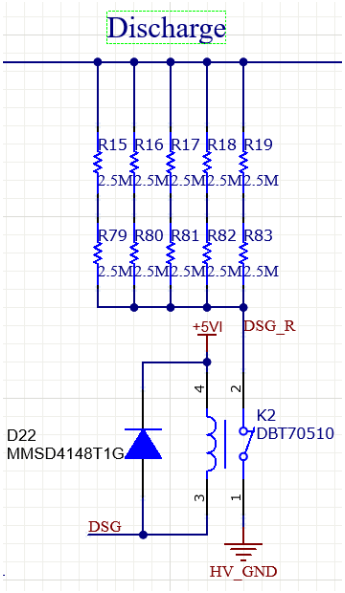


Figure 3.9: Discharge circuit

Each of these ten resistors is rated for 4 kV which, used in the ladder of two, is plenty enough to withstand even the worst scenario for the board. In order to meet the maximum power dissipation of the resistors, the parallel network is used, as each resistor can continuously dissipate 1.5 W. [33]

Interlock and discharge circuit are tied together at the input of the HV power supply. They control the input to the high voltage DC/DC with the relay, which effectively prevents applying full load onto these resistors, as explained in section 3.2.3.2. These resistors will therefore not experience the full continuous power load, rather a peak one which will occur occasionally. [33]

This peak power dissipation can be calculated for one branch of the resistor network. With the maximum design voltage of 4 kV, the absolute worst case scenario across for example resistors R19 and R83 would be:

$$P_{DSG1} = U \cdot I = 4000 \cdot \frac{4000}{5\,\mathrm{M\Omega}} = \frac{16}{5} = 3.2\,\mathrm{W}. \tag{3.3}$$

This power will be then divided between the two resistors effectively applying only half to each one of them, so 1.6 W. This would be the maximum peak, that would occur for around 1 s and in real use-case would not reoccur for another at least couple of seconds.

The maximum value for the capacitor bank at 4 kV is 80 nF. To discharge this through a 1 MΩ, the time constant of this circuit may be calculated as per eq. 3.4. The capacitor is considered discharged after 5 times the time constant of the circuit [4], which gives the discharge time of:

$$\begin{aligned} \tau &= R_{DSG} \cdot C_{DSG} = 1\,\mathrm{M\Omega} \cdot 80\,\mathrm{nF} = 0.09\,\mathrm{s} \\ \Rightarrow t_{DSG} &= 5 \cdot \tau = 5 \cdot 0.09\,\mathrm{s} = 0.45\,\mathrm{s}. \end{aligned} \tag{3.4}$$

It gives plenty of headroom for the 1 s requirement that the board is to meet. The maximum capacitance that would meet the criteria, may be calculated as:

$$\begin{aligned} t_{DSG} &= 5 \cdot \tau = 5 \cdot R_{DSG} \cdot C_{DSG} \\ \Rightarrow C_{DSG} &= \frac{t_{DSG}}{5 \cdot R_{DSG}} = \frac{1\,\mathrm{s}}{5 \cdot 1\,\mathrm{M\Omega}} = 200\,\mathrm{nF}. \end{aligned} \tag{3.5}$$

The other important part of this circuit is the relay. It has to be rated to handle up to 4 kV. The only available one, with higher isolation than the required threshold, was DBT70510 from Sensata Technologies. It is rated to withstand up to 10 kV with switching voltage rated at maximum of 7 kV and switching power maximum of 50 W, which would be more than enough for the application. [29]

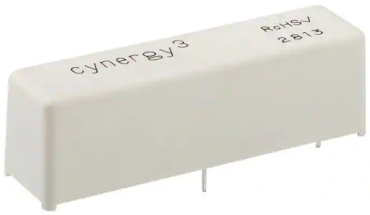


Figure 3.10: DBT50710 High-Voltage Relay [30]

The selection process was heavily influenced by the shortage of components as many other lower-spec alternatives were out of stock. The coil voltage is rated at 5 V and with its resistance of 38 Ω the coil current is fairly high at 131 mA. [29] The chosen relay is the normally closed version, which ensures that, when everything is powered off, the capacitor bank would be tied to ground, so that no excess charge would be left in the capacitors.

Across the coil of the relay, there is a flywheel diode to provide escape path for backslash current, that may be induced by the coil, when the control current would be switched off. The discharge is controlled with an optocoupler, which transfers the control signal from the control side and has its own power supply, MD2, to ensure stability and provide necessary power for the switching of the relay. The discharge control circuitry is displayed in fig. 3.11.

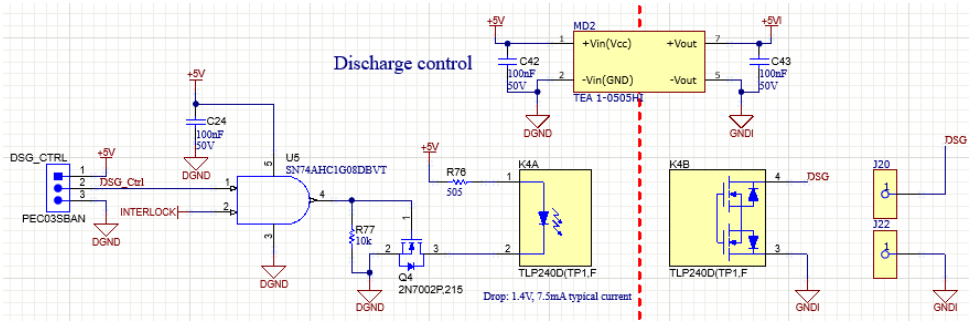


Figure 3.11: Discharge circuit control

Common isolated DC/DC converter, TEA 1-0505H1, is used to isolate the circuitry from the main 5 V power supply to ensure the stability and integrity of the signals on the control side. It can provide up to 200 mA of current, which is sufficient to handle the relay drive. On both sides, there are decoupling capacitors, C42 and C43, to filter out excessive noise coming in or out of the power supply.

The optocoupler is driven with an AND gate operating low-side switching N-type MOSFET. The gate ensures that the discharge is in ON state when the INTERLOCK, which is an active high signal, is not engaged as the relay, when is not driven, defaults to normally closed state to provide the discharge path. Resistor R77 is a necessary pull-down, which prevents the transistor's gate to be floated into undefined state when not driven.

The chosen optocoupler is TLP240D from TOSHIBA, which can handle in its on state up to 250 mA and provides up to 5 kV_{rms} of isolation. The trigger LED current is rated at maximum 3 mA [34], that is supplied through

the resistor R76. The current supplied may be calculated as:

$$I_{LED_{DSG}} = \frac{U}{R} = \frac{V_{ss} - V_{LED}}{R_{LED}} = \frac{5 - 1.4}{3\,\mathrm{k\Omega}} \approx 1\,\mathrm{mA}. \tag{3.6}$$

This provides margin above the typical rated trigger current of 0.6 mA stated in the datasheet. [34]. The DSG_Ctrl signal can be either connected and driven externally or tied to a fixed voltage level using DSG_CTRL pin header.

3.2.3.5 High Voltage Indication circuit

The indication of presence of high voltage is, together with the discharge circuit, the second safety feature integrated onto the mother board to protect the user. The main purpose of this circuit is to turn-on an LED whenever the voltage on the power supply exceeds 50 V. It is rated, as majority of the circuits on the high voltage side of the board, up to a voltage of 4 kV.

Displayed in the fig. 3.12, it is a comparator circuit, that follows the voltage on the capacitor bank through the series resistors R9, R14 and R24. All of these resistors are also part of the constant discharge circuit mentioned earlier in section 3.2.3.4. Providing, together with resistors R20 and R84 shown in fig. 3.8, a constant discharge path.

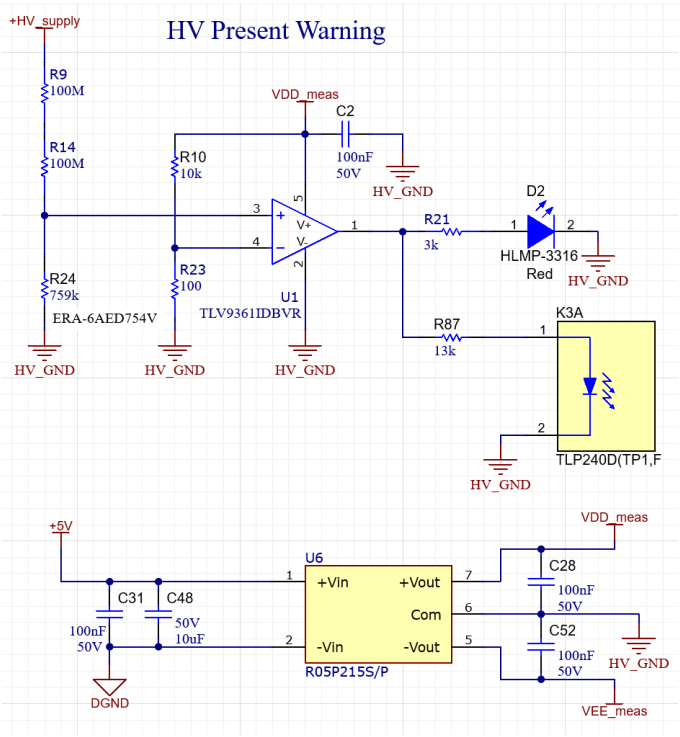


Figure 3.12: High Voltage signalling circuit

With the requirement for the detection voltage, the threshold of the amplifier must have been chosen. It was determined that the lowest detection voltage would be around 150 mV in order to ensure the stable operation in a very noisy environment. As to reach 150 mV for a 50 V voltage at the high voltage power supply, the voltage on the plus node of the U1 amplifier, when applying the maximum rated voltage, should not exceed the power supply voltage of the circuit, which is in this case 15 V.

Closest standard value resistor that ensures it, when using two 100 MΩ as the first resistance in the ladder, is the 759 kΩ. For this combination the voltage at the positive node may be calculated as:

$$\begin{aligned} V_{R_{24}} &= V_{HV_{supply}} \frac{R24}{R9 + R14 + R24} \\ &= 4000\,\mathrm{V} \frac{759\,\mathrm{k\Omega}}{100\,\mathrm{M\Omega} + 100\,\mathrm{M\Omega} + 759\,\mathrm{k\Omega}} \approx 14.8\,\mathrm{V}. \end{aligned} \tag{3.7}$$

When the voltage for the maximum of the allowed range is verified, the opposite one has to be checked as well to ensure correct operation. If 50 V is applied at the high voltage input, the voltage at the positive input node of the amplifier, U1, may be calculated as:

$$\begin{aligned} V_{R_{24}} &= V_{HV_{supply}} \frac{R24}{R9 + R14 + R24} \\ &= 50\,\mathrm{V} \frac{759\,\mathrm{k\Omega}}{100\,\mathrm{M\Omega} + 100\,\mathrm{M\Omega} + 759\,\mathrm{k\Omega}} \approx 189\,\mathrm{mV}. \end{aligned} \tag{3.8}$$

This value also provides some operational margin in case of different temperature state of the circuitry. With this in mind, the threshold has to be set for the $V_{th} = 150\,\mathrm{mV}$. This will be achieved with resistors R10 and R23 on the negative node of the operational amplifier, U1, as:

$$V_{R_{23}} = V_{DD_{meas}} \frac{R23}{R10 + R23} = 15\,\mathrm{V} \frac{100\,\Omega}{10\,\mathrm{k\Omega} + 100\,\Omega} \approx 149\,\mathrm{mV}. \tag{3.9}$$

The indication will be provided with the D2 red LED, which is driven with a current set with the resistor R21, whose value has been empirically set to 3 kΩ to provide sufficient intensity of indication.

The information about the presence of the high voltage is also transferred across the isolation barrier, for the remote software control to read out, using an optocoupler. In this case it is used in reversed direction as in the discharge circuit. Resistor R87 is responsible for setting a correct current for the drive of the optocoupler. Which has been calculated the same way as in a case for the discharge control circuit in eq. 3.6.

The high voltage indication circuit will be powered by its own power supply, R05P215S/P from RECOM. This isolated DC/DC converter will provide 15 V to this circuit as the other power supplies, which may power the daughter board, will be referenced to floating or other voltage levels that would not ensure proper operation at all times.

3.2.3.6 Switch

The high-voltage half bridge switch that is responsible for creating the pulse, is the most important component of this work. The other requirements are determined by the characteristics of the switching element. The mother board was designed for the integrated half-bridge module as it was a part of the previously utilized solution. The daughter board will be able to be slotted-in as a replacement. The switch schematic is shown in fig. 3.13.

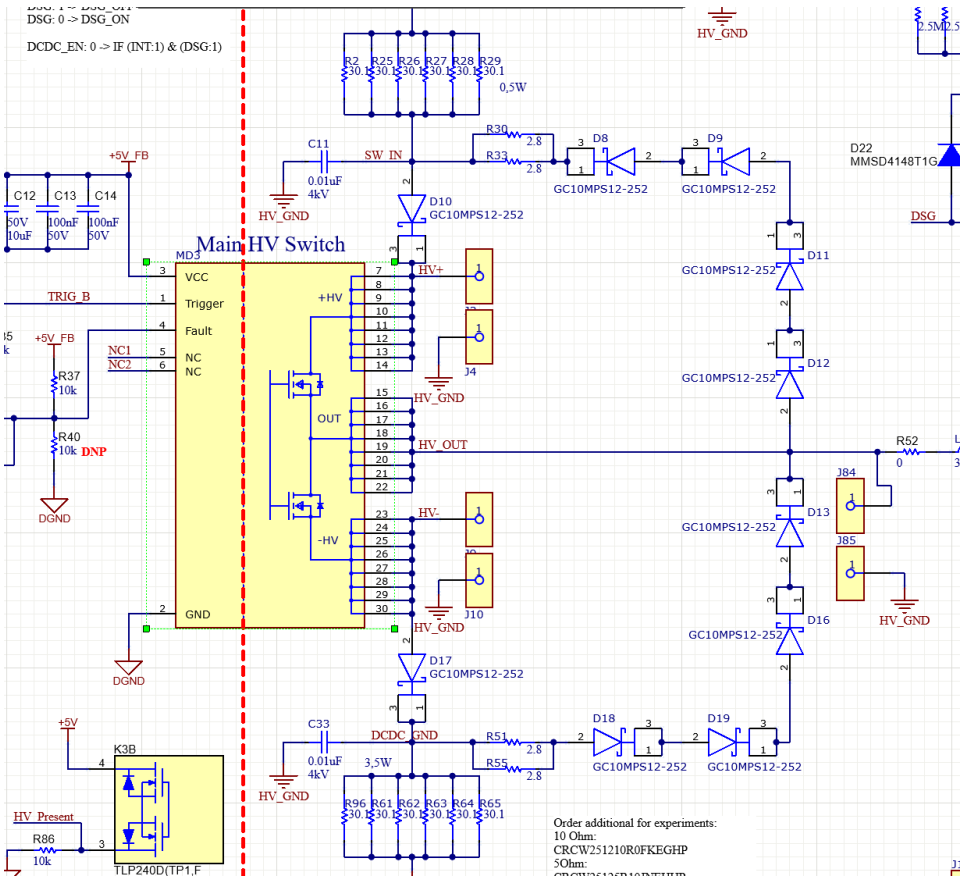


Figure 3.13: Main Switch circuitry

The series resistance is a requirement for the protection of the half-bridge module to ensure proper function with limiting the current that may shoot-through. The resistors R2, R25, R26, R27, R28 and R29 form a 5 Ω parallel network, which has been suggested as the lowest value by the manufacturer. The series diodes D10 and D17 are in place in order to protect the integrated half-bridge module from reverse current flowing through the transistors, due to a slightly inductive load and board parasitics.

Another protection feature, implemented specifically for the module, are the bypassing diodes D8, D9, D11, D12, D13, D16, D18 and D19. Their purpose is to protect the transistor from reverse voltage and are essential for the proper function of the module, because the module itself does not have protection diodes integrated. This was discovered on the previous solution through extensive laboratory testing and this solution was found to be sufficient. All of these diodes are SiC Schottky diodes rated to withstand 1200 V, GC10MPS12-252. They are arranged in series to boost the reverse voltage capabilities.

All of the resistors values, shown in fig. 3.18, were determined through simulations using TINA-TI simulation software as well as the capacitors between the series resistor and the diode D10 and D17, C11 (and C33 respectively). It was found out that these capacitors provide a boost for the output slew-rate in the simulations, while not endangering the switch itself. The results of the simulation are shown in fig. 3.14.

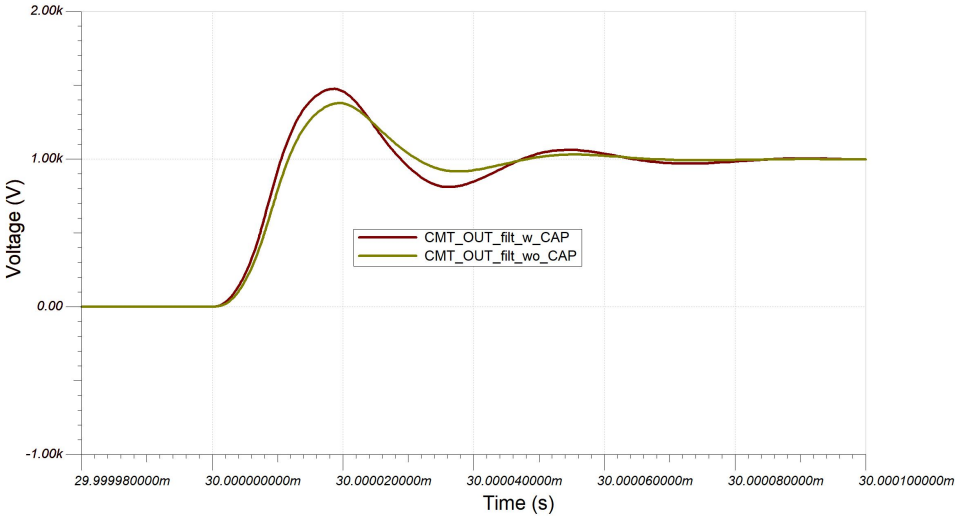


Figure 3.14: Capacitor C11 influence on simulations

The resistance in series with the feedback diodes on the other hand provided a reduction in the overshoot therefore compensating the increase induced

with the capacitors. This is shown in fig. 3.15.

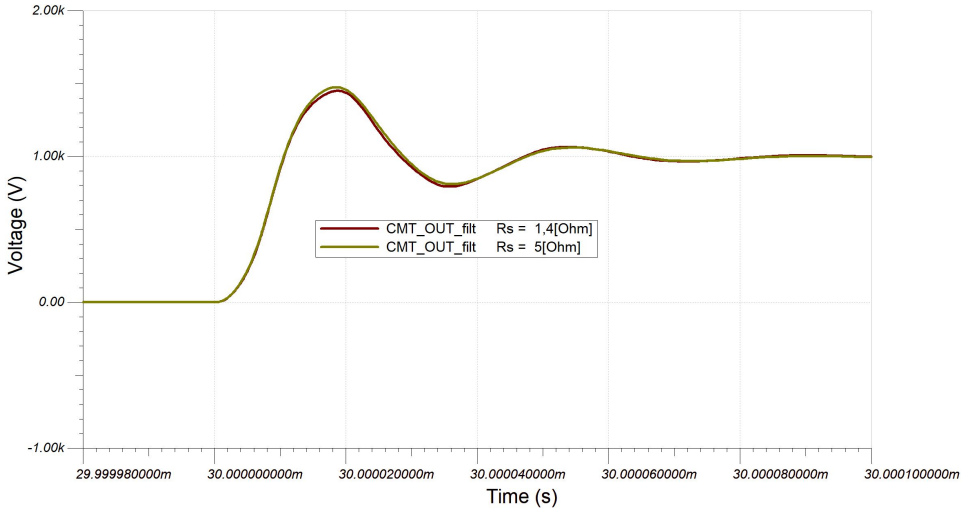


Figure 3.15: Feedback series resistor influence on simulations

For debugging and measurement purposes, there are many probe points to measure the voltage waveform when switching. For these measurements a special high voltage probe must be used. The Keysight 10076C high voltage passive probe with 500MHz bandwidth will be used alongside with special probe points which may facilitate this probe, shown in fig. 3.16. These probe points provide easy connection for this probe to be used.

Figure 3.16: Used probe points [35]

The switch itself, or any other self-made module, will be connected to the board through pin sockets, shown in fig. 3.17. These provide easy slot-in interface that enables to exchange the device in case of malfunction.

Figure 3.17: Sockets for the pins of the switch [36]

3.2.3.7 Output filter

The main function of the output filter is to shape the output waveform in order to generate the maximum possible slew-rate as well as protect DUT from oscillations, which may happen if the output would be without sufficient damping.

For this application, it is determined by the requirements that the slew-rate is calculated from 20% and 80% of the peak voltage of the output waveform. This has been found to be good compromise, which allows to describe the edges true speed as the waveform is not solely linear, because of the parasitics of the board and the switch, which are inducing overshoots and oscillations. The reasoning behind this definition was described in section 2.2.1.5.

The output filter design has been from the most part transferred from the previously used solution and optimized to provide better performance at the expense of higher overshoot as the devices, which will be tested, have isolation ratings far exceeding the testing voltage. For the simulations, TINA-TI has been used and the schematic created for the transient analysis is shown in fig. 3.18.

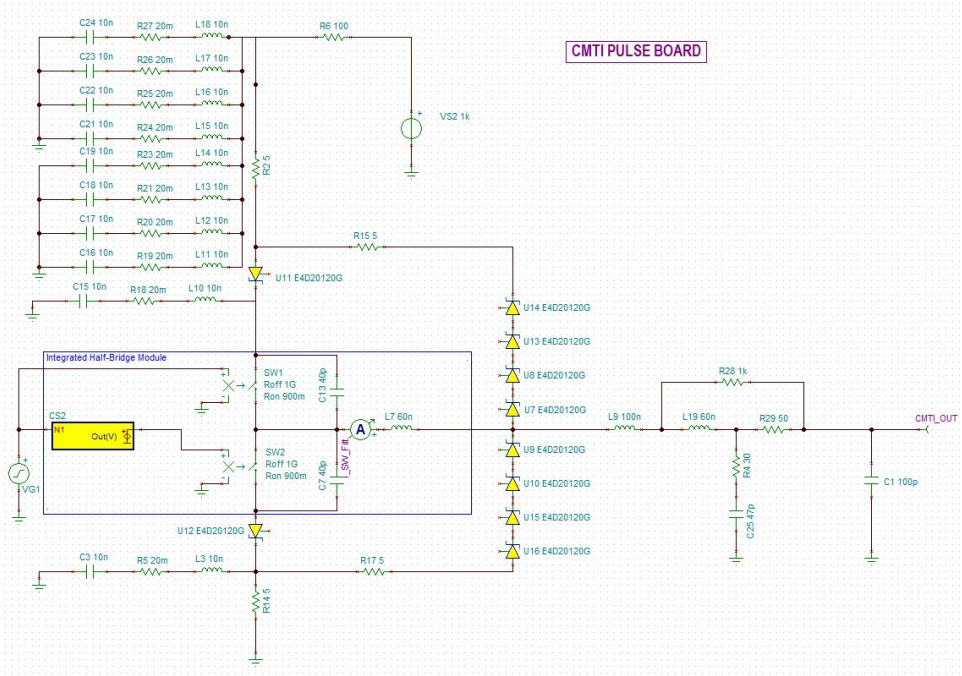


Figure 3.18: Simulation schematic of the Half-Bridge module circuit

The limitations of these simulations are in the lack of parameters that would describe the behavior of the integrated half-bridge module as only the C_{ds}, R_{dsON} and some parasitic inductance were provided by the manufacturer. This was also one of the reasons to explore other solutions like the the daughter board. In the fig. 3.19, the old filter configuration is presented. The evolution into the improved configuration, shown in fig. 3.20, happened through a series of iterative parametric simulations that aimed to optimize each element.

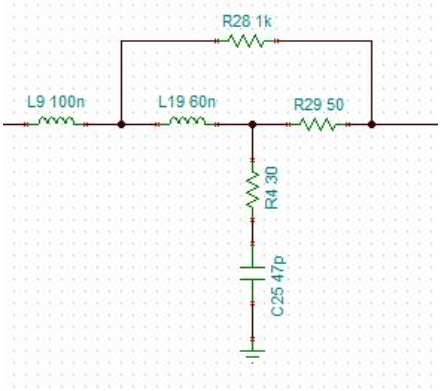


Figure 3.19: Old filter

The basis of this filter is a snubber circuit formed from C25 and R30, which serves as an oscillation damper. This circuit has to be used as without it the parasitic inductances and load capacitance form a series RLC circuit, which may oscillate. These fast following transients, made by these oscillations, could induce false CMTI test failures, which were not caused by the transient itself, but rather by repeating fast oscillations. The snubber circuit on the other hand can significantly hinder the slew-rate performance. So it is essential to find a right balance.

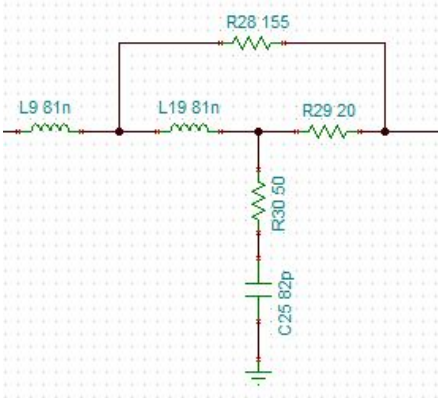


Figure 3.20: New filter

The inductors in the filter provide a way to manipulate the parasitic one and therefore control the behavior. The bypass resistor R28 provides route for some of the high frequency parts of the impulse to get through and series resistor R29 is there to manipulate the resistance in series RLC circuit. The optimized filter is shown in the fig. 3.20. The comparison between the two filters is presented in fig. 3.21. It may be seen that the improved slew-rate is at expanse of higher overshoot, which has been considered as a correct trade-off, because of the fact that tested devices are rated for way higher isolation voltages.

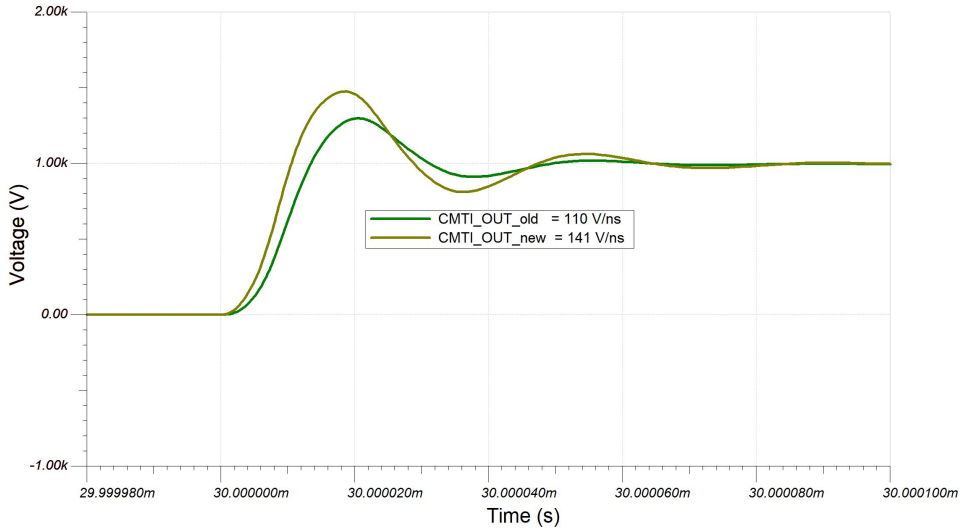


Figure 3.21: Output filter comparison

In the fig. 3.22, the implementation of the filter into the schematic is shown. Various components are separated into parallel combinations in order to satisfy power ratings and also achieve desired values. The resistors used are specifically rated to withstand pulse loading. They come from a CRCW-HP-e3 family of pulse proof, high power, thick film chip resistors from VISHAY and are rated to be capable of handling pulsed loads. They provide high power rating of 1.5 W in 2512 package alongside with operating voltage of up to 500 V_{rms}. [37]

It was verified with the simulations, that the pulse load voltage and power ratings are not exceeded even with the maximum input voltage of 4 kV. The power load was then determined for all components and it is written next to each network that is representing single element. In all cases, overhead was provided with implementing additional parallel resistors to account for variations and future expansions or updates. Capacitor C44 provides future upgrade path, which has not yet been verified and will not be used during evaluation of this thesis.

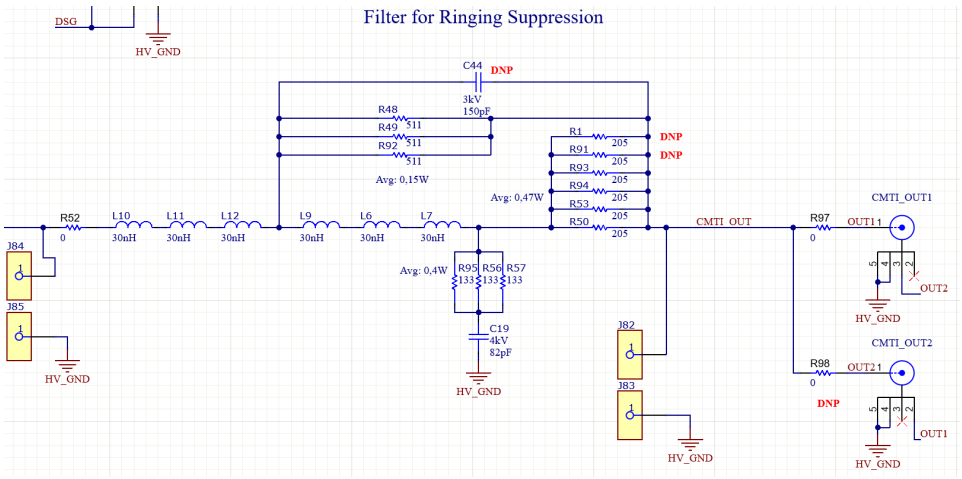


Figure 3.22: Output filter

To complete the description of the schematic in fig. 3.22, there are two sets of probe points to verify and support debugging of the output filter. These allow for measurement of the input and output waveform of the filter. The CMTI pulse will be transferred out of the board through a BNC connector. This BNC is specifically rated to withstand up to 750 V_{rms} and will be edge mounted to allow easy connection with the DUT board via BNC coupler. [38]

To verify the voltage rating of the BNC connector, the V_{RMS} will be calculated. The pulse width of the CMTI waveform is set to 10 µs and when accounting for the maximum theoretical frequency of 1 kHz as the worst case scenario, the resulting duty cycle may be as high as 1%. The RMS voltage of a square wave may be then calculated, with the maximum voltage of 4000 V, as: [39]

$$V_{RMS} = V_{pp}\sqrt{\frac{t1}{T}} = V_{pp}\sqrt{D} = 4000 \cdot \sqrt{0.01} = 400\,\mathrm{V_{rms}}. \tag{3.10}$$

Where the D stands for duty cycle and V_{pp} is the maximum peak voltage.

There are two output BNCs in order to provide the capability to send pulses between two grounds of the isolated device under test in both polarities. The first one enables it to be send to the high-side ground, the second one to the low-side one of the isolated device.

3.2.3.8 Auxiliary power supplies

On the mother board, there are several isolated power supplies providing necessary power to the supporting circuits. Earlier in section 3.2.3.5, the isolated module for high voltage indication circuit was shown as well as the one for discharge control circuit in section 3.2.3.4, fig. 3.11. As this is a second revision of the mother board, it implements some future upgrade paths.

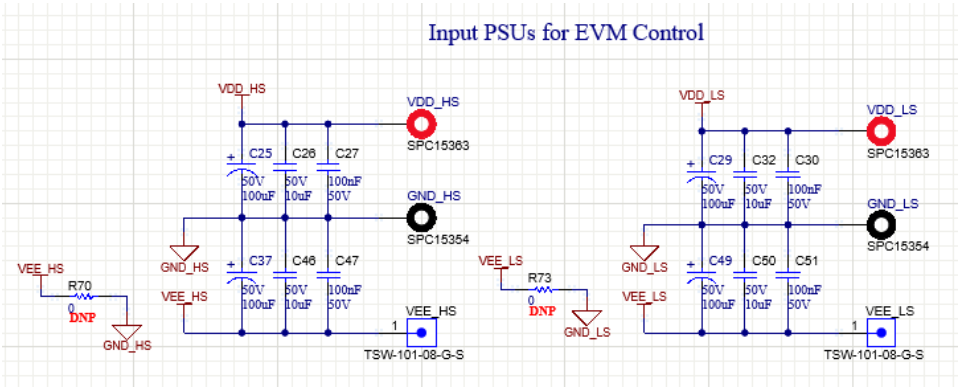


Figure 3.23: Connection for the custom variable isolated power supply boards

One of these is shown in fig. 3.23. These connectors are made to support a mounting of custom isolated power module PCBs, which are yet to be evaluated and they were not part of this thesis. They would ultimately allow to vary the output voltage on both positive and negative power supply and with them being fully programmable, they would essentially provide easy way how to control a switching speed of the MOSFET on the daughter board. Therefore give a possibility to manipulate dt in the definition of the slew-rate alongside with already implemented ability to change dV component.

There are spare footprints for isolated DC/DC converters, placed in the schematic, to support the case when the isolated power module boards would not be present. These are identical to the ones utilized on the daughter board, which are specifically made for driving MOSFETs and IGBTs with asymmetric power supply requirements and they are fully described in section 3.3.1.4. These are shown in fig. 3.24 alongside their respective decoupling capacitors.

Both of these solutions, the isolated DC/DCs and isolated module boards, are parts that provide future development possibilities as the daughter board, designed and shown later in this thesis, is made to be self-sufficient, therefore

these parts of the board will not be used in this thesis. The output sockets, shown in fig. 3.24, are going to be placed so that the daughter board may use them. Their respective position will match the similar holes made with the footprint of the DC/DC modules on the daughter board. Therefore they will provide the possibility to exchange the DC/DC modules on the daughter board for pin header to tap the supply from the mother board.

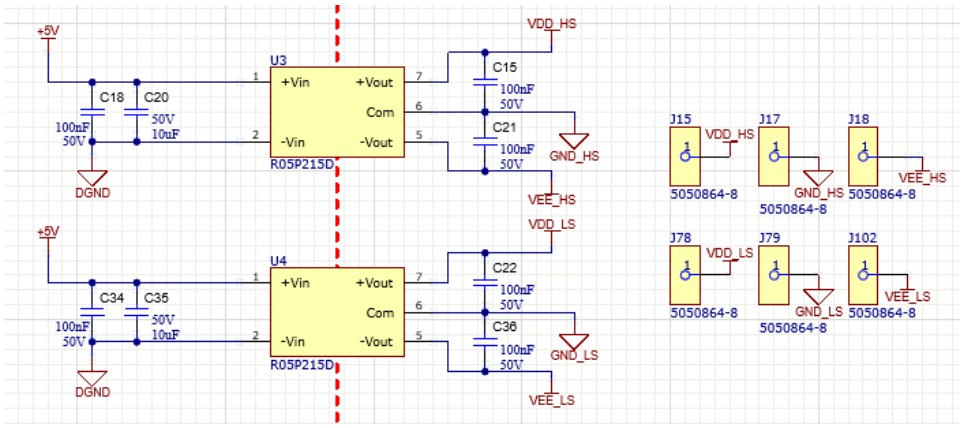


Figure 3.24: Substitute isolated DC/DC modules

In the fig. 3.25, it may be seen that all of these auxiliary power supplies are equipped with LEDs to provide easy debugging and visual indication of power supply being on or off. They also provide discharge path for some of the larger capacitors on the board, which are being utilized to supply sufficient power for the immediate current required for switching a gate of the transistor.

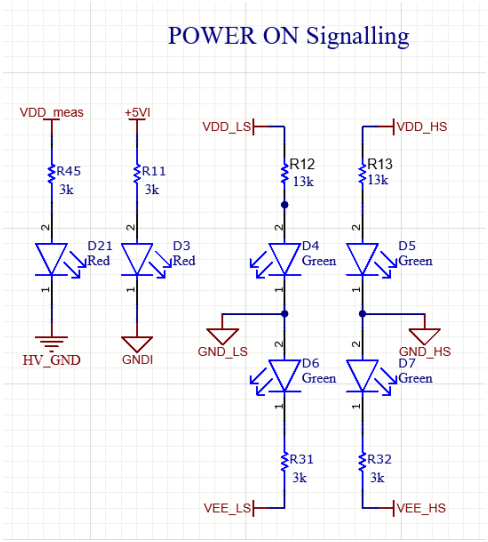


Figure 3.25: LEDs for indication of power present

3.2.4 Layout

With the requirement, that the board has to be able to withstand up to 4 kV, the layout of the board must be done carefully. The space constrains are very generous, so the isolation distances may be met even for the insulation rating of the FR4 and are sufficient to meet the requirements. There are several rules that have to be followed: [40]

1. clearances
2. good corner and pad shapes,
3. material isolation properties.

Based on the IPC-2221B standard calculator [41], the required spacing for the coated conductors on PCB at 4 kV is 11.48 mm, which has been implemented in the layout design.

The breakdown of the PCB through high voltage may happen due to direct arcing or corona discharge. Direct arcing over distance between two conductors happens when the dielectric's ability to withstand the voltage is exceeded. Corona discharge is a failure that may happen because of defects made by degradation of the isolation material. Corona discharge may preceed the direct arc over the isolation.

The chances of both of these destruction events may be reduced or eliminated by smooth round curves. [40] The example of the correct shape of the pads and traces is shown in fig. 3.26.

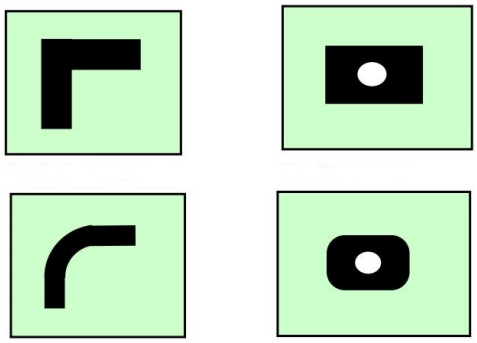


Figure 3.26: Examples of the correct pad and trace shape [40]

As there is enough space to work around and employ the clearances required, it was decided to manufacture the board using standard FR4. Which has initial dielectric rating of up to 900 V per mil. If accounting for aging defects and some margin, it may be considered as 300 V per mil. [40] The board has a standard thickness of 1.54 mm (approximately 60 mils), which gives the total isolation voltage of 18 kV. So the thickness of the board is more than enough to allow connections run underneath each other.

Physical dimensions of the board are mainly influenced by the DUT Board, which this mother board will pair with. In the birds eye view, the height is limited to the height of the DUT board and the width is not limited but should be kept as small as possible. These restrictions form the basic requirements and with them in mind, the first placement of the major blocks of circuitry was done.

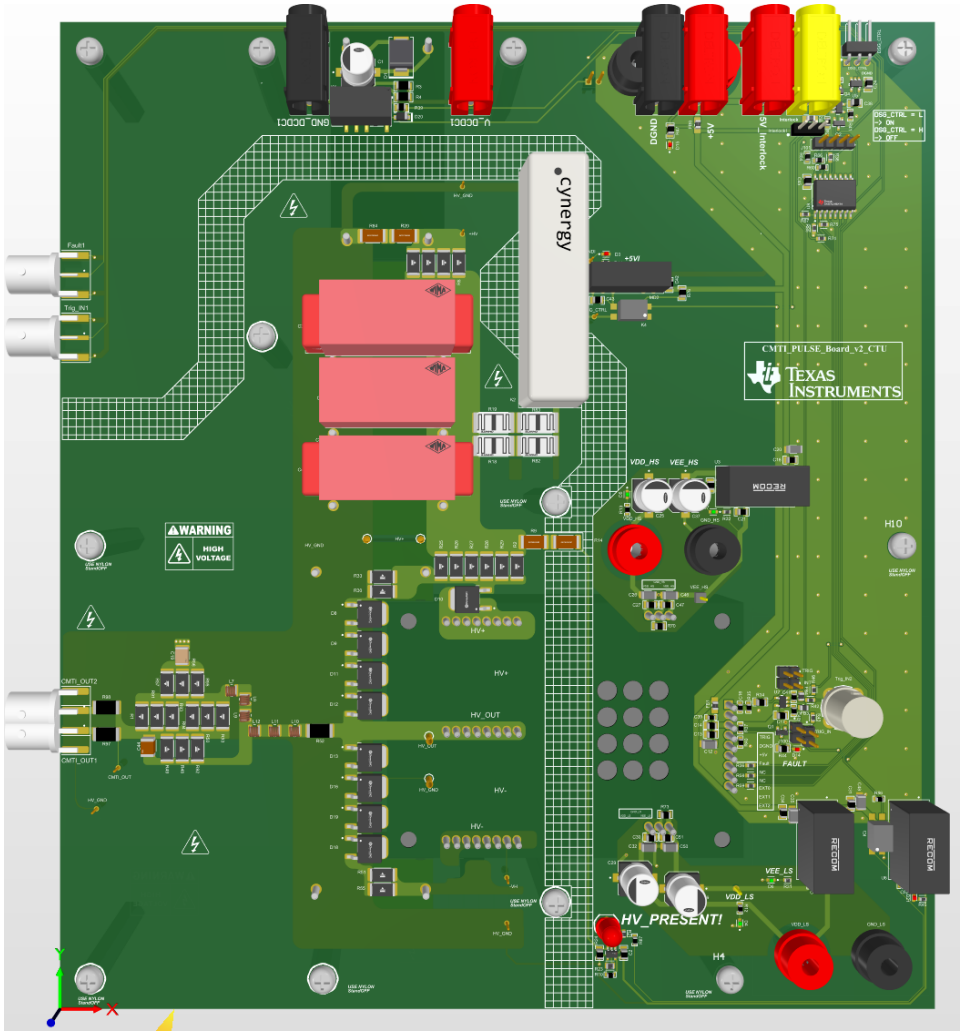


Figure 3.27: Top side 3D model view of the mother board

The physical dimensions settled on 248 mm by 220 mm. In the fig. 3.27, the bird's eye view of the mother board is shown. The connectors are heading north in order to clean up the cabling. The only exception is the interface that is to be mated with the DUT board, which needs to be on the left side of the board.

In the silk layers on both sides, the separation clearances are distinctly highlighted to ensure proper electrical isolation. The division between the isolated portions of the board is well illustrated with the picture of the top layer in fig. 3.28 and for the bottom layer in fig. 3.29. Aside from the connectors discussed before, the main highlight is the placement of the switch, which is located in the middle of the board opposite to the CMTI output BNC connector but on the bottom side.

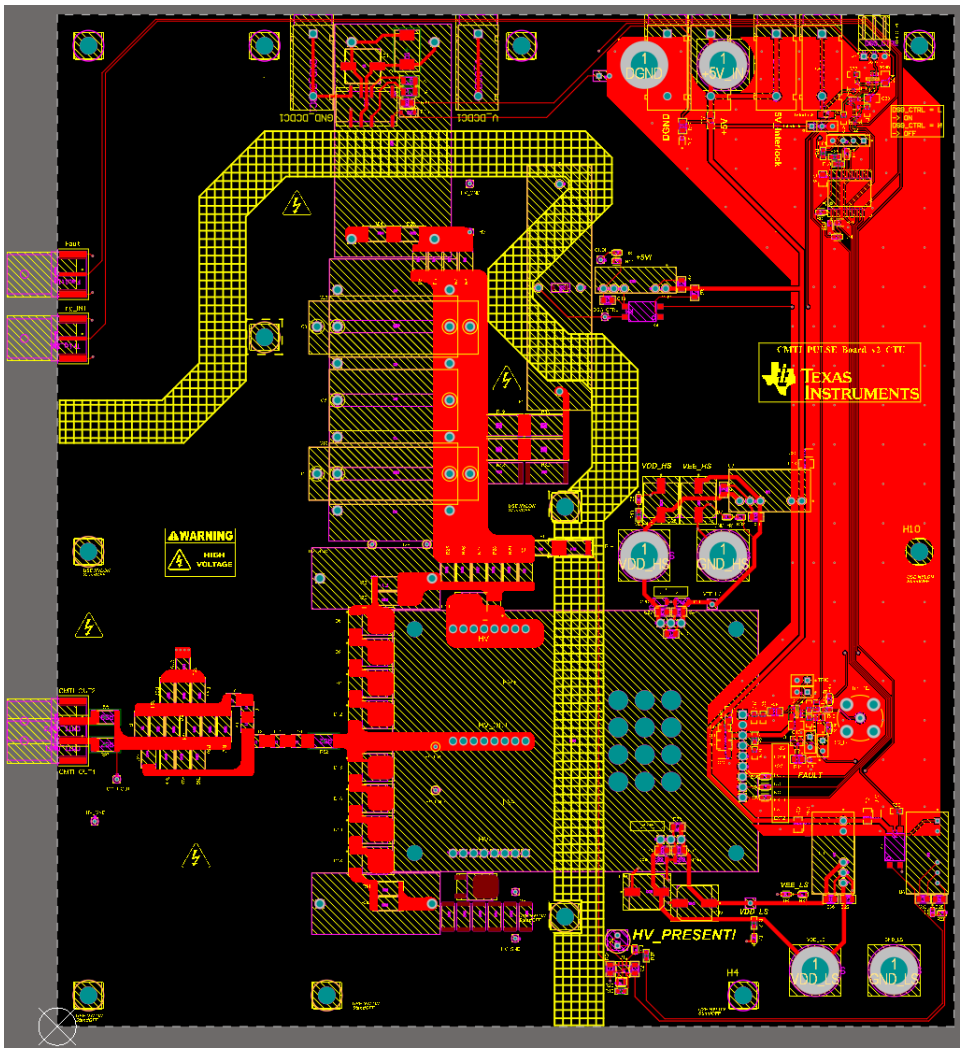


Figure 3.28: Top Layer of the PCB of the mother board

This location was chosen in order to shield the switch from the hot or cold air, which may be present in the test setup as the DUT board and the device will be tested over temperature range using thermostream. This may result in escape of the treated air into the box and the placement of the switch should prevent the immediate influence. As added benefit, this centres the half-bridge's +HV voltage terminal on top and supports heading of the power stage north. There are additional non-plated holes, whose purpose is to make it possible to check whether the switch is in place.

Above the switch, after the protection diode and the series resistors, there is the capacitor bank, which is forming the input high voltage stage together with the PICO DC/DC power supply module that is located on the bottom side for the same reason as the switch. Capacitor bank uses both sides as the capacitors alternate positions to allow for denser placement. The bigger capacitors with the wider footprint are located on the top side, so the user may decide which ones to populate. All of these capacitors are using sockets, so they can be exchanged without soldering according to the specific needs.

Next to the capacitor bank on the right, there is the discharge circuit, which is placed so that it can tap-off directly from the capacitor bank's positive node with the discharge resistors being on both sides of the board directly above each other in array. Next to the white relay, most of the control circuitry of the discharge is placed, alongside with its power supply. The rest is located next to the interlock connectors in the top-right corner of the board together with other parts of the control circuitry.

Above and underneath the switch on the left side, there are the protection series diodes and series resistors. On the right side, there are the connectors for the future implementation of variable supplies for low and high-side drivers with their respective power supply island with necessary passive components, signalling diodes and a connector for the external isolated variable module. Each of these islands has its own spare isolated DC/DC module to cover for it in the case when the isolated modules would not be available.

On the left side of the switch, there are the protection diodes and further right is the output filter and necessary probe points for measurement. This path leads straight into the output BNC connector. The connections are illustrated with the picture of the top layer in fig. 3.28. Below the center of the switch, there is the high voltage indication circuit that is tapping the capacitor bank using the two resistors next to the top side series resistors above the switch. Power supply for this circuit is placed in the bottom-right corner of the board so it will not interfere with the low-side driver supply.

The control part resides on the right side of the switch. The main part of the control circuitry is in the top-right corner of the board next to the connectors for main 5 V power supply and the interlock. Underneath these, the I^2C expander is located. The rest of the control circuitry is close to the control pins of the switch at its right side, together with probe points and alternative connections of the trigger for debugging purposes.

Fig. 3.29 reveals the connections in the bottom layer, showing mainly the high voltage ground connection and also the ground planes of the control side as well as the ones for both low-side and high-side driver power supplies. Lastly, next to the capacitor bank, the rest of the discharge resistor network is placed right underneath their top side counterparts, which can also be seen in fig. 3.30.

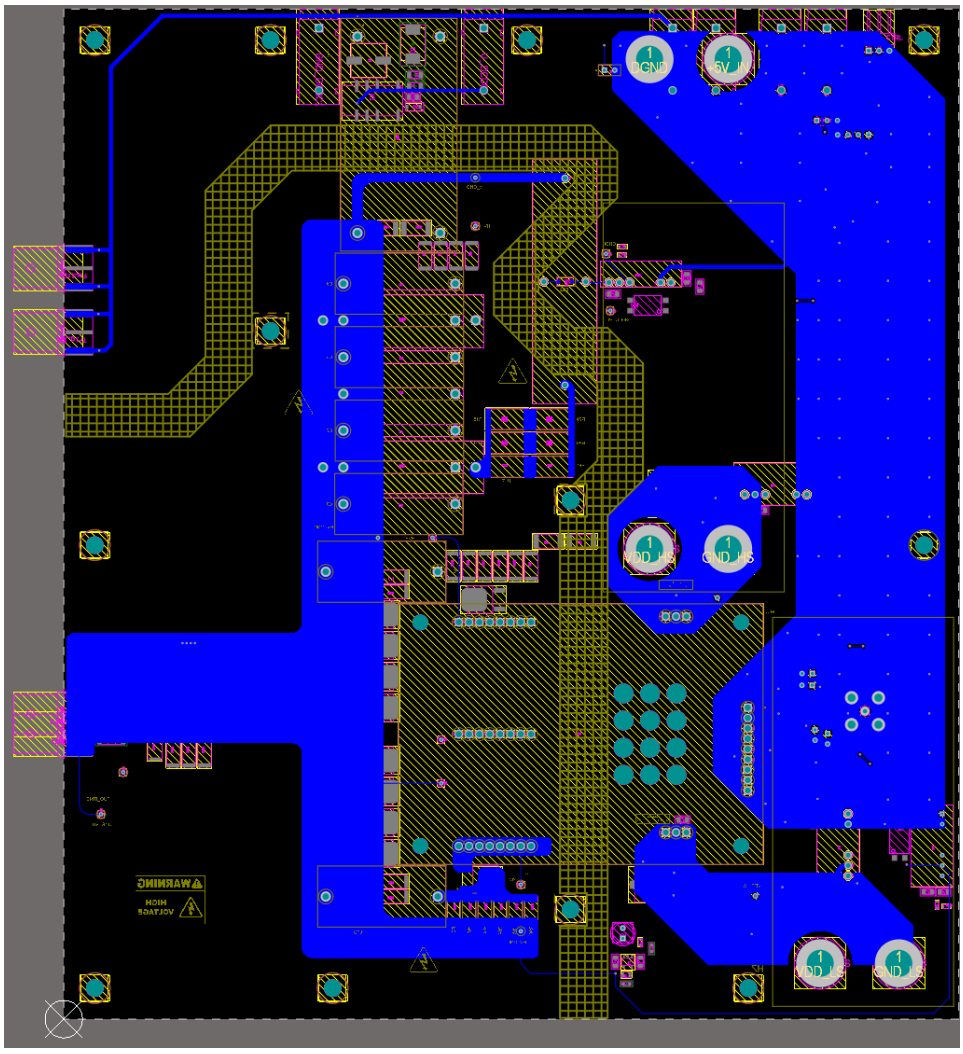


Figure 3.29: Bottom Layer of the PCB of the mother board

In the fig. 3.30, the bottom view of the mother board is shown, which reveals the rest of the circuits. The main components, such as the main high voltage DC/DC module, other side of the capacitor bank and the switch may be seen on the bottom side of the PCB. On the left side of the switch and above its the top-left corner, there are places dedicated for the variable isolated power modules. Whole board will be sitting on tall stand-offs, whose high will be later adjusted after the safety-box will be evaluated to provide sufficient spacing.

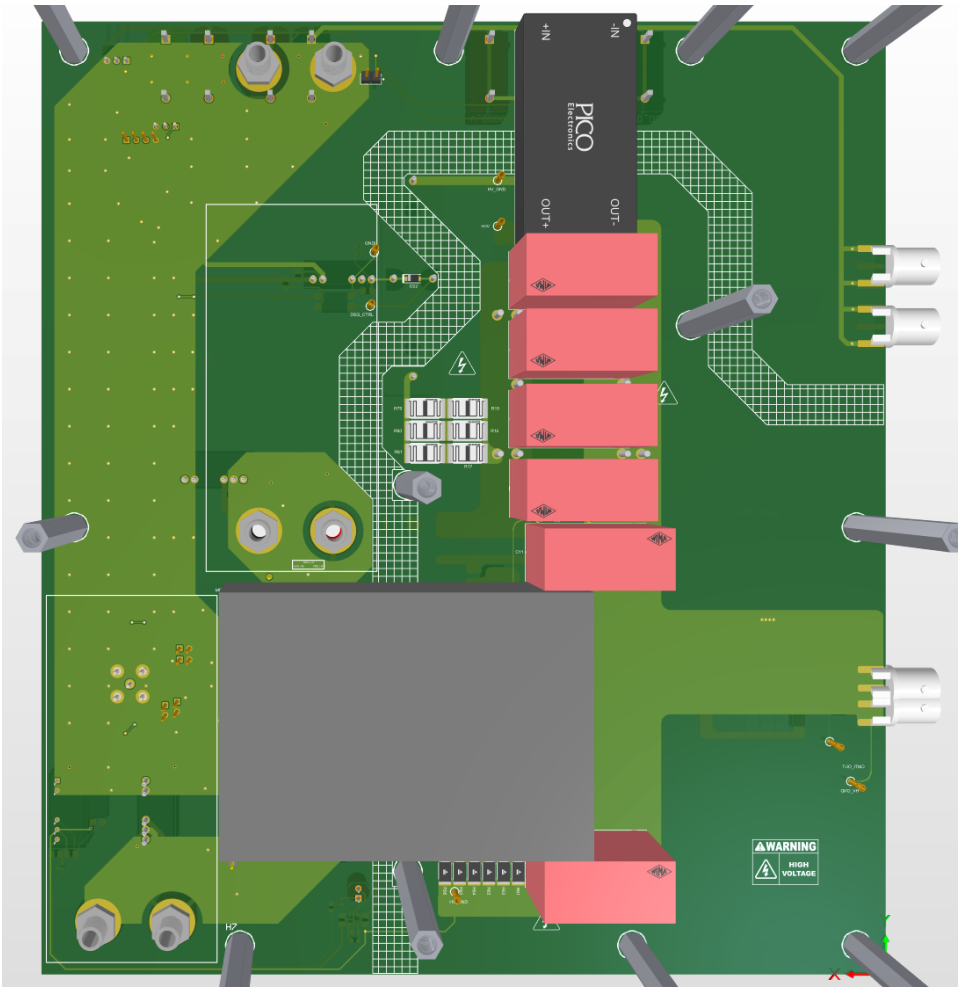


Figure 3.30: Bottom side of the 3D model view of the mother board

3.2.5 Assembly

Assembling process was done manually using soldering iron and hot air soldering iron. The process had to be done step by step with necessary verification in between in order to check the functions of the main and auxiliary circuits before the board would be tested as a whole. The process was following:

1. Firstly, the necessary sockets for the switch, power supplies, high voltage capacitors and other interchangeable through-hole mounted parts had to be soldered to enable quick swapping of these components.
2. Control side power supplies were assembled alongside with their respective indication LEDs. Firstly the discharge, then driver high-side and low-side ones and lastly the one for the high voltage indication circuit. The connectors for the laboratory power supplies were also soldered to enable providing power for the board. Board was powered up, all output voltages of isolated power supplies voltages were measured and checked, whether they are correct.
3. After this, the rest of the necessary circuitry was assembled to the discharge control in order to evaluate it. Digital multimeter was placed between the relay input and output pin in resistance measurement mode and the DSG_CTRL signal was applied alongside with INTERLOCK. The resistance change was observed to indicate that the discharge circuit switched.
4. Same principle was applied in order to verify the proper function of the relay switching the input power coming to the high voltage power supply.
5. In the control part, the trigger input into the switch was assembled and the function generator was connected and set to a burst of one pulse in order to verify the interaction of the trigger with the different INTERLOCK states. The results were observed on the oscilloscope as it was set to capturing the pulse at the input of the switch.
6. Then the high voltage indication circuit was assembled to provide notification about present high voltage. Together with this, the discharge circuit was completed. Both circuits were verified with connecting and turning on the HV power supply. This was measured with high voltage probe at the capacitor bank. The power supply was turned on and the LED switched on. Interlock was then disengaged and after circa 1 s the LED turned off, indicating the discharge time of the bank.
7. As the last thing, the switch will be evaluated. The series resistor networks were added together with protection diodes and the output

filter. High voltage probe was connected to the the output of the filter. The switch was triggered and the waveform was observed.

The completely assembled Mother board is shown in fig. 3.31.

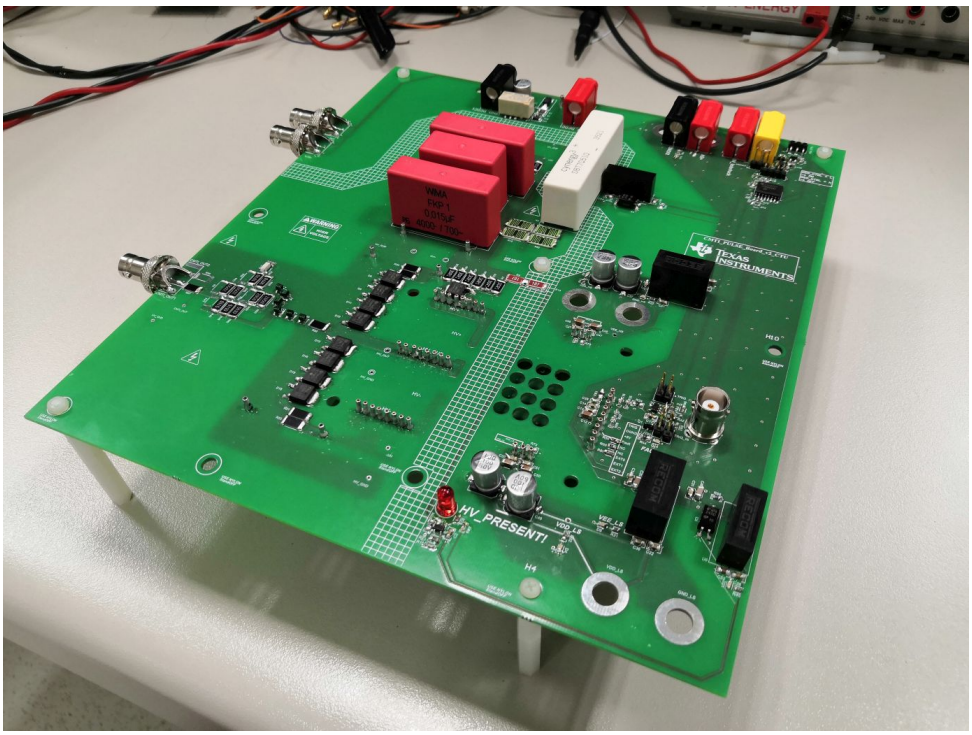


Figure 3.31: Assembled Mother board

Successfully passing the test on lower voltages lead to increase in voltage up to 1 kV. The rising edge of the pulse is displayed in fig. 3.32 and falling edge in fig. 3.33. These two waveforms match closely with expectations and show that the assembled board is working as desired. The results will be discussed in further detail in chapter 4.

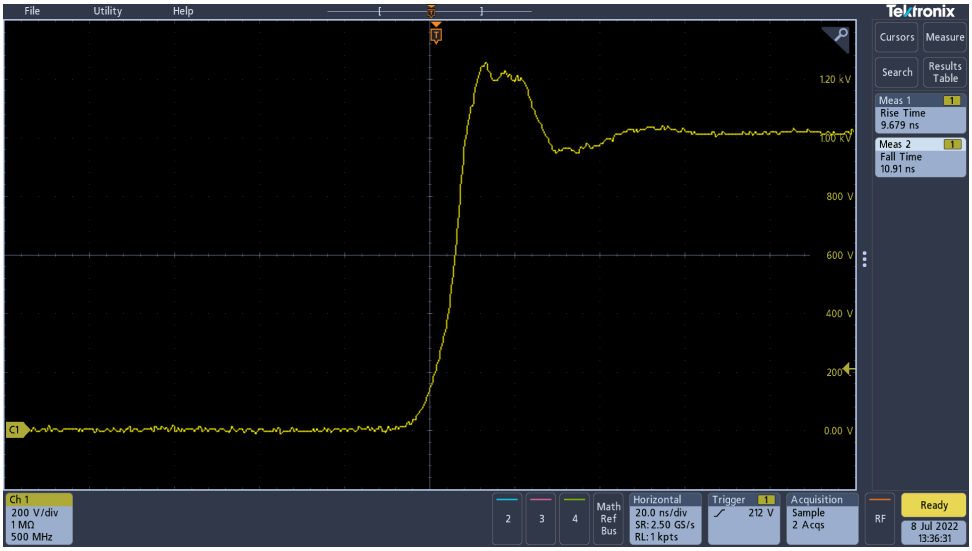


Figure 3.32: Rising Edge Half-Bridge Module 1000 V

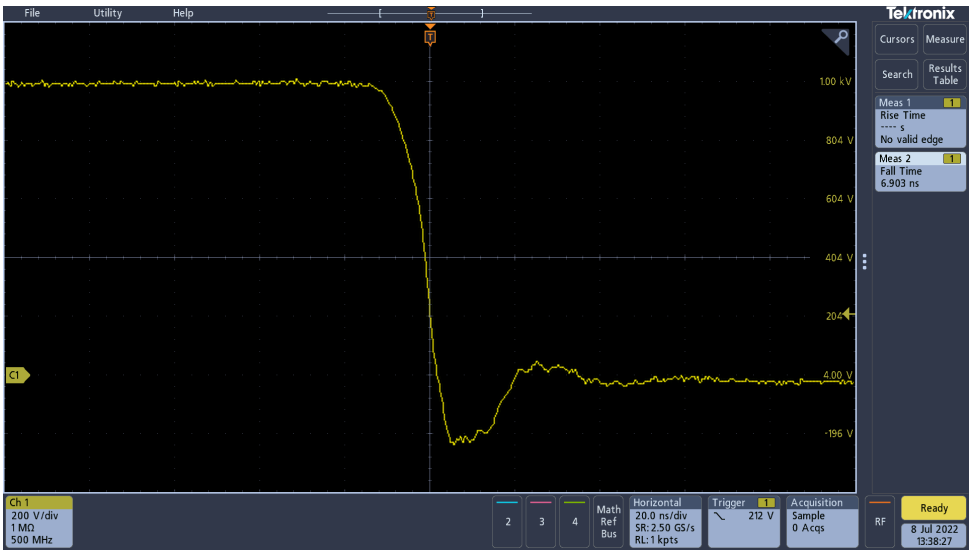


Figure 3.33: Falling Edge Half-Bridge Module 1000 V

With this, the verification and assembly of the mother board is finished and the focus of this work will shift towards the design of the daughter board.

3.3 Daughter board

With the reasons mentioned in section 3.2.2.1, it was decided to develop and verify a pin-to-pin replacement for the used integrated half-bridge module in order to eliminate the draw backs. The new daughter board would allow the evaluation of its capabilities in the same environment as it would fit into the same footprint and use the same output and support infrastructure. The daughter board would be also compatible with existing circuits on the mother board in order to keep it backwards compatible.

In the fig. 3.34, the high-level overview of the SiC Daughter Board is shown. The board consists of two silicon carbide MOSFETs, each driven by their respective isolated driver. It also includes isolated power supplies to provide the right voltages to drive SiC MOSFET.

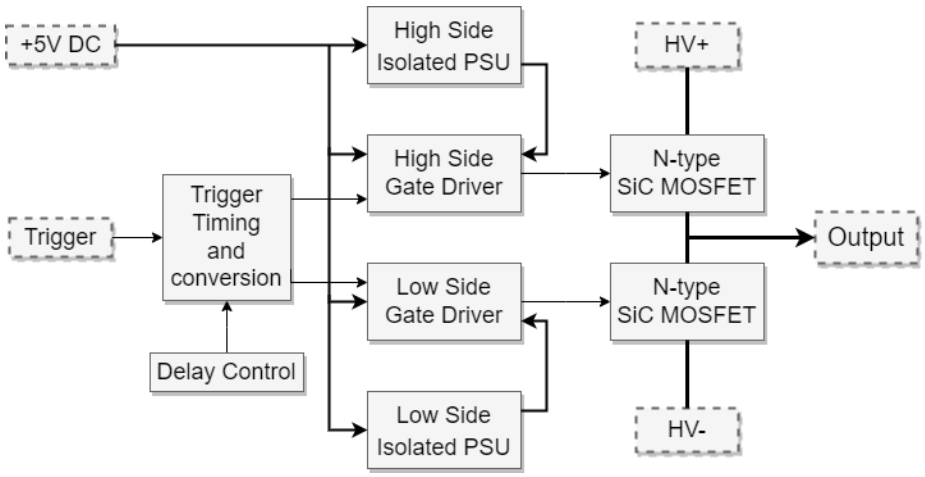


Figure 3.34: High-level overview of the SiC Daughter Board

All of this will be powered from 5 V coming directly from the mother board. At last, there is the control part, which is responsible for providing the correct inputs for the gate drivers. They both need to be driven by two signals and so to retain the interoperability with the half-bridge module, the input positive logic trigger must be converted.

3.3.1 Schematic

In this section, the schematic of the daughter board will be described. This board houses all necessary circuits to drive SiC MOSFETs in the half-bridge configuration and provides conversion from board input control signal to retain the positive logic.

The signals coming from or to the mother board are:

- Trigger
- 5 V - Main power supply
- HV+ - High Voltage positive terminal
- OUT - CMTI Pulse Output
- HV- - High Voltage negative terminal

In the next sections, each part of the board will be shown and described in detail.

3.3.1.1 Transistors

As per section 2.3, the requirements of the setup for voltage capability determined that silicon carbide MOSFETs will be used as switches. These types of transistors can be routinely found available on markets such as Mouser or DigiKey with blocking voltages up to 1700 V, which is an ideal solution for a pin to pin replacement to the half-bridge module with its maximum capability of 2 kV. These transistors are also relatively cheap, costing around 13€ per piece. In the end, the G3R160M17J by GeneSiC Semiconductor, shown in fig. 3.35, was chosen with its key features noted in tab. 3.3.

Other notable characteristics include the TO-263-7 package with 7 pins. It has dedicated gate source pin and SMD style assembly, which makes it superior in terms of switching losses to the conventional 3 and 4 pin packages of TO-247. Those packages experience much higher values of parasitics induced by the packaging. [43]

Table 3.3: Key characteristics of G3R160M17J SiC MOSFET [42]

Characteristic	Value
Drain-Source Voltage	1.7 kV
Gate-Source Voltage (static)	−5 V - +15 V
Gate-Source Voltage (Dynamic)	−10 V - +20 V
Turn-on rise time	12 ns
Turn-off rise time	10 ns
Pulsed Drain Current	32 A

The dedicated source pin is specially designed for gate driving, as it provides path for the gate current going away from the main source inductance, which is exposed to large current transients, when the transistor changes states. It also provides the driver with reference point to which its ground can be tied. [44]

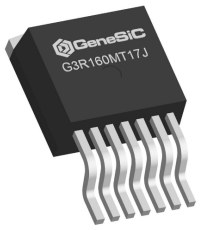


Figure 3.35: Utilized SiC MOSFET by GeneSIC [45]

3.3.1.2 Gate Drivers

As the selection of the transistor was discussed in the previous section, in this one the design of the gate driver is going to be described. The driver should be carefully picked as it determines and greatly influences the final behavior of the MOSFET. The key capabilities of the driver should be mainly in their ability to source or sink current since the faster the gate is charged, the faster the current will flow through the transistor as it turns on.

The other important requirements are namely desired bus voltage and whether it can be used as a high-side or a low-side driver. Also its important to consider timing characteristics as, if the desired configuration would be sensitive to potential miss-match between driver's turn-on and turn-off times, the transistors would encounter excess stress, which in some cases could be destructive.

With these considerations in mind, the 1ED3241MC12H gate driver from Infineon, shown in fig. 3.36, was chosen. It provides up to 18 A of sinking or sourcing capabilities, which is, in the affordable market, one of the best in class. It can drive IGBTs and various FET transistors including SiC MOSFETS. It offers two-level slew-rate control and has a capability to drive switches with bus voltages up to 2300 V. The timing characteristics are also respectable as IC-to-IC performance matching is down to maximum of 10 ns. Last but not least, it may be used as both a high-side and low-side driver. [46]

Figure 3.36: Gate Driver [46]

In the fig. 3.37, the schematic of the gate driver circuit can be seen. The input signals, coming from the control signal conversion and timing adjustment circuit, will be described in the following section. Together with resistors R4, R5, R8, R34, R17, R27, R29 and R37, shown in fig. 3.39, capacitors C6, C7, C14 and C15 form a RC filter, that may be used to suppress unwanted distortions on the input lines if deemed necessary.

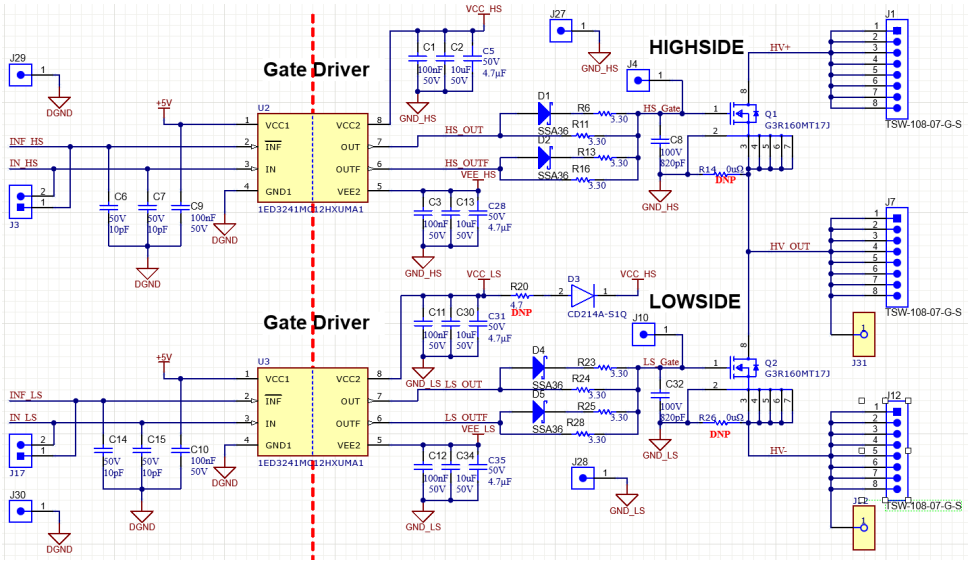


Figure 3.37: Gate Driver Circuit

Capacitors C10 and C9 are typical bypassing capacitors, providing the gate drivers with more stable power supply. Lastly on the input side, there are probe points J17, J3 and, together with ground probe points near (J29, J30), they allow for easy measurement of any combination of input signals.

In the fig. 3.38, the detailed look on the high-side is shown. First thing on the output side are the power supply capacitors. They provide the instantaneous current to support the switching requirements and assurance, that there is plenty of energy at the drivers disposal to drive the transistors. As the driver and the chosen FETs support switching gate with bi-polar power supply, there are two sets of capacitors associated with each driver. One set for the positive supply, the other one is for the negative power supply.

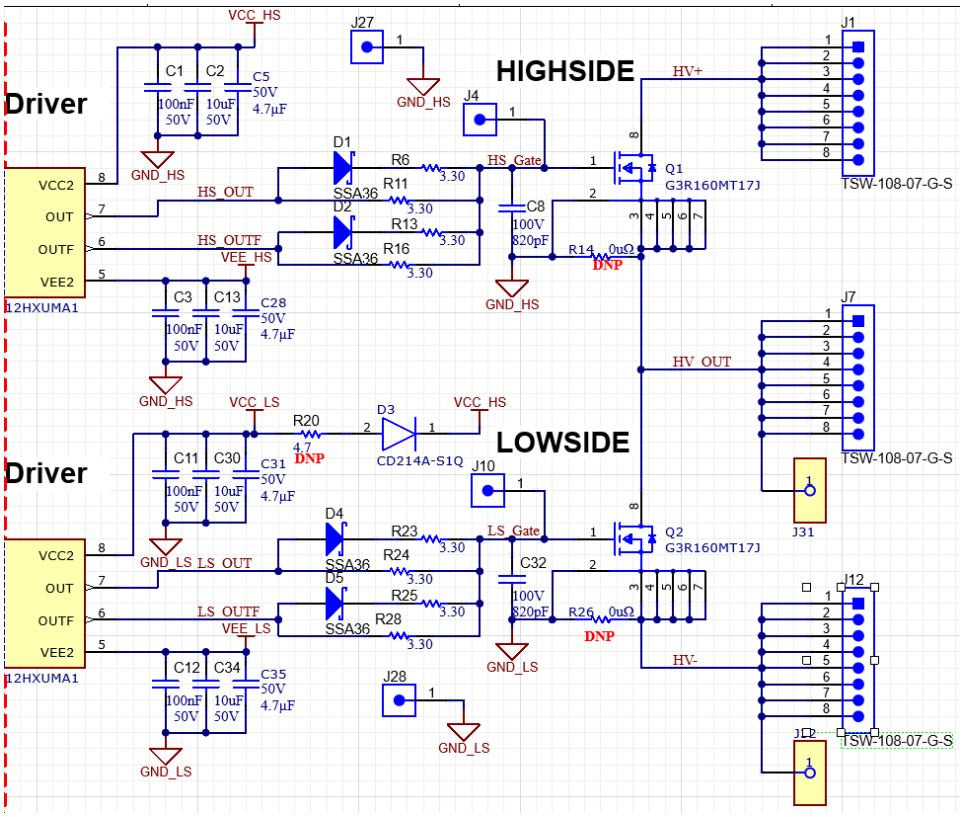


Figure 3.38: High-side Gate Driver Circuit in detail

Then there are two pins which are responsible for driving the transistor gate, OUT and OUTF. Their functionality is thoroughly described in section 3.3.1.3. Diodes D1 and D2 are in place because of the characteristics of the chosen SiC MOSFET. The G3R160MT17J has asymmetric turn-on and turn-off times, to put it into numbers, specifically 12 ns for turn-on, 10 ns for turn-off. [42]

This could influence the switching timing even more, so these diodes provide additional parallel resistors to reduce the gate resistance when charging the gate capacitance thus improving the turn-on characteristics. It's worth noting that if the turn-on and turn-off time of the transistor was identical, then no diodes would be required, and it is easy to manipulate diode direction or population state in order to adjust the circuit to different transistors.

Generally, the gate resistors function is to limit the inrush current to the gate and therefore damp the induced oscillations because, together with the parasitic inductance of the gate loop and gate capacitance, they form a series RLC circuit. On the other hand, increasing the value of the gate resistance is effectively slowing down the turn-on and turn-off times of the transistor. Increasing capacitance of the gate may also be a way to control potential oscillations, with the drawback of increasing the required energy provided by the driver in order to turn the transistor on or off.

The values in schematic were set empirically through measurements on the gate of the transistors as well as on the total output of the setup. A value of $3.3\,\Omega$ was found to be, together with a gate capacitor of $820\,\text{pF}$, a reasonable compromise. This gives following resistances for turn-on:

$$R_{turn_{on}} = R6||R11||R13||R16 = 0.825\,\Omega, \tag{3.11}$$

and for turn-off resistance it equals to:

$$R_{turn_{off}} = \frac{R11 \cdot R16}{R11 + R16} = 1.65\,\Omega. \tag{3.12}$$

The high-side transistor gate driver ground is connected to the source of the transistor Q1 through a Kelvin connection, specially designed to connect the reverse path for the gate current, so that the gate is not disturbed by inrush current through drain and source and its reaction with package inductance on the source pin. R14 is in place just for debugging purposes, normally it will not be populated. The low-side transistor gate driver and transistor are connected in identical manner.

3.3.1.3 Control signals

In the fig. 3.39, the schematic of the circuitry for conversion of the input signal is shown. Ultimately the input signal TRIG, coming from the mother board, needs to synchronously drive two separate gate-drivers, and additionally needs to be split to drive two signals of each gate driver, IN and INF. These signals

are responsible for controlling the two output signals of the gate driver, OUT and OUTF. OUT is a standard output signal following positive input logic on pin IN. The behavior of OUTF is determined by the state of the terminal INF at the moment of the input edge coming into the IN pin.

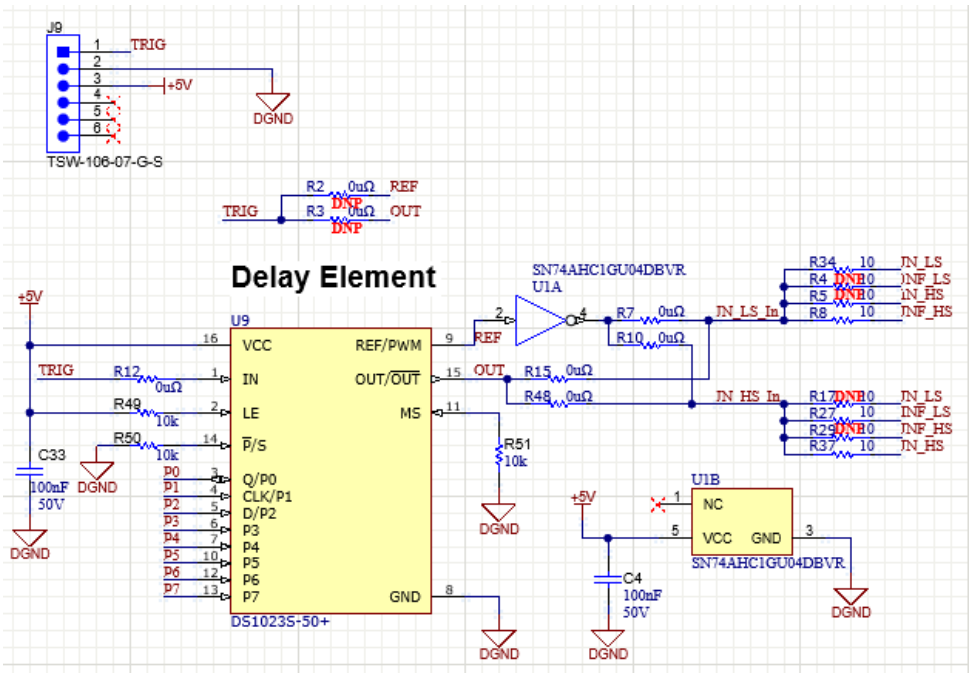


Figure 3.39: Schematic of the control signal conversion

Because there is a driver for each MOSFET in the half-bridge configuration, the single-ended input TRIG signal has to be converted into a time-aligned differential signal. With any logic gate or buffer, additional delay would be added to this differential control signal. Any undesired delay can result in a timing miss-match and thus an unbalanced turn on/off of the controlled transistors. The solution involves two logic elements. The first is a single inverter gate U1, SN74AHC1GU04DBVR, to create the inverted signal. This adds a constant/fixed delay against the original signal. The second is a programmable delay element U9 that is used to skew the second control signal to be slightly earlier, in-phase, or slightly later than the first signal.

Variable delay IC from Maxim Integrated, DS1023-50+, was chosen because of its versatility. It is produced in 5 versions according to what resolution of a time delay is needed. It supports parallel and serial communication for delay control. Because of its inherent step-zero delay, it provides a reference output, which is delayed by this base delay, and also output, which is then shifted by the value set with the interface. This results in accurate time shift between both signals.[47]

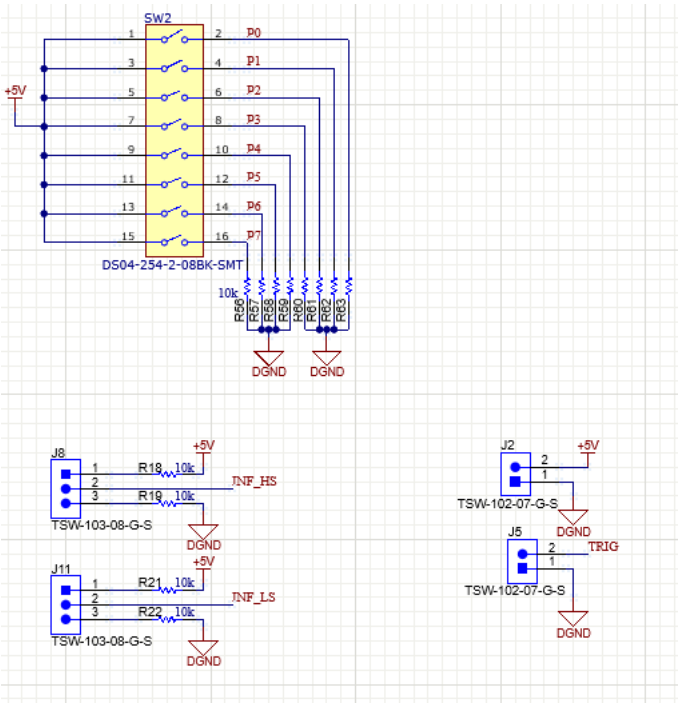


Figure 3.40: Delay control using a DIP Switch

This IC was also chosen because it provides a possibility to compensate for other miss-matches that could come from other sources like, for example, the gate driver, which also has a between-device propagation delay miss-match of up to 10 ns. [46] In order to set the delay, a DIP switch, shown in fig. 3.40, in combination with parallel network of resistors was used. This delay was then adjusted empirically after the board was assembled. There are also probe points to aid debugging and jumpers for the possibility of setting the INF signals into fixed states.

These resistors after the inverter and delay IC, shown in fig. 3.39, allow to set the direction of the added delay. By default, R7 and R48 will be populated, and R10 and R15 unpopulated, such that high-side input will be delayed with reference to low-side input. Rather, if R10 and R15 are populated instead, the low-side signal can be delayed. With this, the signals for the IN terminal of each driver were created. Now it remains to generate the second one, INF. The INF signals will be created according to what slew-rate setting will be needed as the driver offers two different possibilities. Their timing diagram is shown in fig. 3.41.

The input TRIG signal has been split into a buffered version and an inverted yet time-shift-programmable version. These two signals will be used to drive the 4 pins of the input to the isolated gate-drivers of high-side IN and INF

and the low-side IN and INF. Fig. 3.41 shows 2 control scenarios that are supported.

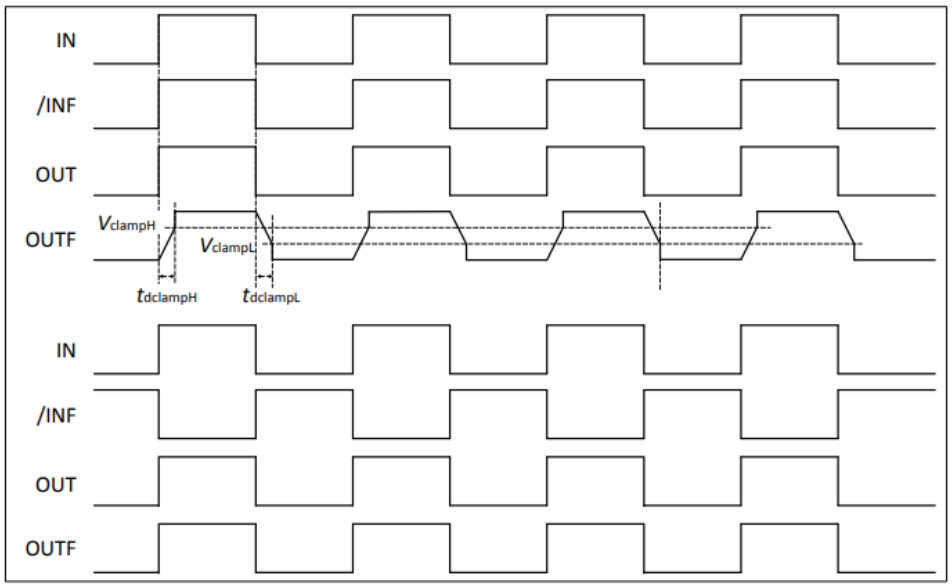


Figure 3.41: Timing diagram of 2 use-cases of input-output control scheme of 1ED3241MC12H [48]

In the top case, when IN and INF are driven identically and in phase, the OUTF is passively following behavior of the OUT pin, going into high impedance mode when the OUT pin is transitioning and then tying itself to the logic level of the pin as well. In this case the drive current is halved, so there is a reduction in the speed of turn-on or turn-off time of the transistor. In the bottom case in fig. 3.41, the OUT and OUTF are actively acting together, creating the maximum possible sourcing and sinking capability of 18 A. [46]

There are multiple methods to adjust slew-rate such as varying the high-voltage, modifying the filter, adjusting the gate voltage, etc and it was deemed that this gate-driver feature for slew-rate modification was not going to add enough value to explore. However, the option to evaluate this capability would still be implemented with the resistor network at the end of the delay circuitry, shown in fig. 3.39. This thesis will use the bottom case of the timing diagram, shown in fig. 3.41.

Resistors R4, R5, R8, R34, R17, R27, R29 and R37 together provide the ability to decide the desired combination of control scheme for the driver inputs. For the use-case of this thesis, the fastest possible slew-rate setting is required. To achieve this R34, R8, R27 and R37 will be populated.

3.3.1.4 Power supplies

The isolated power supplies are the last major part of the daughter board. As mentioned in section 3.3.1.1, the chosen SiC transistors have a capability to be driven with asymmetrical opposite supply common-mode voltages from −5 V to 15 V with dynamic range providing an overhead defined from −10 V to 20 V to allow for brief transient events.

The output side of the isolated gate driver has to stay isolated from sensitive control circuitry of the input side, so an isolated power supply has to be added. It is not that common, to find isolated power supplies with asymmetrical opposite outputs in order to avoid adding complexity in terms of using multiple power supplies.

There are few types, which have this capability, even though not exactly fitting this application. The chosen one is an isolated DC/DC converter R05P22005D from RECOM, shown in fig. 3.42. This power supply comes from a series specifically made for supplying drivers for various types of transistors, like IGBT and SiC, which require an asymmetrical power supply. It is made in a compact standardized SIP-7 package, so it may be interchangeable with many other isolated converters in the same package, if different voltages would be required.

Figure 3.42: R05P22005D Isolated DC/DC Converter from RECOM [49]

The R05P22005D is a 2 W PSU capable of delivering up to 50 mA on its 20 V output and 200 mA on its −5 V output. It offers a very high 6.4 kV isolation rating with very low isolation capacitance. It minimizes the bill of materials by integrating capacitors into the package, requiring only optional decoupling ones at the input and output. [49] The schematic is shown in fig. 3.43.

Even though they are not specifically required, there are bypassing capacitors on both sides of the isolated DC/DC converter for improved power supply robustness. On the output, there are optional resistors R1, R9, R32 and R33. These can form and output RC filter if the application would

require it. By default, these resistors will be populated with 0 Ω. Since the chosen transistors support only 15 V as the maximum common-mode positive voltage, there is a need to lower the positive supply from 20 V. To do this, s simple linear regulator circuit will be used.

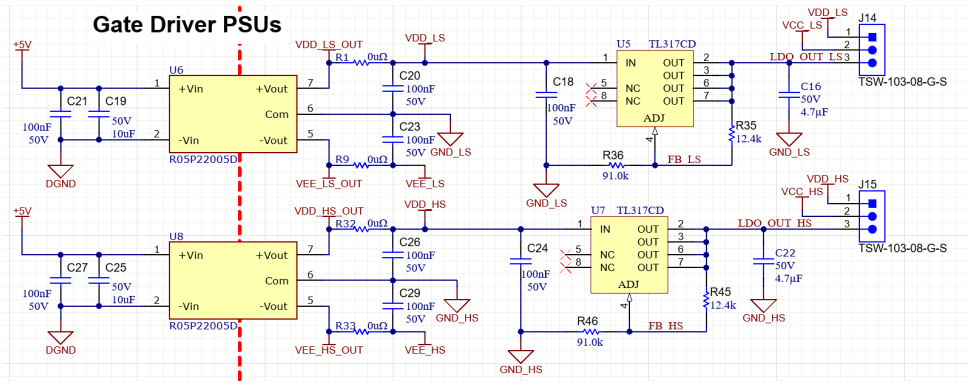


Figure 3.43: Schematic of Power Supplies for the Gate Drivers

Voltage on the positive supply will be lowered using a TL317CD from Texas Instruments, which is a 3 terminal adjustable linear voltage regulator with a capability to supply up to 100 mA of current. It can provide output voltages ranging from 1.25 V to 32 V, that are set with external resistor network. [50] The circuit, shown in fig. 3.43, follows recommended design that is described in the datasheet. The resistor network can be determined from the equation: [50]

$$V_O = V_{REF} \cdot (1 + \frac{R2}{R1}) + (I_{ADJ} \cdot R2). \tag{3.13}$$

In the schematic R1 = R35 and R2 = R36 for low-side power supply, R1 = R45 and R2 = R46 for the high-side one. Since both the high-side and low-side supply driver are identical, the following calculations apply for both of these circuits. The lower resistor will be set from available standard values as R2 = 91 kΩ. With $I_{ADJ} = 50\,\mu A$ and $V_{REF} = 1.25\,V$ [50], the equation is:

$$15\,V = 1.25\,V + 1.25\,V \cdot \frac{91\,k\Omega}{R1} + 50\,\mu A \cdot 91\,k\Omega \tag{3.14}$$

and when the equation is solved for R1, it can be transcribed as:

$$R_1 = \frac{1.25\,V \cdot R_2}{15\,V - 50\,\mu A \cdot R_2 - 1.25\,V} = \frac{113750}{9.2} = 12\,364\,\Omega. \tag{3.15}$$

The closest available value from the standard lines of resistors was 12.4 kΩ.

With the voltages set, the last piece in the schematic, in fig. 3.43, is the pin header at the end. This provides possibility for using either the output directly from the isolated DC/DC or the output from the LDO. This allows flexibility for the future, because some transistors may benefit from different configuration of the power supplies. Some may be rated only for uni-polar operation with maximum common-mode of 15 V and some may use up to 20 V. As a result, when V_{EE} would not be used, shorting pins 2 and 3 on the pin headers J19 and J20, shown in fig. 3.44, would enable to use uni-polar isolated DC/DC, which would fit into the standard SIP-7 footprint.

3.3.1.5 Auxiliary circuits and connectors

In the last section, the remaining auxiliary circuits and output connectors will be described. For the easement of debugging and future use, signalling LEDs are utilized, this enables to verify proper function of the board when powering up or during operation. These diodes are set to relatively low currents and therefore low luminescent ability, but still provide sufficient indication.

As the voltage drop over the green diodes D6, D7, D8 and D9, as shown in fig. 3.44, is around 2.1V. [51], the diode current, with chosen resistors, would be:

$$I_{LED_{V_{CC}}} = \frac{U}{R} = \frac{V_{CC} - V_{LED}}{R_{LED}} = \frac{15 - 2.1}{13\,\text{k}\Omega} \approx 1\,\text{mA} \tag{3.16}$$

$$I_{LED_{V_{EE}}} = \frac{U}{R} = \frac{V_{EE} - V_{LED}}{R_{LED}} = \frac{5 - 2.1}{3\,\text{k}\Omega} \approx 1\,\text{mA} \tag{3.17}$$

With these current values, the luminous intensity will be around 2 mcd [51], which has proven to be adequate for the application.

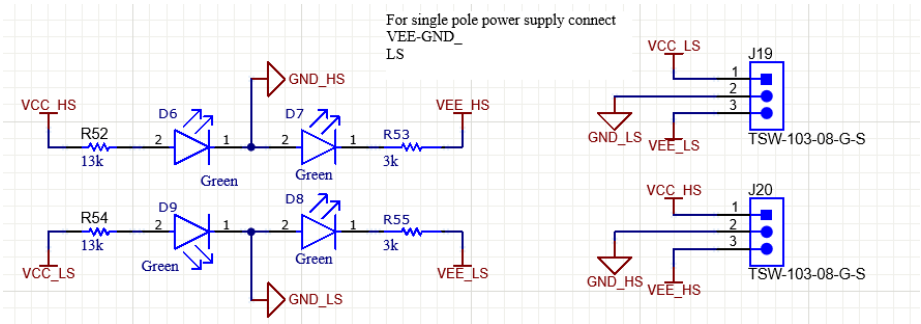


Figure 3.44: LEDs and pin headers for debugging purposes

The Daughter board will mate with the Mother board using pin headers with standard 2.54 mm spacing, which follows the footprint of the integrated

half-bridge module. This is done in order to maintain compatibility and allow to switch between the modules when needed. In total, one 6-pin and three 8-pin pin headers are used. One for each terminal HV+, HV-, OUT and the 6-pin one for the control interface.

All of these pin headers will mate with pin sockets on the mother board, which are shown in fig. 3.45. To allow for even greater flexibility in terms of power supply interchangeability, both isolated DC/DC converters are going to slot in the similar sockets as the daughter board will, so they can be swapped without soldering.

Figure 3.45: Socket to be used with Isolated DC/DCs [52]

3.3.2 Layout

With the schematic design completed, the PCB itself had to be designed. The size of this board is set by the dimensions of the integrated half-bridge module as it is supposed to be a compatible replacement. The physical proportions of the module and therefore the daughter board are then 89 mm by 64 mm. The pin headers, which are to be mated with the sockets on the mother board, are distributed so that they respect the module's footprint.

Since the dimensions are enough for the component density, it was decided to use 2-layer board to reduce cost and manufacturing time. Top layer will have all the necessary major components on it, while the count of the components on bottom layer will be kept to a minimum. This also helps with maintaining the integrity of the solid ground plane underneath the control part. [2] For the high voltage side of this board, the same general requirements for the high voltage layout guidelines apply as mentioned at the beginning of section 3.2.4.

Fig. 3.46 shows the top layer of the PCB and fig. 3.47 reveals the view of the Daughter board from the top. In the middle of the left side of the board, there is the control part, which sits next to the input pin header connector. The isolated power supplies, for supplying power to the gate drivers, are

located above and underneath it. Next to the each isolated DC/DC module, there are also the LDOs, pin headers for selecting the power supply input and signalling diodes for debugging purposes.

The control part, with the delay elements and a DIP switch underneath it, has the resistor network, for selecting the combination of the input signals to the gate driver, on its right-hand side together with the probe points. In the middle, there are the isolated gate drivers with all of their bypassing capacitors above and underneath each of them. On their right side the gate driving circuitry is located, including the resistors, diodes and gate capacitor, as close as possible to their respective gates of the transistors.

The right side of the board houses the transistors in between each connector. On the top, there is the high-voltage input, HV+, pin header and underneath it is the high-side transistor. Below it, there is the CMTI output connector, OUT, and when heading further down, the low-side transistor and the ground terminal for the high-voltage input, HV-, are placed respectively.

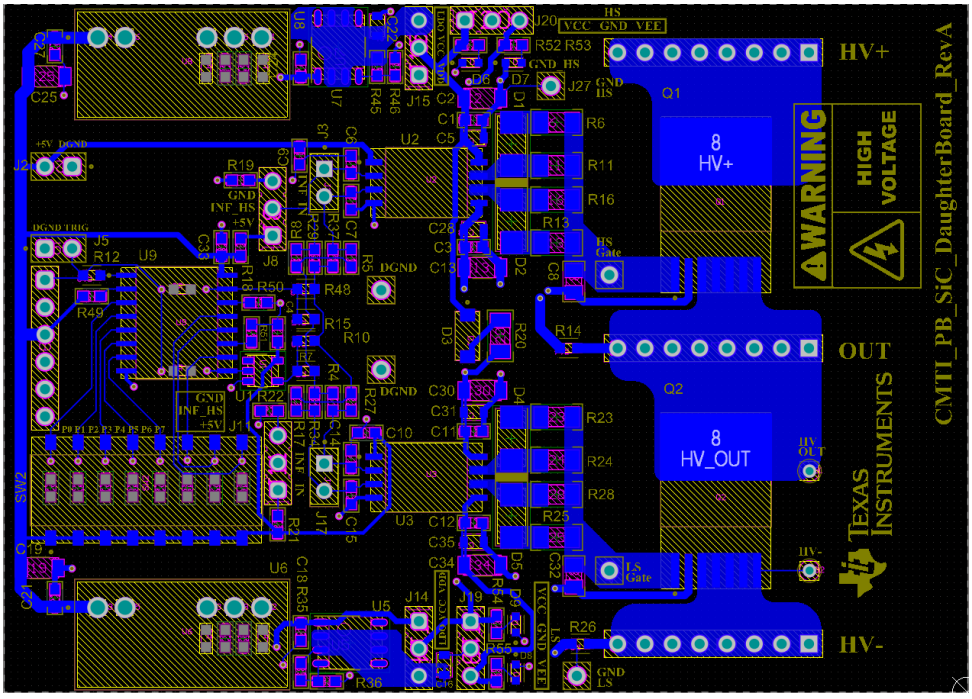


Figure 3.46: Top layer of the Daughter Board's PCB

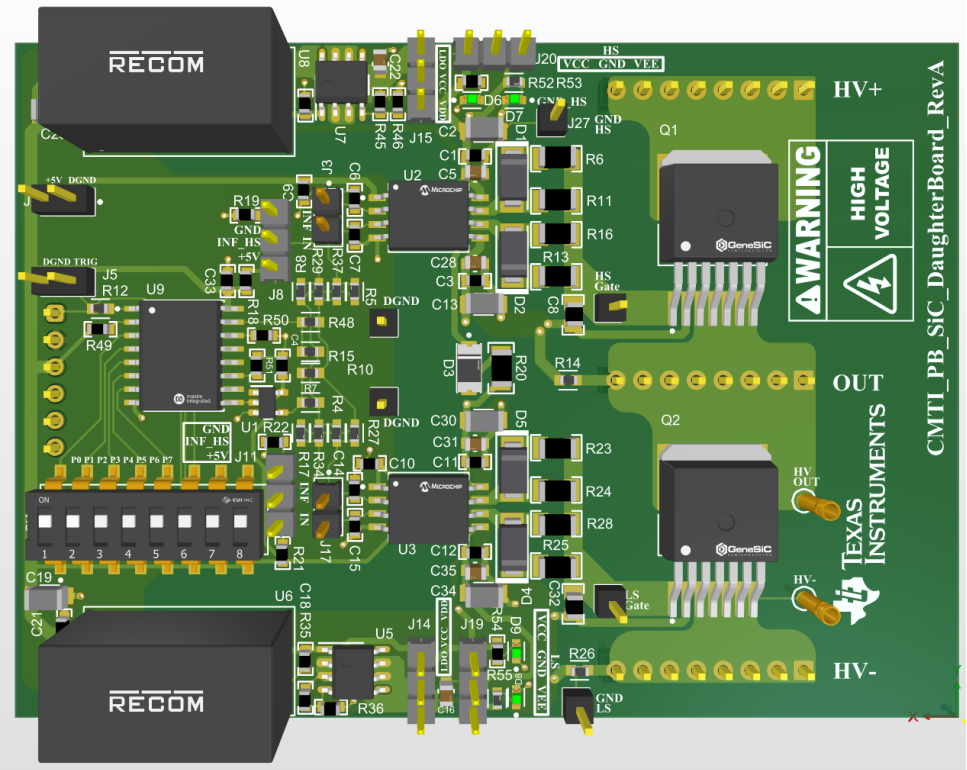


Figure 3.47: View from the top of the Daughter Board PCB Model

Each transistor's gate input, located to the left of its bottom pins, has its own dedicated source tap, next to the gate pin, used as the reverse path for the gate driving current. This forms the gate driving loop, which should be kept as short as possible. Next to the gate pins, there are also their respective probe points for measuring transistor's gate voltage. On the output side, there are also probe points for the high-voltage probe to allow to measure the output waveform right at its source.

In the fig. 3.48, the bottom side of the copper PCB layer can be seen. Because of the effort to maintain the integrity of the solid ground plane and easement of debugging, the number of components going to the bottom of the board was limited to a minimum. On the bottom side, the output connectors may be seen. These pin headers will mate to the sockets on the mother board.

There are also other less critical components such as the resistor network for the DIP switch, bypassing capacitors for the isolated DC/DC modules and bypassing resistors for disabling the delay element. It may be seen that the bottom layer, shown in fig. 3.49, is used mainly for power routing and individual grounds of the system, with the ground of the control part on the left and the respective grounds of each isolated gate driver above and

underneath it.

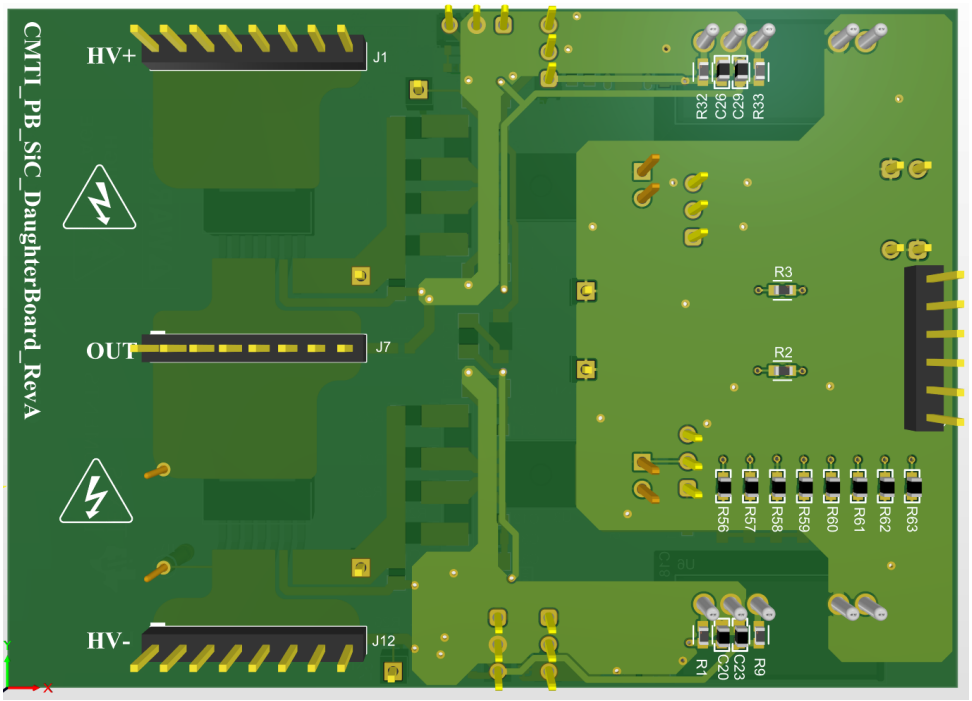


Figure 3.48: View from the bottom of the Daughter Board

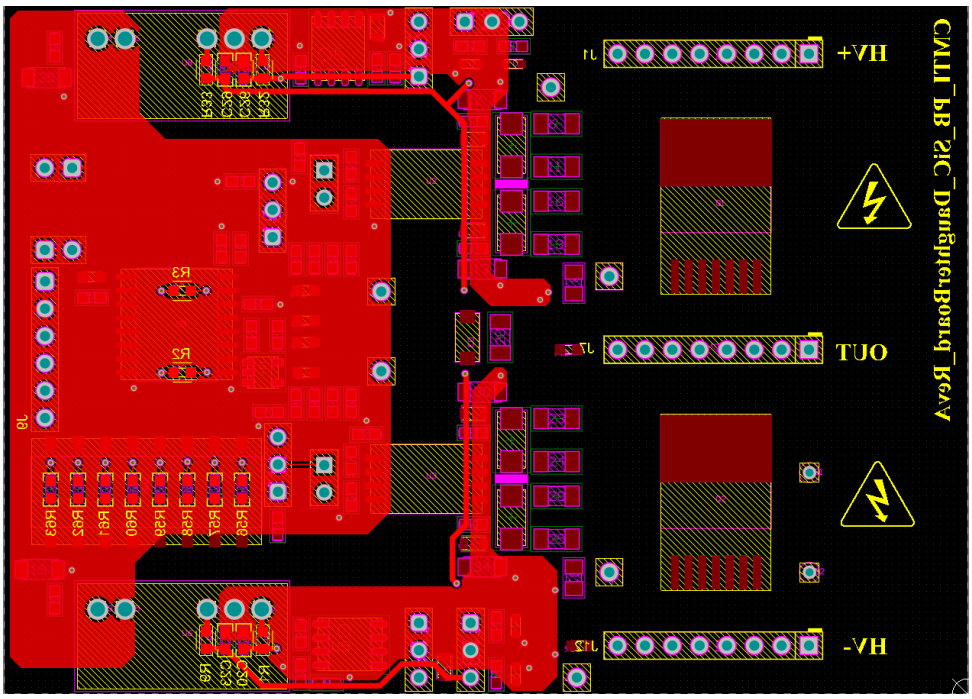


Figure 3.49: Bottom layer of the Daughter Board's PCB

3.4 Assembly

As with the mother board, the daughter board also utilized the same iterative assembly and verification process. Soldering up small blocks first, then individually testing them to verify their functions before the whole circuit would be verified. Assembled board prepared for testing is shown in fig. 3.50.

1. Firstly, the control part of the daughter board would be tested. The variable delay element was soldered together with the inverter gate and the passive components belonging to these parts. The probe points were set up and used to measure the rising edges at the input of the drivers. They were matched using the delay element with a delay of approx. 1.5 ns, which corresponds to the propagation delay of the inverter gate.
2. After this, power supplies on the low and high-side were assembled, together with their respective LDOs and indication LEDs. The voltage output on both isolated DC/DC converters and linear regulators was measured and verified to correspond with intended value.
3. All remaining passive elements were soldered alongside with the driver itself. Everything was powered up together for the first time and after settling, no shorts or other unusual behavior was observed. The trigger signal was then applied and the gates measured.
4. When the driver's output was verified, transistors were soldered and the board was slotted into the mother board to verify the output. Once the right output waveform was measured, the resistor values at the gates were tweaked with iterative process of changing the gate resistance and then measuring output of the gates and lastly the CMTI output.

The measured output waveform is shown in fig. 3.52 for the falling edge event and in fig. 3.51 for the rising edge event. These two waveforms match closely with expectations and show that the assembled board is working as desired. The results will be discussed in further detail in Chapter 4.

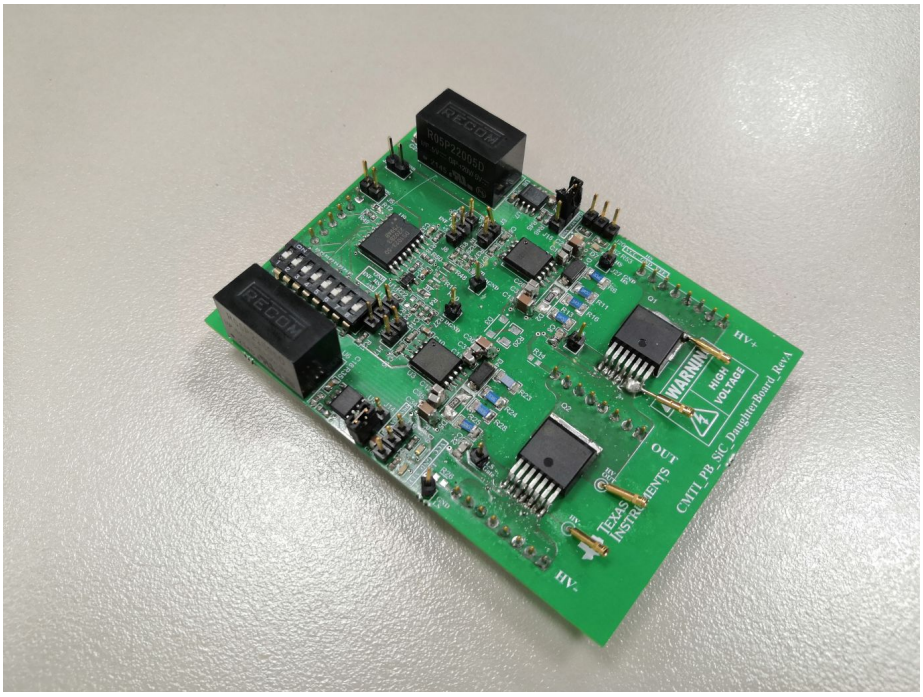


Figure 3.50: Assembled Daughter board

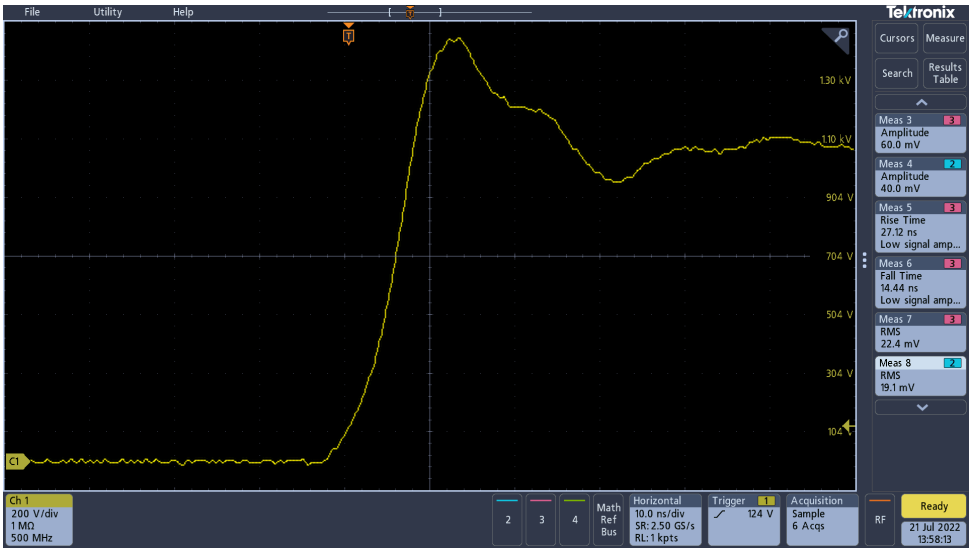


Figure 3.51: Rising Edge SiC Daughter Board at 1000 V

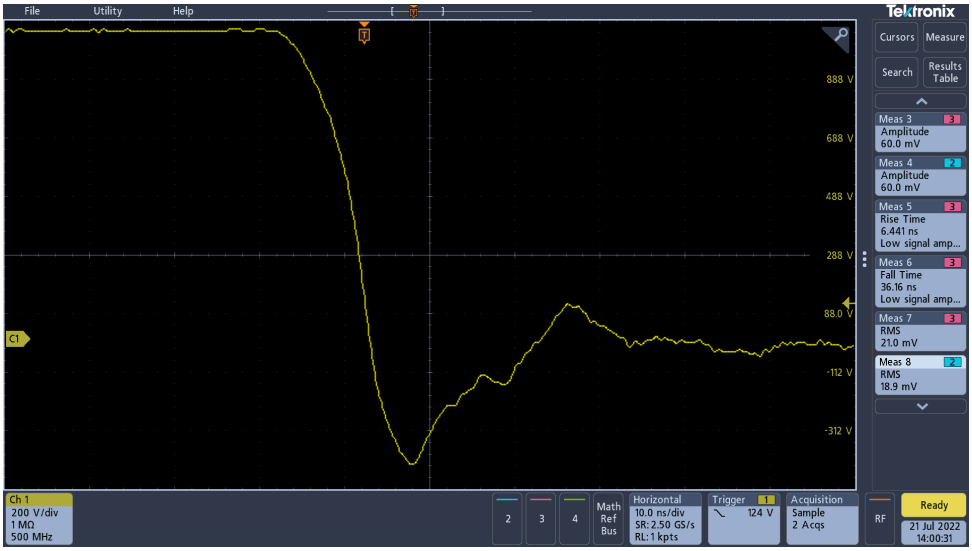


Figure 3.52: Falling Edge SiC Daughter Board at 1000 V

Chapter 4

Results and Discussion

In this chapter, the results of the implemented pulse board are presented and analyzed. A large focus of these results is on the slew-rate of the output waveform, as this is what will be used as the stimulus for CMTI testing purposes. Table 4.1 shows the different switches that had been evaluated throughout the development process

Table 4.1: Table of the tested switches

Switch	Driver	Transistor
Integrated Half-Bridge Module	-	-
SiC Daughter Board	1ED3241MC12H	G3R160M17J
Evaluation Board (EVM)	1ED3241MC12H	MSC750SMA170B

The presented version of the mother board is the second revision, as it incorporated many lessons learned from the fist one. The first revision supported the evaluation module (item 3 above in table 4.1) of the gate driver, which was also later used in the daughter board solution. They differed in the auxiliary circuits, where the driving circuits for the EVM were removed and reworked to a new control concept presented in section 3.3.1.3.

4.1 Evaluation Board

The EVM, an off-the-shelf purchasable evaluation module of the gate driver, was used to evaluate the performance of the gate drivers and first SiC

transistors. Many experiments were performed on this board and the gained knowledge was used for the development of the daughter board, discussed in detail in section 3.3. The EVM and daughter board share the same isolated gate drivers, but the daughter board features more capable SiC transistors and comes as a stand-alone replacement for the integrated half-bridge module.

The daughter board also improves upon the EVM by incorporating the isolated power supplies for the gate drivers of the transistors and the control part, which converts the input trigger signal into the needed control signals for the gate drivers, integrated on the board. The EVM control part featured many safety circuits which further worsened the results, adding miss-matches to the timing of the driver's control signals.

The resulting output waveforms of the EVM tested on the first revision of the mother board are shown in fig. 4.1 for the rising edge and fig. 4.2 for the falling edge.

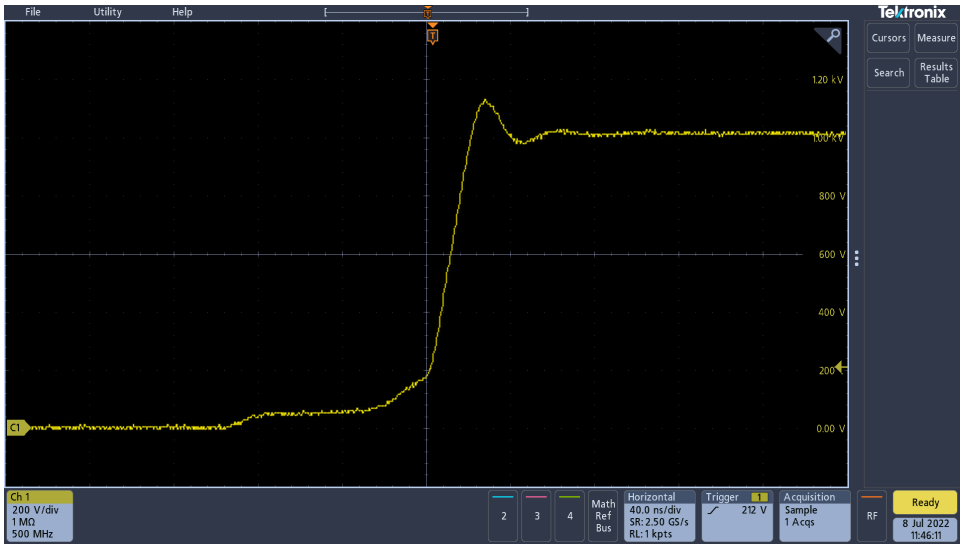


Figure 4.1: Rising Edge Evaluation Board at 1000 V

The waveforms in fig. 4.2 and fig. 4.1 show the issue with the transition quality early on for both edges. To improve this, the control part was completely reworked to provide the compensation for various timing miss-matches that could affect the switching waveform. To further improve it, additional capacitors were provided for the power supplies of the gate drivers to improve their robustness, together with adding many probe points for easement of the debugging process.

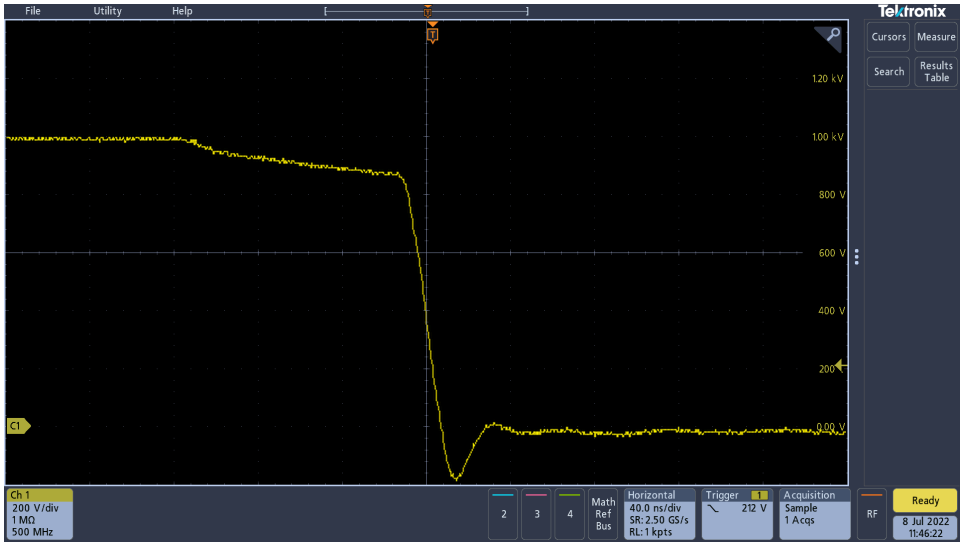


Figure 4.2: Falling Edge Evaluation Board at 1000 V

4.2 Slew-Rate comparison

As mentioned previously, the ultimate goal is to achieve a high-voltage high slew-rate pulses with good pulse quality such that this pulse board can be used for CMTI testing. In table 4.1, three HV half-bridge modules were mentioned, and in this section the slew-rates of their output waveforms will be compared.

In the context of CMTI analysis, and for a rising or a falling edge event, the slew-rate is analyzed as 20% to 80% of the edge's transition with regards to peak to peak voltage. The reasons for this definition were described in section 2.2.1.5. The equation for the slew-rate may be then written as:

$$\begin{aligned} V_{peak_{80\%}} &= (V_{max} - V_{min}) \cdot 80\% + V_{min} \\ V_{peak_{20\%}} &= (V_{max} - V_{min}) \cdot 20\% + V_{min} \\ SR_{V_{peak_{20\%-80\%}}} &= \frac{V_{peak_{80\%}} - V_{peak_{20\%}}}{t_{@V_{peak_{80\%}}} - t_{@V_{peak_{20\%}}}} [\mathrm{V\,s^{-1}}]. \end{aligned} \tag{4.1}$$

All three half-bridge solutions from table 4.1 were tested at 3 different settled voltages (also known as common-mode voltage) 500 V, 1000 V and

1500 V. The output was measured after the filter and, to simulate the device under test, 100 pF load capacitor was added, which has been estimated to be on average the load capacitance that the pulse board would pulse into.

The results for the rising edge of all three solutions are shown in fig. 4.3 and the numeric results shown in tab. 4.2.

Table 4.2: Rising Edge Performance Comparison

Voltage	EVM	Half-Bridge Module	SiC DB
500 V	33.5 V ns^{-1}	48.35 V ns^{-1}	69.5 V ns^{-1}
1000 V	43.8 V ns^{-1}	117.45 V ns^{-1}	151.2 V ns^{-1}
1500 V	48.9 V ns^{-1}	170.7 V ns^{-1}	193.15 V ns^{-1}

It may be seen that the daughter board achieves overall better resulting slew-rates than the integrated half-bridge module on all three common-mode voltages. The difference being the largest on the lowest voltage, 500 V, where the difference was around 43% in favour of the daughter board. This delta would come down as the common-mode voltage increases to approximately 13% also in favor of the DB on the highest voltage. The maximum slew-rate achieved was 193 V ns^{-1}.

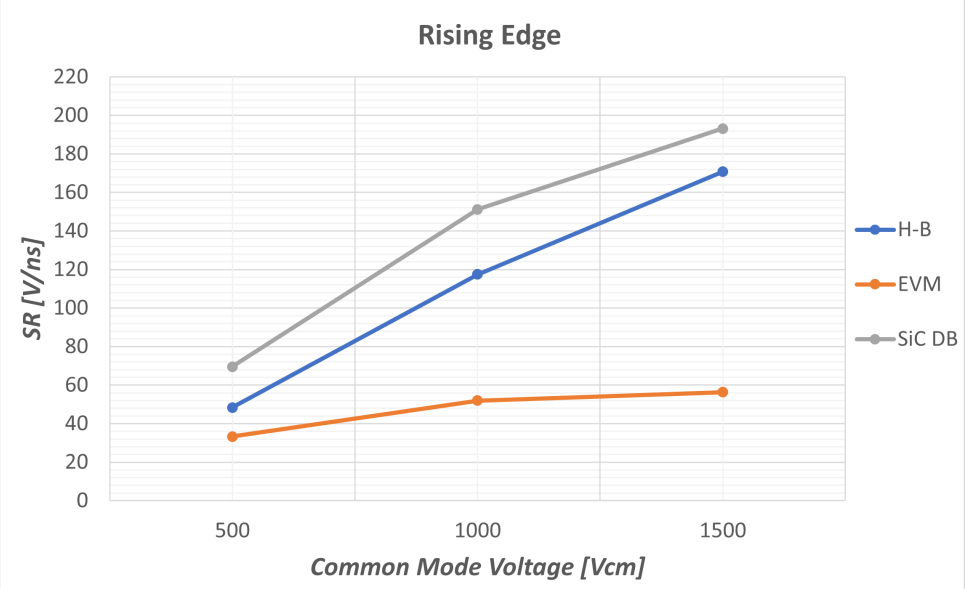


Figure 4.3: Comparison of the slew-rates of rising edges for various switches

In the fig. 4.4, the falling edge data for all three solutions are presented alongside with their numeric counterparts in tab. 4.3. Here a much bigger improvement over the Half-Bridge module may be seen as its falling edge has general deficit to its own rising edge. This may be observed over the

whole common-mode voltage range. On the 500 V common-mode voltage the difference reaches 59% in favor of the daughter board and on the highest voltage it comes down to 29%, while achieving 204 V ns^{-1}.

Table 4.3: Falling Edge Performance Comparison

Voltage	EVM	Half-Bridge Module	SiC DB
500 V	33.3 V ns^{-1}	43.2 V ns^{-1}	68.1 V ns^{-1}
1000 V	52.1 V ns^{-1}	106.8 V ns^{-1}	148.6 V ns^{-1}
1500 V	56.3 V ns^{-1}	157.5 V ns^{-1}	204.3 V ns^{-1}

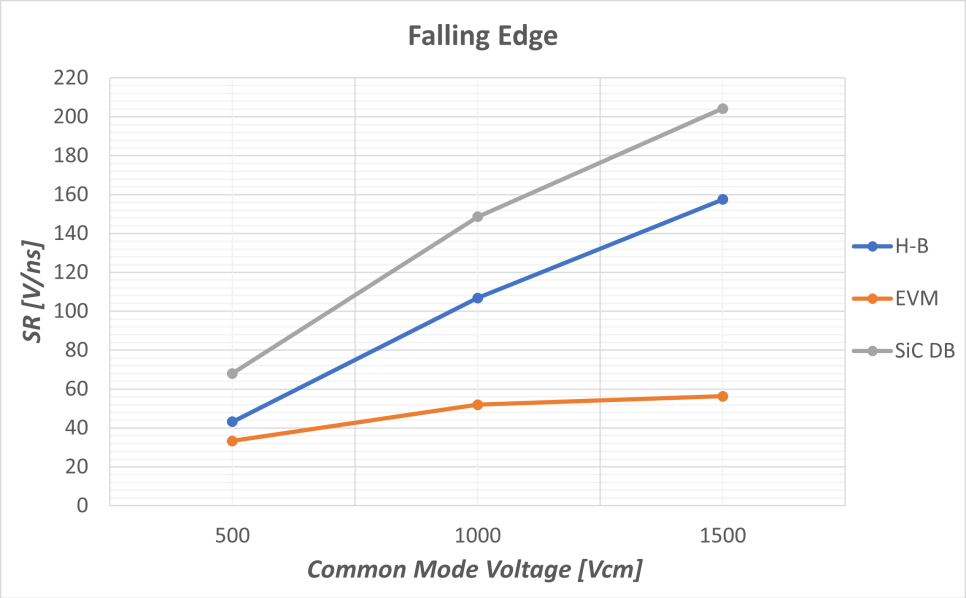


Figure 4.4: Comparison of the slew-rates of falling edges for various switches

The last comparison was done to explore the linearity of the change in the slew-rate with increasing common-mode voltage. The slew-rate was measured over a broader range from 100 V to 1500 V with 100 V steps to determine if there are any notable points of concern. Any issues in the perceived linearity of the slew-rate to common-mode voltage relation would pose an issue to the integrity of the CMTI test, this curve should be as linear as possible.

The results may be seen in fig. 4.5. This chart shows that beyond approximately 1300 V the slew-rate change of the rising edge starts to not respect the linearity set with the results for the lower voltages. This behavior is not apparent on the falling edge, which seems to continue in a more linear trend. The results were taken as a single measurement with an oscilloscope, so additional averaging, with more samples on one voltage, could obtain more accurate results.

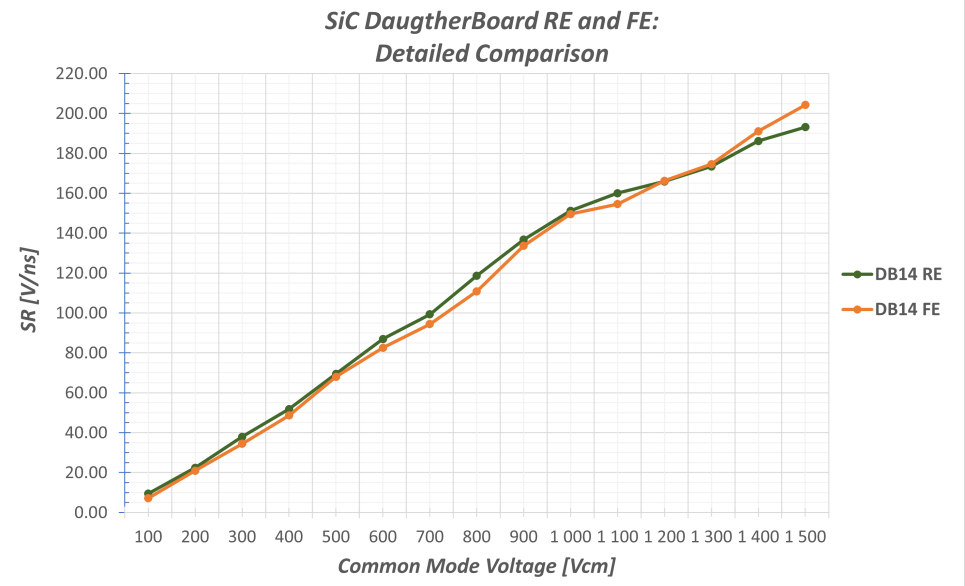


Figure 4.5: Detailed Comparison of the slew-rates of the Daughter Board

Chapter 5

Conclusion

The goal of this master thesis was to design, manufacture and verify the functionality of a new Pulse Board, which will be used in Common-Mode Transient Immunity testing in a lab environment. This board is responsible for generating voltage pulses with variable slew-rates to allow accurate testing of the performance of isolated analog to digital converters, used mainly in power applications for current sensing, for example in motor drives and power inverters. The Pulse Board is composed of two boards, the mother board and the daughter board. In this thesis, the following goals were achieved:

- In the theoretical part, in the second chapter, different types of isolation principles for data transmission over the isolation barrier were presented and compared. Followed with definition of different parameters that are being used to characterize the isolation capability of the barrier, including the CMTI test. At the end of the theoretical part, the traditional Si MOSFET was described and compared with new emerging types of wide-bandgap devices such as the silicon carbide, SiC, and gallium nitride, GaN, transistors.
- In the practical part, in the third chapter, the overall requirements for the solution were defined alongside with the high-level overview of the testing setup. Using Altium Designer 22, the schematic of both the daughter board and the mother board was designed and thoroughly described.
- Third chapter also defines the physical restrictions for the newly designed setup. In it the printed circuit boards of both solutions were designed, assembled and systematically verified.

- In the fourth chapter, using the mother board as a platform, the behavior of the daughter board was tested with measuring slew-rates at the output of the board. This performance was then compared to the previous solution, which was also evaluated using the mother board.

After the extensive evaluation and comparison, the overall achieved results may be summarized as following. The newly designed SiC Daughter board:

1. Outperforms the previous solution by 59% on the falling edge slew-rate and by 43% on the rising edge for the lowest measured common-mode voltage of 500 V. On the highest common-mode voltage, 1.5 kV, the falling edge is improved by 29% and the rising edge by 13%.
2. It maintains fairly linear performance over the measured common-mode voltage range.
3. Its waveform integrity is good and appears like a standard rise/fall edge of a square wave.
4. Can achieve slew-rates in a range from $10\,\mathrm{V\,ns^{-1}}$ to $200\,\mathrm{V\,ns^{-1}}$, which makes it a viable replacement for the existing solution.
5. The performance of the rising and falling edge mirrors well and even outperforms the existing solution.
6. The newly designed solution is pin-to-pin compatible replacement to the existing solution.

To improve this solution even further, the programmable voltage sources for the gate drivers could be developed. Achieving the ability to manipulate the turn-on and turn-off times of both transistors, through the change of the driving voltage. This enables the potential of changing the dt component in the definition of the slew-rate, which would, together with the already implemented variation of dV, provide complex possibilities to test for example the same slew-rates at different voltages.

References

1. *Design Fundamentals of Implementing an Isolated Half-Bridge Gate Driver* [online]. Analog Devices [visited on 2022-07-24]. Available from: https://www.analog.com/en/technical-articles/isolated-half-bridge-gate-driver.html.
2. ZÁHLAVA, Vít. *Návrh a konstrukce desek plošných spojů: principy a pravidla praktického návrhu*. Praha: BEN - technická literatura, 2010. ISBN 978-80-7300-2.
3. HASSE, P.; ELECTRICAL ENGINEERS, Institution of. *Overvoltage Protection of Low Voltage Systems*. Institution of Engineering and Technology, 2000. Energy Engineering. ISBN 9780852967812.
4. VOBECKÝ, Jan; ZÁHLAVA, Vít. *Elektronika*. Prague: GRADA, 2005. ISBN 978-80-247-1241-3.
5. GRAF, R.F. *Modern Dictionary of Electronics*. Elsevier Science, 1999. Electronics & Electrical. ISBN 9780750698665.
6. *Optocoupler Physical Layout* [online]. unknown [visited on 2022-07-10]. Available from: https://en.wikipedia.org/wiki/Galvanic_isolation#/media/File:Optoisolator_topologies_both.svg.
7. COLTMAN, J.W. The Transformer [historical overview]. *IEEE Industry Applications Magazine*. 2002, vol. 8, no. 1, pp. 8–15. Available from DOI: 10.1109/2943.974352.
8. *Transformer* [online]. Unknown [visited on 2022-07-24]. Available from: https://en.wikipedia.org/wiki/Transformer.
9. *Anatomy of a Digital Isolator* [online]. David Krakauer [visited on 2022-07-24]. Available from: https://www.analog.com/en/technical-articles/anatomy-of-a-digital-isolator.html.

10. *Designing with Digital Isolators* [online]. Texas Instruments [visited on 2022-07-24]. Available from: https://www.ti.com/lit/an/slyt335/slyt335.pdf?ts=1659287727150&ref_url=https%253A%252F%252Fwww.google.com%252F.

11. *Capacitive Isolation: A Fundamental Building Block in Future AC/DC Power Conversion* [online]. Zhihong Yu [visited on 2022-07-24]. Available from: https://www.monolithicpower.com/en/capacitive-isolation-article.

12. NASIRI, Adel; ALTIN, N.; OZDEMIR, Saban; CUZNER, Robert. Review of Standards on Insulation Coordination for Medium Voltage Power Converters. *IEEE Open Journal of Power Electronics*. 2021, vol. PP, pp. 1–1. Available from DOI: 10.1109/OJPEL.2021.3065813.

13. *Safety in Electronics Design* [online]. Würth Electronics [visited on 2022-07-24]. Available from: https://www.we-online.com/web/en/electronic_components/news_pbs/blog_pbcm/blog_detail-worldofelectronics_46078.php.

14. *Considerations for Selecting Digital Isolators* [online]. Luke Trowbridge [visited on 2022-07-24]. Available from: https://www.ti.com/lit/an/slla426/slla426.pdf?ts=1659290886245&ref_url=https%253A%252F%252Fwww.google.com%252F.

15. *High-voltage reinforced isolation: Definitions and test methodologies* [online]. Texas Instruments [visited on 2022-07-24]. Available from: https://www.ti.com/lit/wp/slyy063/slyy063.pdf.

16. *Surge Testing of Digital Isolators* [online]. Analog Devices [visited on 2022-07-24]. Available from: https://www.analog.com/ru/technical-articles/surge-testing-of-digital-isolators.html.

17. *New Product Update: High-voltage isolated I2C* [online]. Texas Instruments [visited on 2022-07-24]. Available from: https://www.ti.com/lit/ml/slyp777/slyp777.pdf.

18. *High Frequency TDDB of Reinforced Isolation Dielectric* [online]. Texas Instruments [visited on 2022-07-24]. Available from: https://www.ti.com/lit/ml/slyy191/slyy191.pdf?ts=1659719270707&ref_url=https%253A%252F%252Fwww.google.com%252F.

19. *MOSFET Physics* [online]. Texas Instruments [visited on 2022-07-24]. Available from: https://www.ti.com/lit/an/slua909/slua909.pdf?.

20. *MOSFET* [online]. The Amazing World of Electronics [visited on 2022-07-24]. Available from: https://elamazing.com/2021/03/31/mosfet/.

21. *MKS Instruments Handbook: Semiconductor Devices and Process Technology* [online]. TMKS Instruments [visited on 2022-07-24]. Available from: https://www.mks.com/n/mosfet-physics.

22. STEVANOVIC, Ljubisa D.; MATOCHA, Kevin S.; LOSEE, Peter A.; GLASER, John S.; NASADOSKI, Jeffrey J.; ARTHUR, Stephen D. Recent advances in silicon carbide MOSFET power devices. In: *2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*. 2010, pp. 401–407. Available from DOI: 10.1109/APEC.2010.5433640.

23. LI, Huan; WANG, Jue; REN, Na; XU, Hongyi; SHENG, Kuang. Investigation of 1200 V SiC MOSFETs' Surge Reliability. *Micromachines*. 2019, vol. 10, p. 485. Available from DOI: 10.3390/mi10070485.

24. ROCCAFORTE, Fabrizio; GRECO, Giuseppe; FIORENZA, Patrick; IUCOLANO, Ferdinando. An Overview of Normally-Off GaN-Based High Electron Mobility Transistors. *Materials*. 2019, vol. 12, no. 10. ISSN 1996-1944. Available from DOI: 10.3390/ma12101599.

25. DIMITRIJEV, S. SiC power MOSFETs: The current status and the potential for future development. In: *2017 IEEE 30th International Conference on Microelectronics (MIEL)*. 2017, pp. 29–34. Available from DOI: 10.1109/MIEL.2017.8190064.

26. GRECO, Giuseppe; IUCOLANO, Ferdinando; ROCCAFORTE, Fabrizio. Review of technology for normally-off HEMTs with p-GaN gate. *Materials Science in Semiconductor Processing*. 2018, vol. 78, pp. 96–106. ISSN 1369-8001. Available from DOI: https://doi.org/10.1016/j.mssp.2017.09.027.

27. *TCA9534A Low Voltage 8-Bit I2C and SMBUS expander datasheet* [online]. Texas Instruments [visited on 2022-07-24]. Available from: https://www.ti.com/lit/ds/symlink/tca9534a.pdf.

28. *VV-SERIES 1-5 kVDC OUTPUT Isolated, Single Output Modules* [online]. PICO Electronics [visited on 2022-07-24]. Available from: https://www.picoelectronics.com/node/13287.

29. *Panasonic Non-Latching Relay, 4.5V dc Coil, 1A Switching Current Datasheet* [online]. Panasonic [visited on 2022-07-24]. Available from: https://eu.mouser.com/datasheet/2/315/ds_61022_en_txs-2934307.pdf.

30. *Panasonic Non-Latching Relay, 4.5V dc Coil, 1A Switching Current* [online]. Panasonic [visited on 2022-07-24]. Available from: https://sg.rs-online.com/web/p/power-relays/8718241.

31. *WIMA FKP 1 Family Picture* [online]. WIMA GmbH [visited on 2022-07-24]. Available from: https://eu.mouser.com/ProductDetail/WIMA/FKP1Y026807I00MSSD?qs=RB4whv9F6rxCdbzIdLZiwQ%3D%3D.

32. *WIMA FKP 1 Family Datasheet* [online]. WIMA GmbH [visited on 2022-07-24]. Available from: https://eu.mouser.com/datasheet/2/440/WIMA_FKP_1-1139839-1880538.pdf.

33. *HVC Series Datasheet* [online]. Ohmite Mfg Co. [visited on 2022-07-24]. Available from: https://www.ohmite.com/assets/docs/res_hvc.pdf.

34. *TLP240D, TLP240DF Datasheet* [online]. TOSHIBA [visited on 2022-07-24]. Available from: https://eu.mouser.com/datasheet/2/408/TLP240D_datasheet_en_20200204-1075474.pdf.

35. *Probe Points: 1305-0-15-15-47-27-04-0* [online]. Mill-Max [visited on 2022-07-24]. Available from: https://www.mouser.de/ProductDetail/Mill-Max/1305-0-15-15-47-27-04-0?qs=zH5E5oA7rL%252BYQRYVe9Cs9Q%3D%3D.

36. *Pin Socket: 5050864-8* [online]. TE Connectivity AMP Connectors [visited on 2022-07-24]. Available from: https://www.digikey.com/en/products/detail/te-connectivity-amp-connectors/5050864-8/813493?s=N4IgTCBcDaIKwAZEA4BsAWAtMkBdAvkA.

37. *CRCW-HP-e3 resistor series Datasheet* [online]. Vishay [visited on 2022-07-24]. Available from: https://www.mouser.de/datasheet/2/427/crcwhpe3-1713858.pdf.

38. *Amphenol 031-70526-13 Datasheet* [online]. Amphenol RF [visited on 2022-07-24]. Available from: https://s3-us-west-2.amazonaws.com/catsy.582/C31-70526-XX.pdf.

39. NASTASE, Adrian S. *How to Derive the RMS Value of Pulse and Square Waveforms* [online] [visited on 2022-07-24]. Available from: https://masteringelectronicsdesign.com/how-to-derive-the-rms-value-of-pulse-and-square-waveforms/.

40. *High Voltage Printed Circuit Design and Manufacturing Notebok* [online]. Robert Tarzwell and Ken Bahl [visited on 2022-07-24]. Available from: https://www.smps.us/pcbtracespacing.html.

41. *PCB Trace Spacing Calculation for Voltage levels* [online]. Lazar Rozenblat [visited on 2022-07-24]. Available from: https://www.magazines007.com/pdf/High-Voltage-PCDesign.pdf.

42. *G3R160MT17J 1700V 160mOhm SiC MOSFET* [online]. GeneSiC Seminconductor [visited on 2022-07-24]. Available from: https://eu.mouser.com/datasheet/2/169/G3R160MT17J-2449134.pdf.

43. DENK, Fabian; HAEHRE, Karsten; EIZAGUIRRE CABRERA, Santiago; SIMON, Christoph; HEIDINGER, Michael; KLING, Rainer; HEERING, Wolfgang. RDS(on) vs. inductance: comparison of SiC MOSFETs in 7pin D2Pak and 4pin TO-247 and their benefits for high-power MHz inverters. *IET Power Electronics*. 2019, vol. 12, no. 6, pp. 1349–1356. Available also from: https://ietresearch.onlinelibrary.wiley.com/doi/10.1049/iet-pel.2018.5838.

44. *CoolMOS C7 650V Switch in a Kelvin Source Configuration* [online]. Infineon [visited on 2022-07-24]. Available from: https://www.infineon.com/dgdl/Infineon+-+Application+Note+-+TO-247-4pin+-+650V+CoolMOS+C7+Switch+in+a+Kelvin+Source+Configuration.pdf?fileId=db3a30433e5a5024013e6a9908a26410.

45. *G3R160MT17J* [online]. GeneSiC [visited on 2022-07-24]. Available from: https://www.mouser.de/ProductDetail/GeneSiC-Semiconductor/G3R160MT17J?qs=zW32dvEIR3uu8Xpb7yFpOA%3D%3D.

46. *Datasheet EiceDRIVER™ 1ED32xxMC12H* [online]. Infineon [visited on 2022-07-23]. Available from: https://www.infineon.com/dgdl/Infineon-EiceDRIVER_1ED32xxMC12H-DataSheet-v02_00-EN.pdf?fileId=5546d46278d64ffd01790e8498044865.

47. *DS1023 Datasheet* [online]. Maxim Integrated [visited on 2022-07-23]. Available from: https://eu.mouser.com/datasheet/2/256/DS1023-1291890.pdf.

48. *1ED324xMC12H, 1ED325xMC12H - Technical description* [online]. Infineon [visited on 2022-07-23]. Available from: https://www.infineon.com/dgdl/Infineon-AN-2021-03_Technical_description_1ED324xMC12H_1ED325xMC12H-ApplicationNotes-v01_00-EN.pdf?fileId=5546d46278d64ffd01790e849f6d486b.

49. *RxxP2xxyyD Series Datasheet* [online]. RECOM [visited on 2022-07-24]. Available from: https://eu.mouser.com/datasheet/2/468/RxxP2xxyy-1709962.pdf.

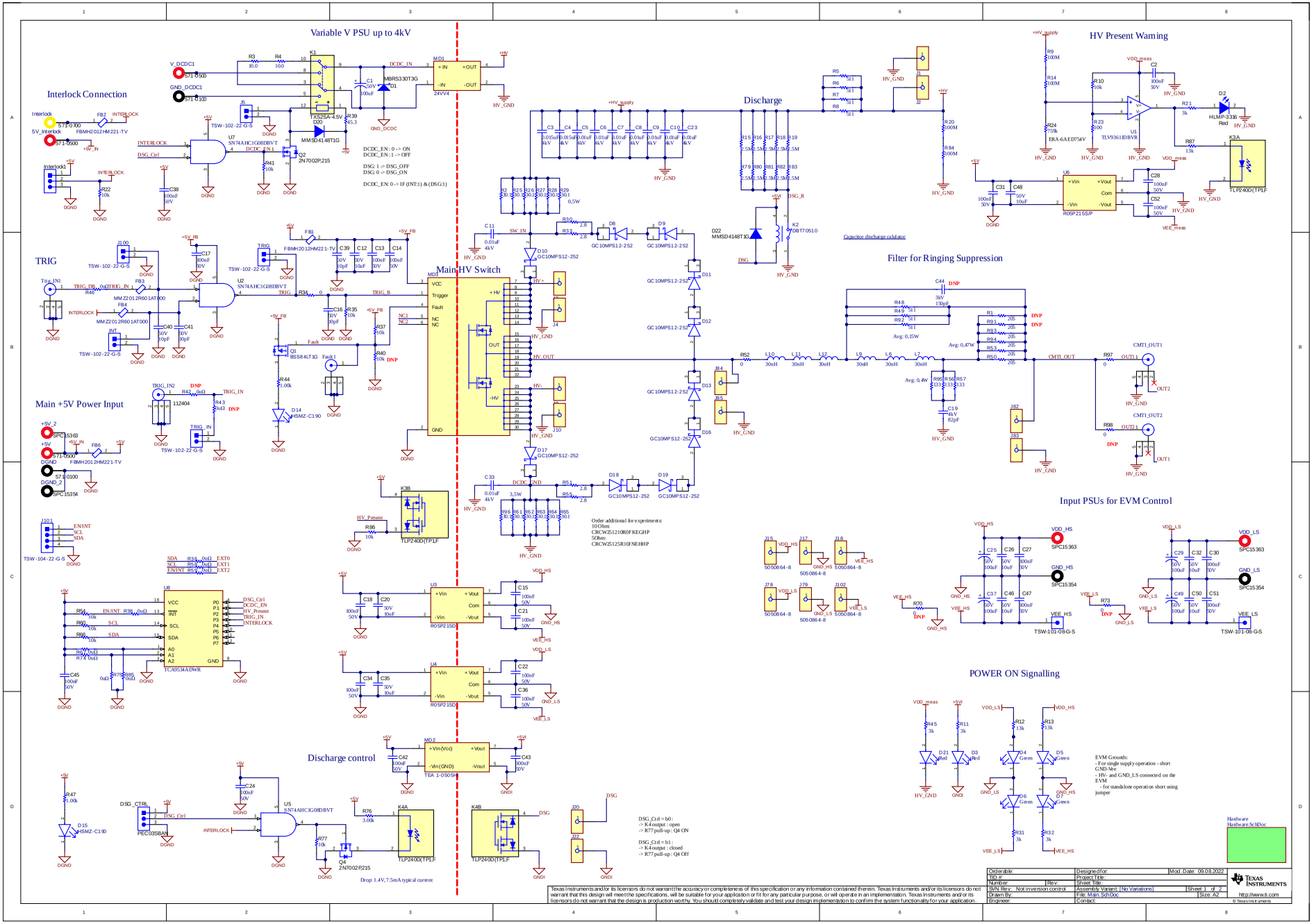
50. *TL317 100-mA 3-Terminal Adjustable Positive Voltage Regulator* [online]. Texas Instruments [visited on 2022-07-24]. Available from: https://www.ti.com/lit/ds/symlink/tl317.pdf?HQS=dis-mous-null-mousermode-dsf-pf-null-wwe&ts=1658667290605&ref_url=https%253A%252F%252Fcz.mouser.com%252F.

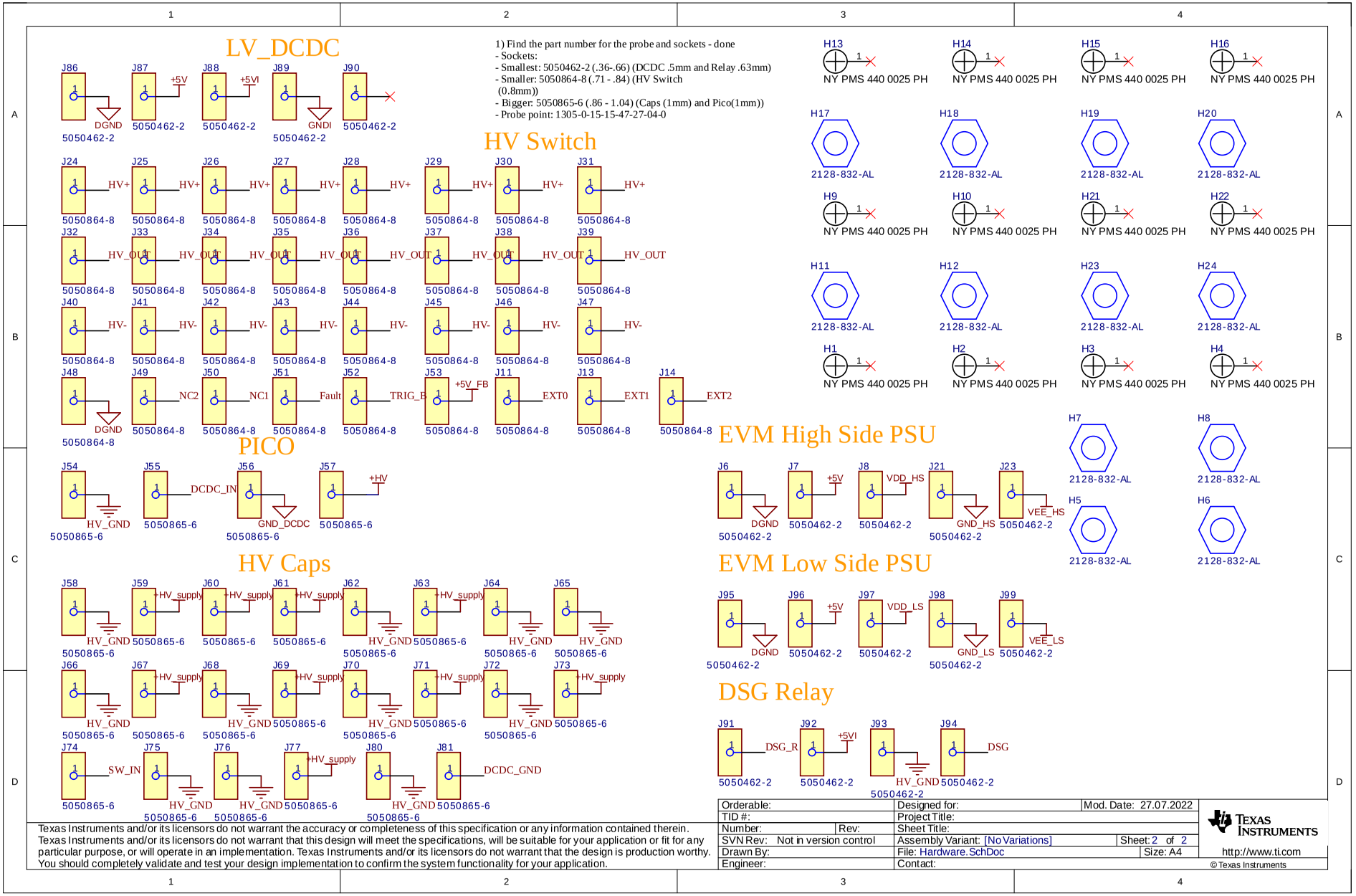
51. *150060VS75000 Green LED* [online]. Würth Elektronik [visited on 2022-07-24]. Available from: https://eu.mouser.com/datasheet/2/445/150060VS75000-1714627.pdf.

52. *Mouser: 5050462-2 TE Connectivity* [online]. TE Connectivity [visited on 2022-07-24]. Available from: https://eu.mouser.com/ProductDetail/TE-Connectivity-AMP/5050462-2?qs=gcGXOotcZFAyoce5uFMggQ%3D%3D.

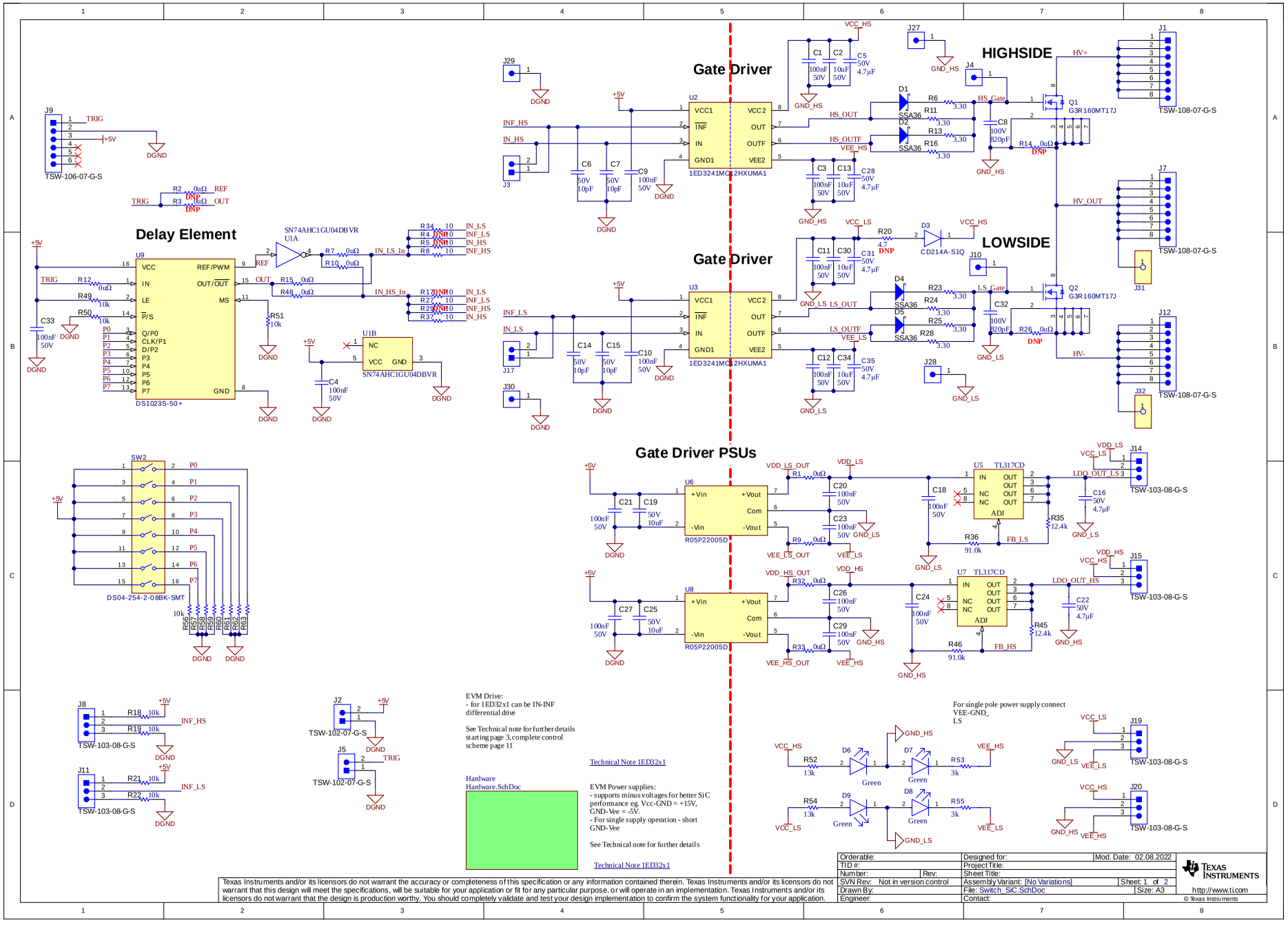
Attachments

A Schematic of the Mother board

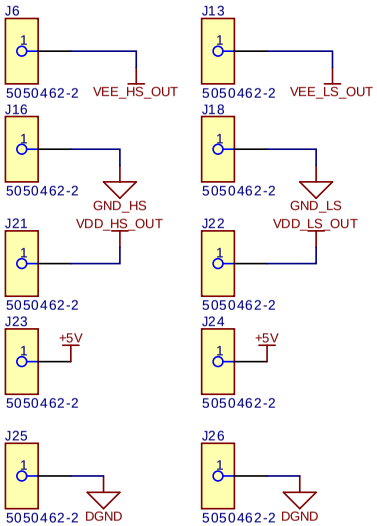

Variable V PSU up to 4kV
Interlock Connection
TRIG
Main +5V Power Input
Main HV Switch
Discharge
Filter for Ringing Suppression
HV Present Warning
Input PSUs for EVM Control
POWER ON Signalling
Discharge control
Capacitor discharge calculator
DCDC_EN: 0 -> ON
DCDC_EN : 1 -> OFF
DSG: 1 -> DSG_OFF
DSG: 0 -> DSG_ON
DCDC_EN: 0-> IF (INT:1) & (DSG:1)
Order additional for experiments
10 Ohm:
CRCW251210R0FKEGHP
50hm:
CRCW25125R10FNEHHP
DSG_Ctrl = b0:
-> K4 output : open
-> R77 pull-up : Q4 ON
DSG_Ctrl = b1 :
-> K4 output : closed
-> R77 pull-up : Q4 Off
Drop 1.4V, 7.5mA typical current
EVM Grounds:
- For single supply operation - short GND-Vee
- HV- and GND_LS connected on the EVM
- for standalone operation short using jumper
Hardware
Hardware.SchDoc
Texas Instruments and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. Texas Instruments and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. Texas Instruments and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.
Orderable:
TID #:
Number:
Rev:
SVN Rev: Not inversion control
Drawn By:
Engineer:
Designed for:
Project Title:
Sheet Title:
Assembly Variant: [No Variations]
File: Main.SchDoc
Contact:
Mod. Date: 09.08.2022
Sheet: 1 of 2
Size: A2
http://www.ti.com
© Texas Instruments


LV_DCDC
1) Find the part number for the probe and sockets - done
- Sockets:
- Smallest: 5050462-2 (.36-.66) (DCDC .5mm and Relay .63mm)
- Smaller: 5050864-8 (.71 - .84) (HV Switch (0.8mm))
- Bigger: 5050865-6 (.86 - 1.04) (Caps (1mm) and Pico(1mm))
- Probe point: 1305-0-15-15-47-27-04-0
HV Switch
PICO
HV Caps
EVM High Side PSU
EVM Low Side PSU
DSG Relay
NY PMS 440 0025 PH
2128-832-AL
Texas Instruments and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein.
Texas Instruments and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. Texas Instruments and/or its licensors do not warrant that the design is production worthy.
You should completely validate and test your design implementation to confirm the system functionality for your application.
Orderable:
Designed for:
Mod. Date: 27.07.2022
TID #:
Project Title:
Number:
Rev:
Sheet Title:
SVN Rev: Not in version control
Assembly Variant: [No Variations]
Sheet: 2 of 2
Drawn By:
File: Hardware.SchDoc
Size: A4
Engineer:
Contact:
Texas Instruments
http://www.ti.com
© Texas Instruments

B Schematic of the Daughter board


Gate Driver
HIGHSIDE
Gate Driver
LOWSIDE
Gate Driver PSUs
Delay Element
EVM Drive:
- for 1ED32x1 can be IN-INF differential drive
See Technical note for further details starting page 3, complete control scheme page 11
Technical Note 1ED32x1
Hardware
Hardware.SchDoc
EVM Power supplies:
- supports minus voltages for better SiC performance eg. Vcc-GND = +15V, GND-Vee = -5V.
- For single supply operation - short GND-Vee
See Technical note for further details
Technical Note 1ED32x1
For single pole power supply connect VEE-GND_LS
Texas Instruments and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. Texas Instruments and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. Texas Instruments and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.
Orderable:
Designed for:
Mod. Date: 02.08.2022
TID #:
Project Title:
Number:
Rev:
Sheet Title:
SVN Rev: Not in version control
Assembly Variant: [No Variations]
Sheet: 1 of 2
Drawn By:
File: Switch_SiC.SchDoc
Size: A3
Engineer:
Contact:
http://www.ti.com
© Texas Instruments

PSUs for Gate Driver



Orderable:		Designed for:	Mod. Date: 28.06.2022
TID #:		Project Title:	
Number:	Rev:	Sheet Title:	
SVN Rev: Not in version control		Assembly Variant: [No Variations]	Sheet: 2 of 2
Drawn By:		File: Hardware.SchDoc	Size: A4
Engineer:		Contact:	

TEXAS INSTRUMENTS
http://www.ti.com